LM555JAN Timer

Check for Samples: LM555JAN

FEATURES

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

DESCRIPTION

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

Connection Diagram

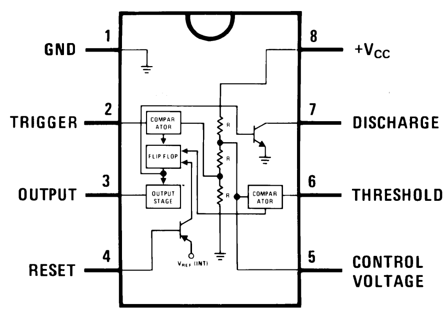


Figure 1. Dual-In-Line Package

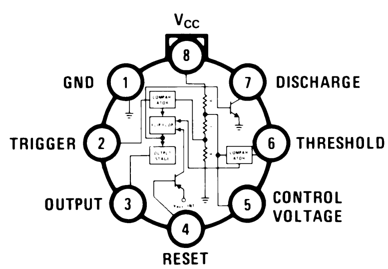
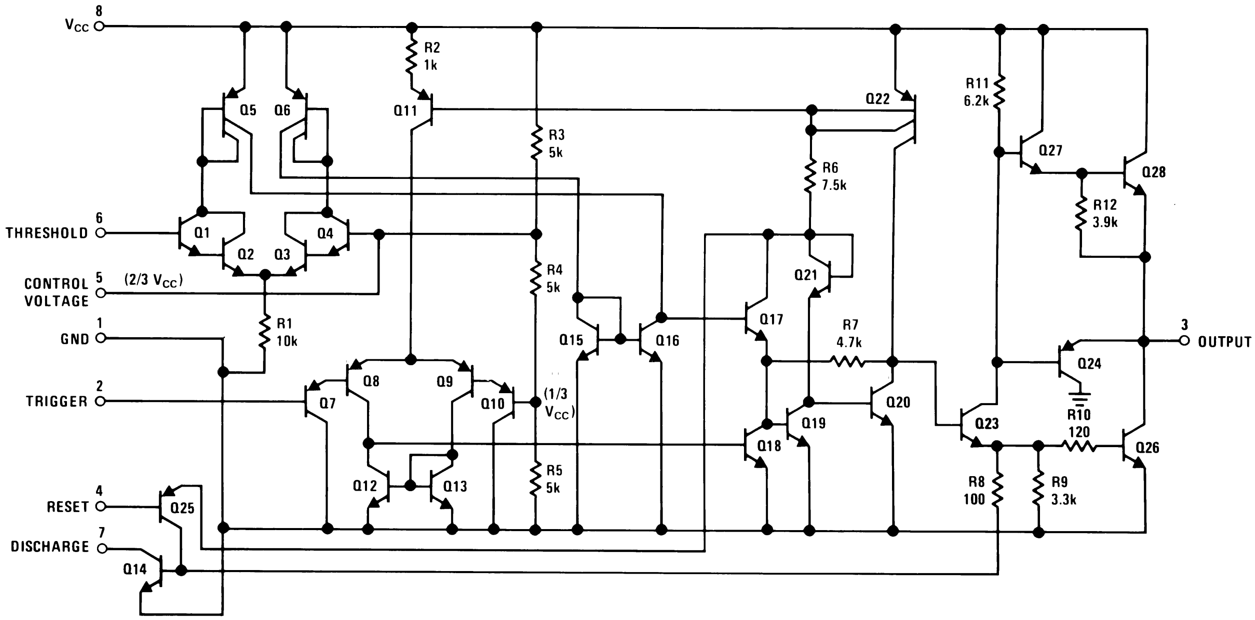


Figure 2. Metal Can Package

Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

Supply Voltage	+18V
Discharge Current	+200mA
Output Sink Current	+200mA
Output Source Current	−200mA
Power Dissipation [2]	
Metal Can	300mW @ +125°C
CERDIP	370mW @ +125°C
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C
Maximum Junction Temperature (T_{Jmax})	+175°C
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Soldering Information (Soldering 10 Seconds)	300°C
Thermal Resistance	
θ_{JA}	
CERDIP Still Air	123°C/W
CERDIP 500LF / Min Air Flow	69°C/W
Metal Can Still Air	171°C/W
Metal Can 500LF / Min Air Flow	92°C/W
θ_{JC}	
CERDIP	18°C/W
Metal Can	41°C/W
ESD Tolerance [3]	1KV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(3) Human body model, 1.5KΩ in series with 100pF.

Recommended Operating Conditions

Supply Voltage Range	+4.5V to +16V_{DC}

Table 1. Quality Conformance InspectionMil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

Electrical Characteristics DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Power Supply Current	V_{CC} = 4.5V			5.0	mA	1, 2, 3
		V_{CC} = 16.5V			20	mA	1, 2, 3
V_{Trig}	Trigger Voltage	V_{CC} = 4.5V		1.3	1.8	V	1
				1.3	2.1	V	2
				1.15	1.8	V	3
		V_{CC} = 16.5V		5.2	5.8	V	1
				5.2	6.1	V	2
				5.0	5.8	V	3
I_{Trig}	Trigger Current	V_{CC} = 16.5V		-5.0		µA	1, 2, 3
V_{Th}	Threshold Voltage	V_{CC} = 4.5V		2.7	3.3	V	1
				2.6	3.4	V	2, 3
		V_{CC} = 16.5V		10.7	11.3	V	1
				10.6	11.4	V	2, 3
I_{Th}	Threshold Current	V_{CC} = 16.5V			250	nA	1, 2
					2,50 0	nA	3
V_{OL}	Logical "0" Output Voltage	V_{CC} = 4.5V, I_{Sink} = 5mA			0.25	V	1
					0.35	V	2, 3
		V_{CC} = 4.5V, I_{Sink} = 50mA			2.2	V	1, 2
					2.6	V	3
		V_{CC} = 16.5V, I_{Sink} = 10mA			0.15	V	1, 3
					0.25	V	2
		V_{CC} = 16.5V, I_{Sink} = 50mA			0.5	V	1, 3
					0.7	V	2
		V_{CC} = 16.5V, I_{Sink} = 100mA			2.2	V	1
					2.8	V	2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, I_{Source} = -100mA		2.6		V	1, 2
				2.2		V	3
		V_{CC} = 16.5V, I_{Source} = -100mA		14.6		V	1, 2
				14		V	3
I_{CEX}	Discharge Transistor Leakage Current	V_{CC} = 16.5V			100	nA	1, 3
					3,00 0	nA	2
V_{Sat}	Discharge Transistor Saturation Voltage	V_{CC} = 16.5V			0.8	V	1, 3
					1.0	V	2
V_R	Reset Voltage	V_{CC} = 16.5V	[1], [2]	0.1	1.3	V	1, 2, 3
I_R	Reset Current	V_{CC} = 16.5V		-1.6		mA	1, 2, 3

(1) Parameter tested go-no-go, only.
(2) Datalog reading of 0.7V will reflect the Reset Voltage levels passing and a reading of 0.5V or 1.5V reflects the Reset voltage levels failing the low level or high level respectfully.

Electrical Characteristics AC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{PLH}	Propagation Delay Time	V_{CC} = 4.5V			800	nS	9, 11
					900	nS	10
		V_{CC} = 16.5V			800	nS	9, 11
					900	nS	10
t_{PHL}	Propagation Delay Time	V_{CC} = 4.5V			12	µS	9, 10, 11
		V_{CC} = 16.5V			12	µS	9, 10, 11
t_{TLH}	Transition Time	V_{CC} = 4.5V			300	nS	9, 10, 11
		V_{CC} = 16.5V			300	nS	9, 10, 11
t_{THL}	Transition Time	V_{CC} = 4.5V			300	nS	9, 10, 11
		V_{CC} = 16.5V			300	nS	9, 10, 11
t_{DOH}	Time Delay Output High R_T = 1KΩ	V_{CC} = 4.5V		106.7	113.3	µS	9, 10, 11
		V_{CC} = 16.5V		106.7	113.3	µS	9, 10, 11
	Time Delay Output High R_T = 100KΩ	V_{CC} = 4.5V		10.67	11.33	mS	9, 10, 11
		V_{CC} = 16.5V		10.67	11.33	mS	9, 10, 11
$\Delta t_D / \Delta V_{CC}$	Drift In Time Delay	ΔV_{CC} = 12, V_{CC} = 4.5V to 16.5V	(1)	-220	220	nS/V	9
$\Delta t_D / \Delta T$	Temperature Coefficient of Time Delay	V_{CC} = 16.5V		-11	11	nS/°C	10, 11
t_{Ch}	Capacitor Charge Time R_T = 1KΩ	V_{CC} = 4.5V		120	156	µS	9, 10, 11
		V_{CC} = 16.5V		120	156	µS	9, 10, 11
	Capacitor Charge Time R_T = 100KΩ	V_{CC} = 4.5V		11.3	15	mS	9, 10, 11
		V_{CC} = 16.5V		11.3	15	mS	9, 10, 11
t_{Dis}	Capacitor Discharge Time R_T = 1KΩ	V_{CC} = 4.5V		57.5	80	µS	9, 10, 11
		V_{CC} = 16.5V		57.5	80	µS	9, 10, 11
	Capacitor Discharge Time R_T = 100KΩ	V_{CC} = 4.5V		5.4	7.7	mS	9, 10, 11
		V_{CC} = 16.5V		5.4	7.7	mS	9, 10, 11
$\Delta t_{Ch} / \Delta V_{CC}$	Drift In Capacitor Charge Time	ΔV_{CC} = 12, V_{CC} = 4.5V to 16.5V		-820	820	nS/V	9
$\Delta t_{Ch} / \Delta T$	Temperature Coefficient Capacitor Charge Time	V_{CC} = 16.5V	(1)	-68	68	nS/°C	10, 11
t_{Res}	Reset Time	V_{CC} = 16.5V			1.5	µS	9, 11
					2.0	µS	10

(1) Calculated parameter.

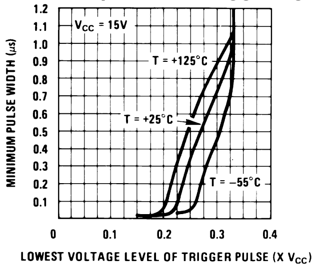
Electrical Characteristics DC Drift Parameters

Delta calculations performed on JAN S devices at Group B, Subgroup 5, only.

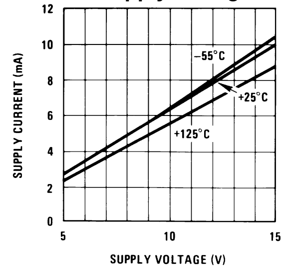
Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{Trig}	Trigger Voltage	V_{CC} = 16.5V		-0.05	0.05	V	1
V_{Th}	Threshold Voltage	V_{CC} = 16.5V		-0.05	0.05	V	1
V_{OL}	Logical "0" Output Voltage	V_{CC} = 16.5V, I_{Sink} = 10mA		-0.05	0.05	V	1
I_{CEX}	Discharge Transistor Leakage Current	V_{CC} = 16.5V		-50	50	nA	1

Typical Performance Characteristics

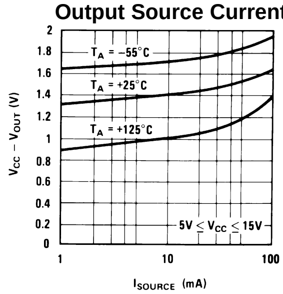
Minimum Pulse Width Required for Triggering



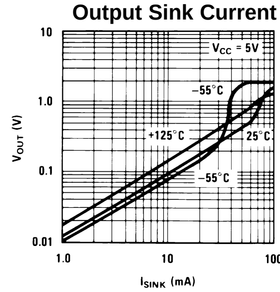
Supply Current vs. Supply Voltage



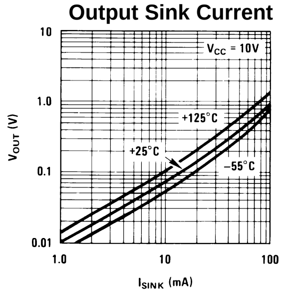
High Output Voltage vs. Output Source Current



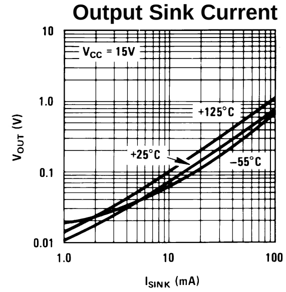
Low Output Voltage vs. Output Sink Current



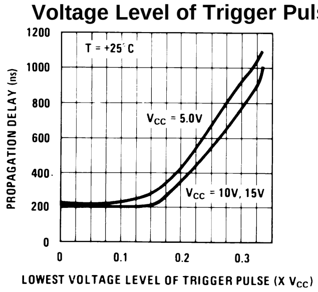
Low Output Voltage vs. Output Sink Current



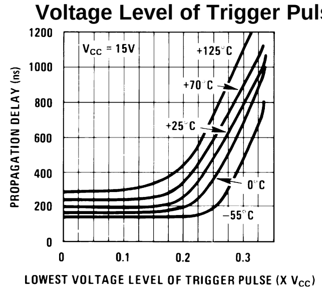
Low Output Voltage vs. Output Sink Current



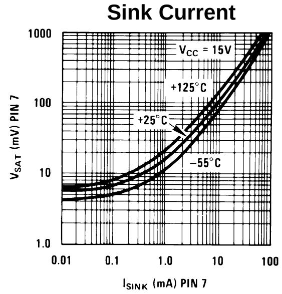
Output Propagation Delay vs. Voltage Level of Trigger Pulse



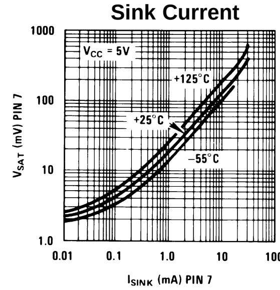
Output Propagation Delay vs. Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs. Sink Current



Discharge Transistor (Pin 7) Voltage vs. Sink Current



Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (Figure 3). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

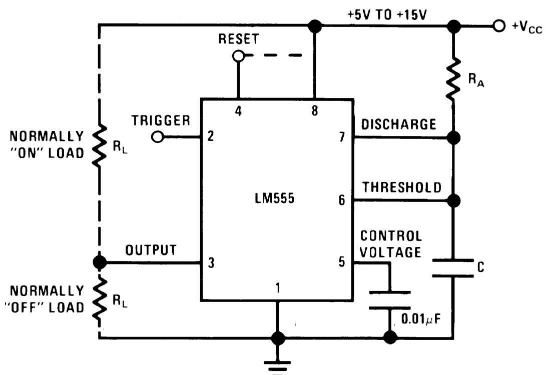
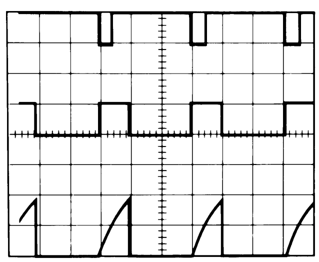


Figure 3. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 4 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1kΩ
C = 0.01μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

Figure 4. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 5 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

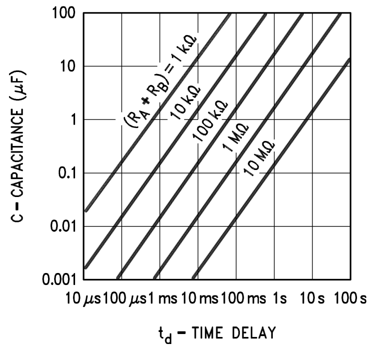


Figure 5. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in Figure 6 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

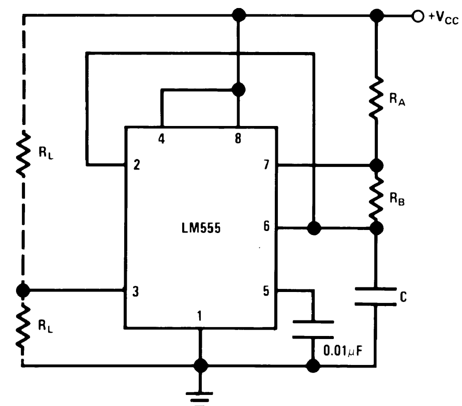
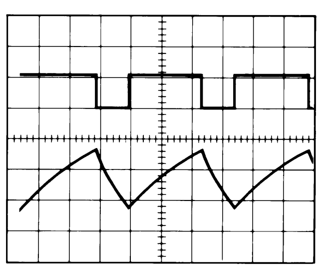


Figure 6. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 7 shows the waveforms generated in this mode of operation.



V_{CC} = 5V
TIME = 20μs/DIV.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

Figure 7. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C \tag{1}$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C \tag{2}$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C \tag{3}$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C} \tag{4}$$

Figure 8 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B} \tag{5}$$

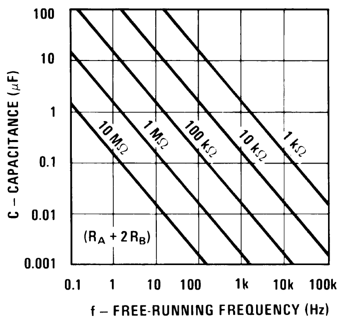
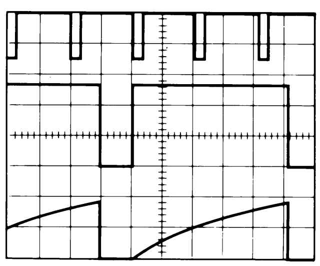


Figure 8. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of Figure 3 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 9 shows the waveforms generated in a divide by three circuit.



V_{CC} = 5V — Top Trace: Input 4V/Div.
TIME = 20μs/DIV. — Middle Trace: Output 2V/Div.
R_A = 9.1kΩ — Bottom Trace: Capacitor 2V/Div.
C = 0.01μF

Figure 9. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 10 shows the circuit, and in Figure 11 are some waveform examples.

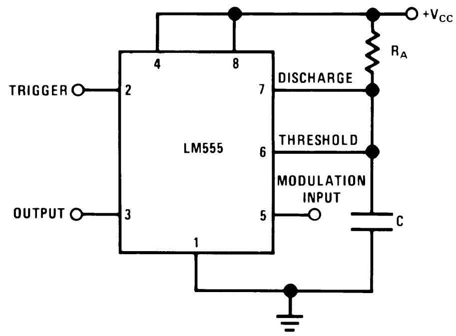
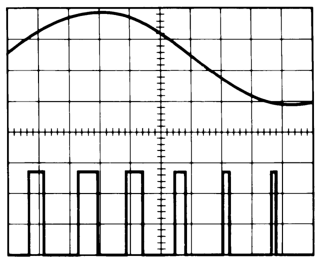


Figure 10. Pulse Width Modulator



V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01μF

Figure 11. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in Figure 12, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 13 shows the waveforms generated for a triangle wave modulation signal.

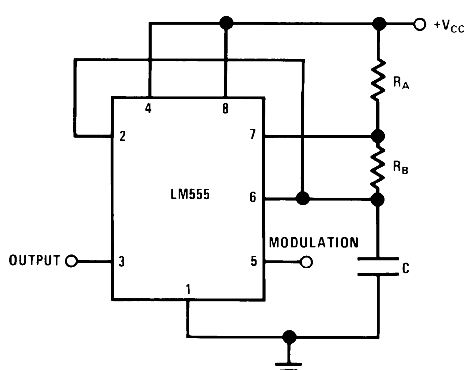
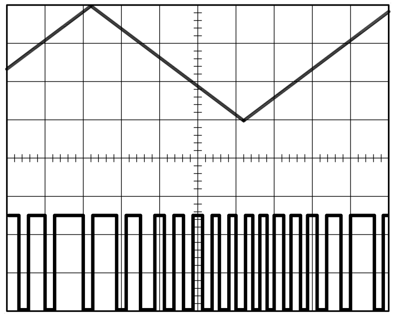


Figure 12. Pulse Position Modulator



V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01μF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

Figure 13. Pulse Position Modulator

LINEAR RAMP

When the pull-up resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 14 shows a circuit configuration that will perform this function.

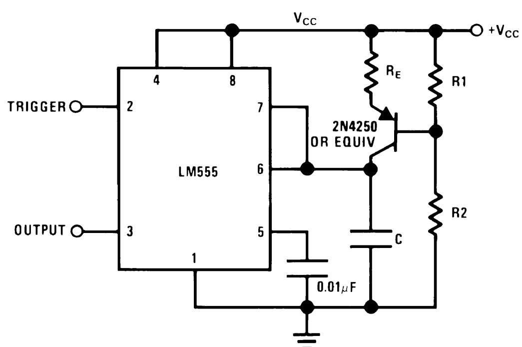


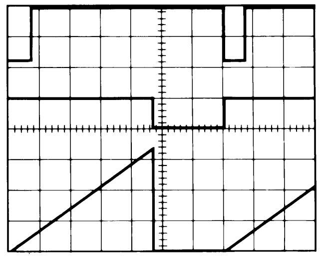
Figure 14.

Figure 15 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1 V_{CC} - V_{BE}\, (R_1 + R_2)} \qquad V_{BE} \cong 0.6V \tag{6}$$

$$V_{BE} \simeq 0.6V \tag{7}$$



V_{CC} = 5V Top Trace: Input 3V/Div.
TIME = 20μs/DIV. Middle Trace: Output 5V/Div.
R_1 = 47kΩ Bottom Trace: Capacitor Voltage 1V/Div.
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 μF

Figure 15. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in Figure 16. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right] \quad (8)$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2} \quad (9)$$

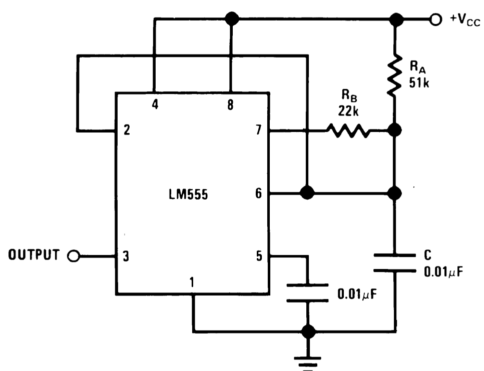


Figure 16. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Table 2. Revision History

Date Released	Revision	Section	Changes
08/04/05	A	New Release to corporate format	1 MDS datasheet converted into corporate format. MJLM555-X Rev 1A0 to be archived
07/25/06	B	Applications Information, page 8	Correct a typo in the paragraph after figure 1 (change the word internal to interval) to reflect same change made to Commercial data sheet. Revision A will be Archived.
09/27/2010	C	Obsolete Data Sheet	End Of Life on Product/NSID Sept. 1998