LM565/LM565C Phase Locked Loop

Check for Samples: LM565, LM565C

FEATURES

- **200 ppm/°C frequency stability of the VCO**
- **Power supply range of ±5 to ±12 volts with 100 ppm/% typical**
- **0.2% linearity of demodulated output**
- **Linear triangle wave with in phase zero crossings available**
- **TTL and DTL compatible phase detector input and square wave output**
- **Adjustable hold in range from ±1% to > ±60%**

APPLICATIONS

- **Data and tape synchronization**
- **Modems**
- **FSK demodulation**
- **FM demodulation**
- **Frequency synthesizer**
- **Tone decoding**
- **Frequency multiplication and division**
- **SCA demodulators**
- **Telemetry receivers**
- **Signal regeneration**
- **Coherent demodulators**

DESCRIPTION

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CN is specified for operation over the 0°C to +70°C temperature range.

Connection Diagram

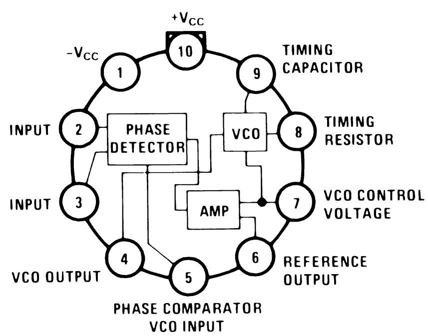


Figure 1. Metal Can Package

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

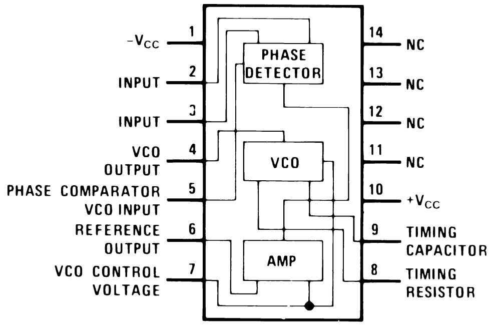


Figure 2. Dual-in-Line Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

Supply Voltage	±12V
Power Dissipation [2]	1400 mW
Differential Input Voltage	±1V
Operating Temperature Range	
LM565H	−55°C to +125°C
LM565CN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) The maximum junction temperature of the LM565 and LM565C is +150°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W junction to ambient or +45°C/W junction to case. Thermal resistance of the dual-in-line package is +85°C/W.

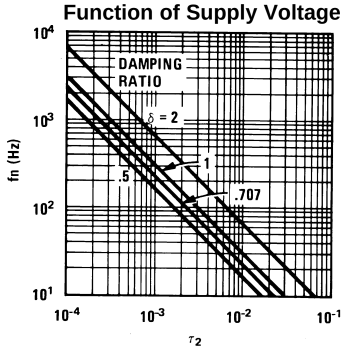
Electrical Characteristics

AC Test Circuit, $T_A = 25°C$, $V_{CC} = ±6V$

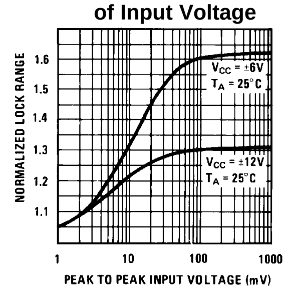
Parameter	Conditions	LM565			LM565C			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	$-4V < V_2, V_3 < 0V$	7	10			5		kΩ
VCO Maximum Operating Frequency	$C_o = 2.7$ pF	300	500		250	500		kHz
VCO Free-Running Frequency	$C_o = 1.5$ nF $R_o = 20$ kΩ $f_o = 10$ kHz	−10	0	+10	−30	0	+30	%
Operating Frequency Temperature Coefficient			−100			−200		ppm/°C
Frequency Drift with Supply Voltage			0.1	1.0		0.2	1.5	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{p-p}
Triangle Wave Output Linearity			0.2			0.5		%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{p-p}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	$f_o = 10$ kHz		6600			6600		Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	400	200	300	450	mV_{p-p}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\|V_7 - V_6\|$			30	100		50	200	mV
Temperature Drift of $\|V_7 - V_6\|$			500			500		μV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D			0.68			0.68		V/radian

Typical Performance Characteristics

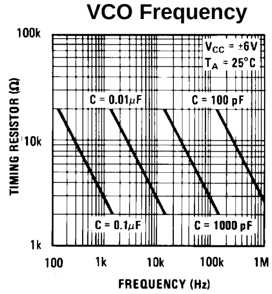
Power Supply Current as a Function of Supply Voltage



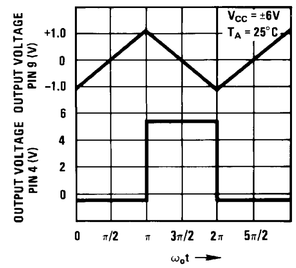
Lock Range as a Function of Input Voltage



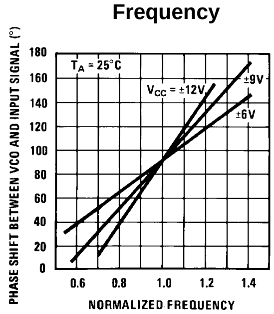
VCO Frequency



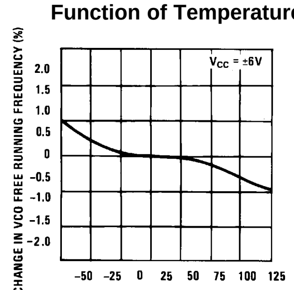
Oscillator Output Waveforms



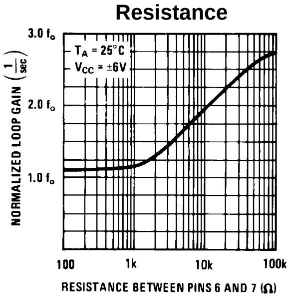
Phase Shift vs Frequency



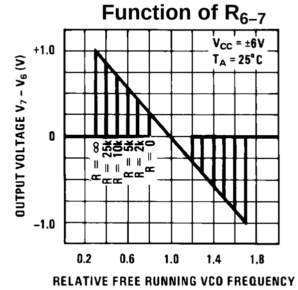
VCO Frequency as a Function of Temperature



Loop Gain vs Load Resistance



Hold in Range as a Function of R_{6-7}



Schematic Diagram

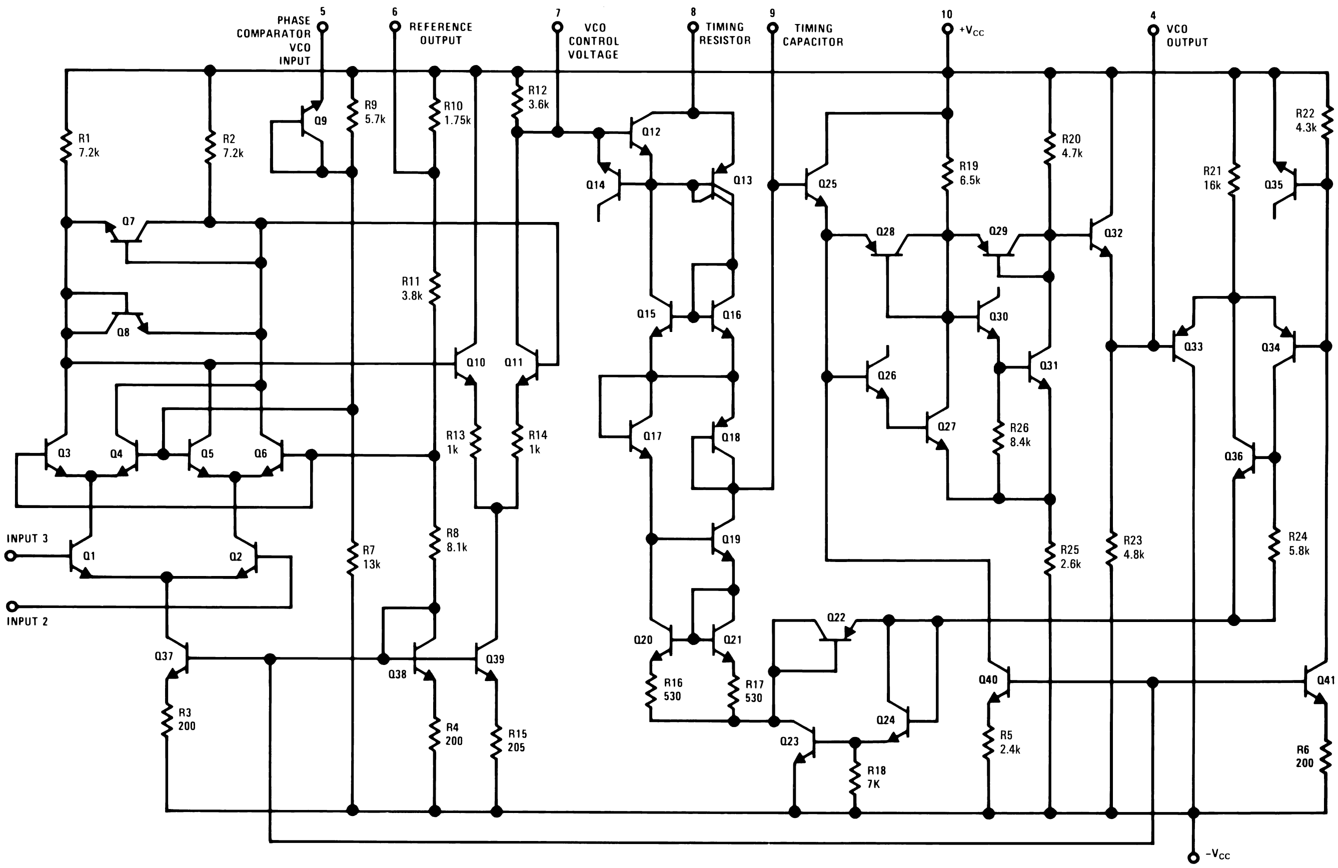
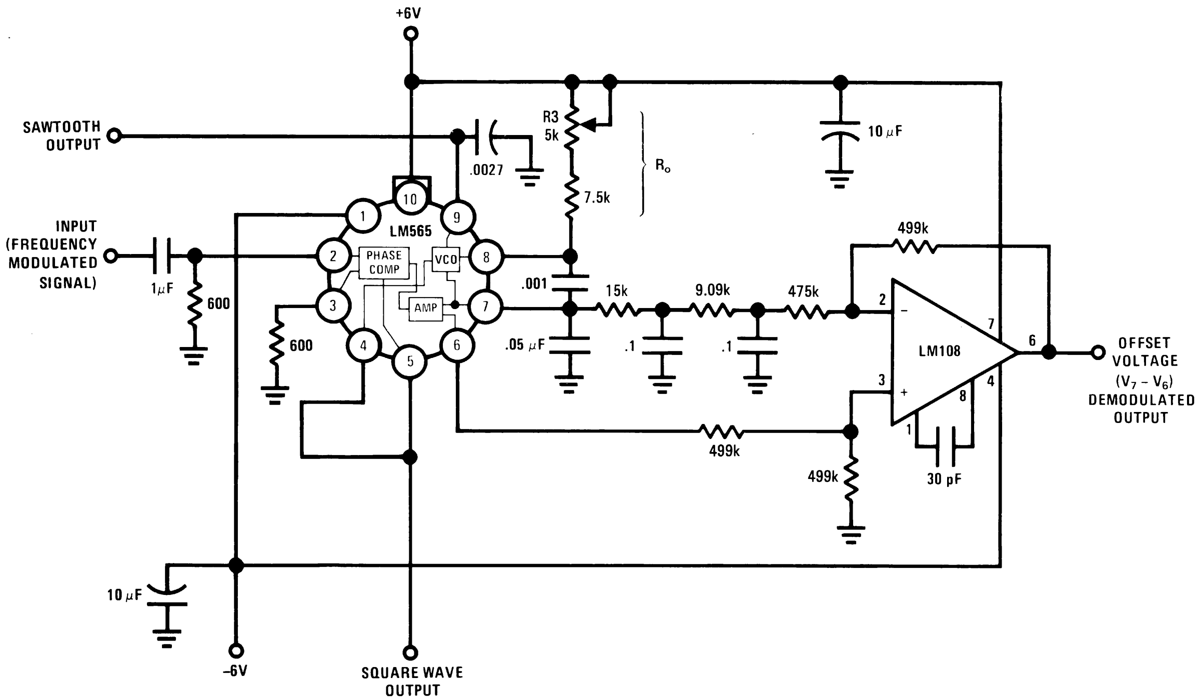


Figure 3. Schematic Diagram

AC Test Circuit



Note: S_1 open for output offset voltage ($V_7 - V_6$) measurement.

Figure 4. AC Test Circuit

Typical Applications

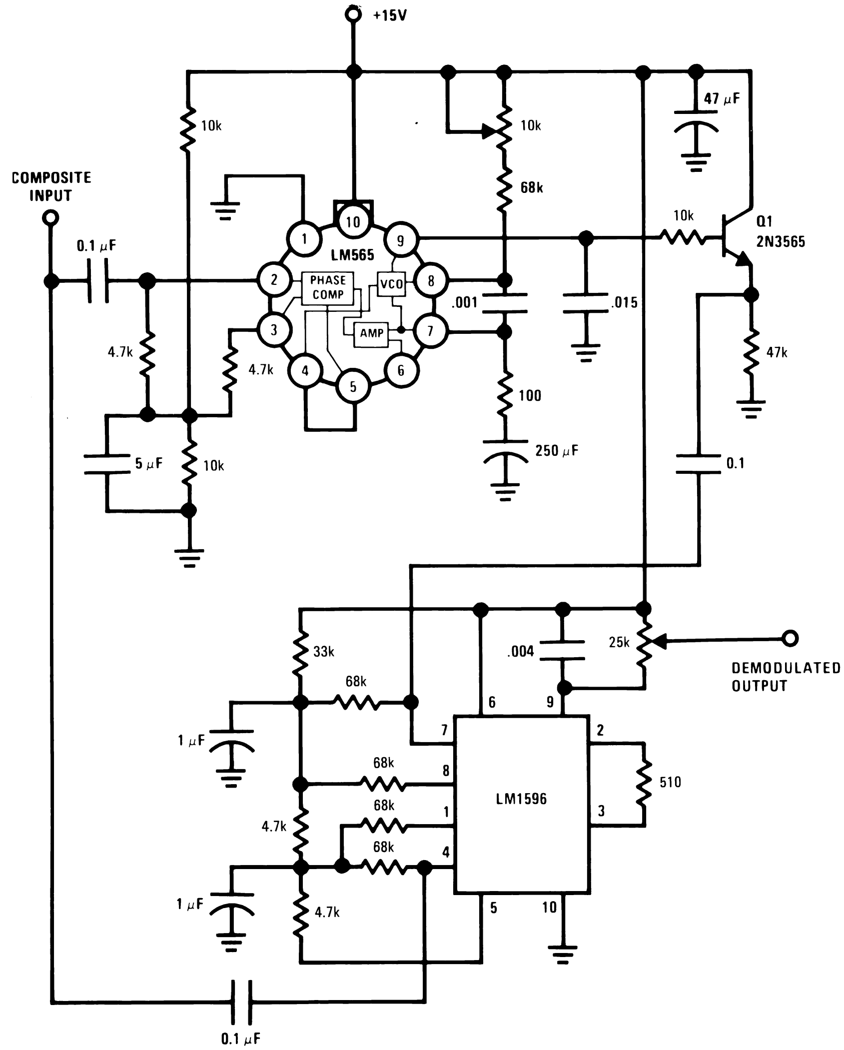


Figure 5. 2400 Hz Synchronous AM Demodulator

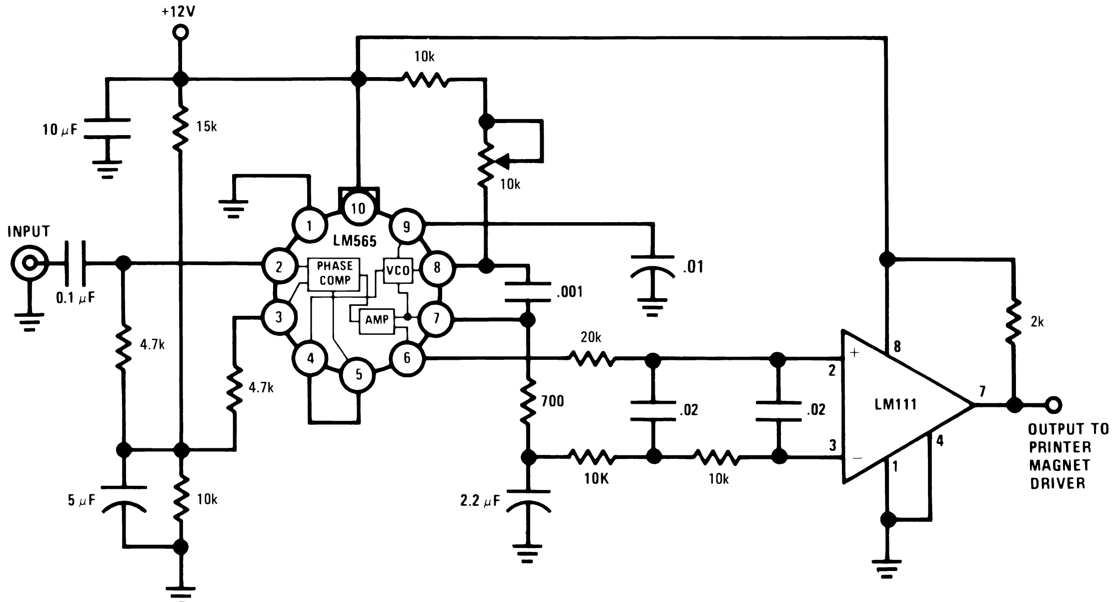


Figure 6. FSK Demodulator (2025–2225 cps)

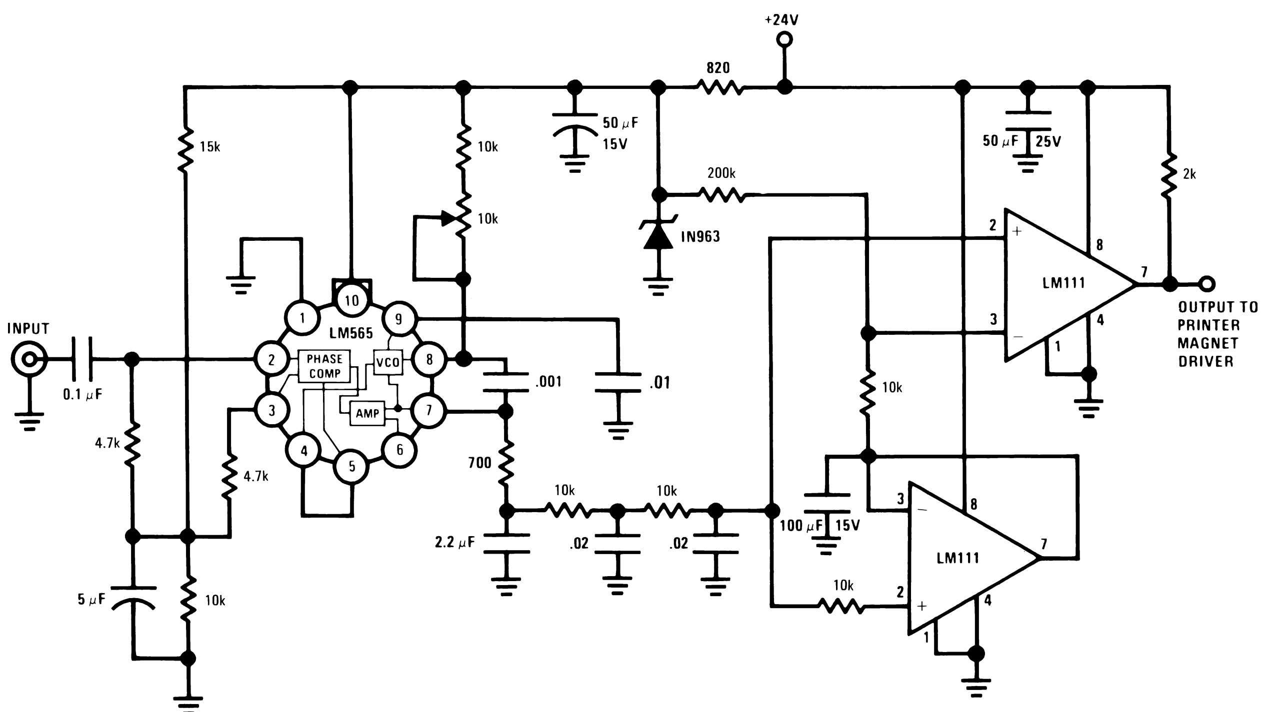


Figure 7. FSK Demodulator with DC Restoration

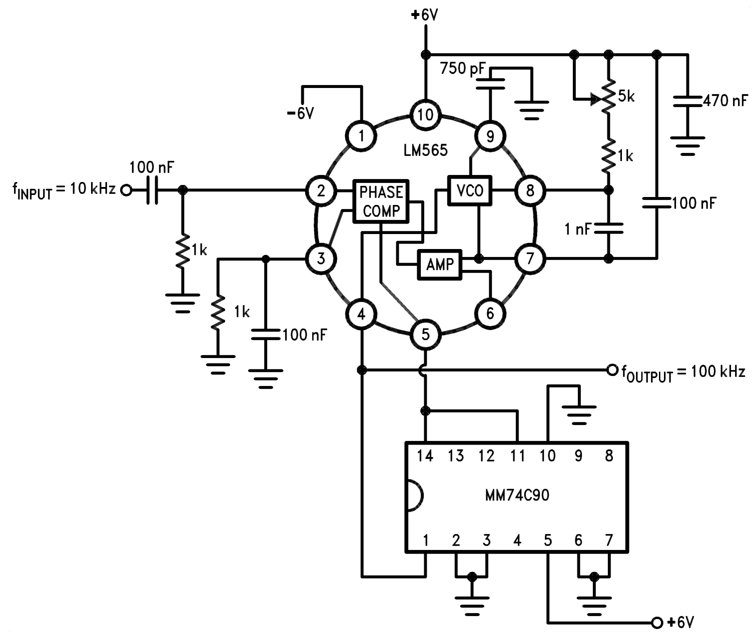


Figure 8. Frequency Multiplier (×10)

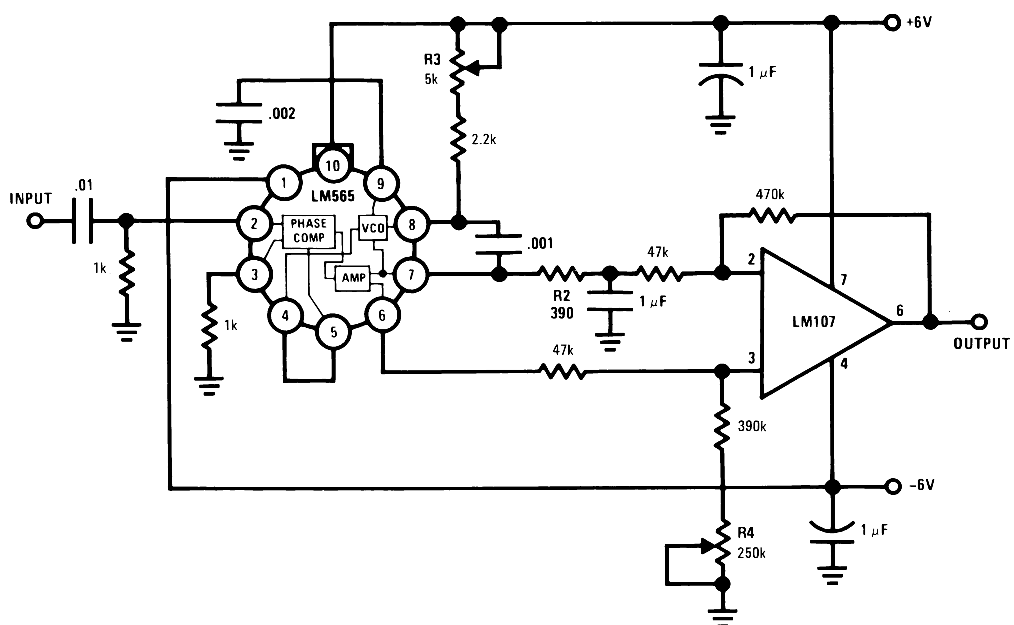


Figure 9. IRIG Channel 13 Demodulator

APPLICATIONS INFORMATION

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o \cong \frac{0.3}{R_o C_o} \quad (1)$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo theory, this is called the “velocity error coefficient.”

$$\text{Loop gain} = K_o K_D \left(\frac{1}{\text{sec}}\right)$$
$$K_o = \text{oscillator sensitivity} \left(\frac{\text{radians/sec}}{\text{volt}}\right)$$
$$K_D = \text{phase detector sensitivity} \left(\frac{\text{volts}}{\text{radian}}\right) \quad (2)$$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6\, f_o}{V_C} \quad (3)$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

$$f_H = \pm \frac{8\, f_o}{V_C} \quad (4)$$

f_o= free running frequency of VCO

V_c= total supply voltage to the circuit

THE LOOP FILTER

In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7); this filter may take one of two forms:

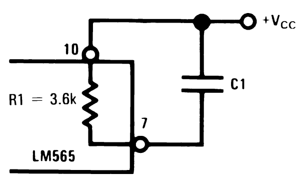


Figure 10. Simple Lead Filter

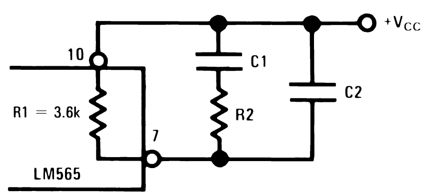


Figure 11. Lag-Lead Filter

A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi} \sqrt{\frac{K_o K_D}{R_1 C_1}} \quad (5)$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2} \sqrt{\frac{1}{R_1 C_1 K_o K_D}} \quad (6)$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1C_1 < K_o K_D$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

$$\tau_1 + \tau_2 = (R_1 + R_2)\, C_1 \quad (7)$$

R_2 is selected to produce a desired damping factor δ, usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta \cong \pi \, \tau_2 f_n \quad (8)$$

These two equations are plotted for convenience.

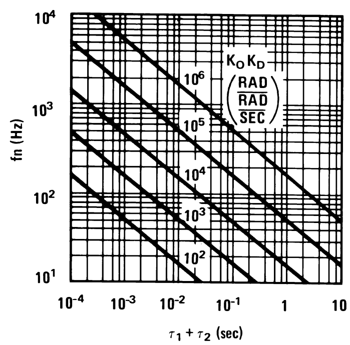


Figure 12. Filter Time Constant vs Natural Frequency

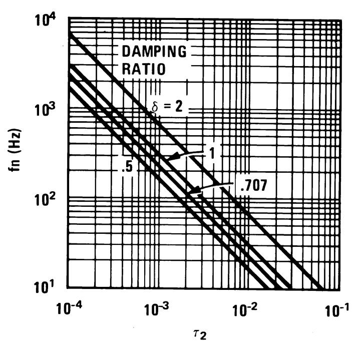


Figure 13. Damping Time Constant vs Natural Frequency

Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of carrier. In general $C_2 \le 0.1\, C_1$.