National Semiconductor

LM6121/LM6221/LM6321 High Speed Buffer

General Description

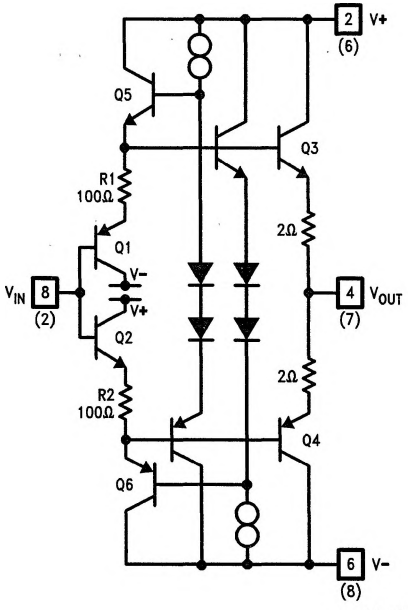
These high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. They can drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6121 family are monolithic ICs which offer performance similar to the LH0002 with the additional features of current limit and thermal shutdown.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

- High slew rate — 800 V/μs
- Wide bandwidth — 50 MHz
- Slew rate and bandwidth 100% tested
- Peak output current — ±300 mA
- High input impedance — 5 MΩ
- LH0002H pin compatible
- No oscillations with capacitive loads
- 5V to ±15V operation guaranteed
- Current and thermal limiting
- Fully specified to drive 50Ω lines

Simplified Schematic



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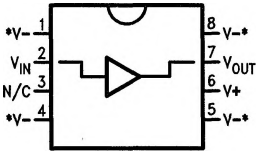
Numbers in ( ) are for 8-pin N DIP.

Pin Configurations



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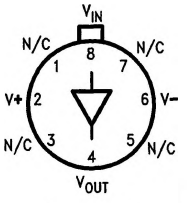
*Heat-sinking pins.

Order Number LM6221N or LM6321N
See NS Package Number N08E



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Top View

Note: Pin 6 connected to case.

Order Number LM6121H or LM6221H
See NS Package Number H08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V (±18)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance (Note 10)	±2000V

	Package H	Package N
θ_{JA} (Note 4)	150°C/W	47°C/W
Maximum Junction Temp. (T_j)	150°C	150°C
Operating Temperature Range		
LM6121	−55°C to +125°C	
LM6221	−40°C to +85°C	
LM6321	0°C to +70°C	
Operating Supply Range	4.75 to ±16V	

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	Typ	LM6121 Tested Limit (Note 6)	LM6121 Design Limit (Note 7)	LM6221 Tested Limit (Note 6)	LM6221 Design Limit (Note 7)	LM6321 Tested Limit (Note 6)	LM6321 Design Limit (Note 7)	Units
A_{V1}	Voltage Gain 1	R_L = 1k, V_{IN} = ±10V	0.990	0.980 **0.970**		0.980	**0.950**	0.970	**0.950**	
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_{IN} = ±10V	0.900	0.860 **0.800**		0.860	**0.820**	0.850	**0.820**	V/V Min
A_{V3}	Voltage Gain 3 (Note 8)	R_L = 50Ω V_{IN} = 2 V_{pp} V^+ = 5V **(1.5 V_{pp})**	0.840	0.780 **0.750**		0.780	**0.700**	0.750	**0.700**	
V_{OS}	Offset Voltage	R_L = 1 kΩ	15	30 **50**		30	**60**	50	**100**	mV Max
I_B	Input Bias Current	R_L = 1 kΩ, R_S = 10 kΩ	1	4 **7**		4	**7**	5	**7**	μA Max
R_{IN}	Input Resistance	R_L = 50Ω	5							MΩ
C_{IN}	Input Capacitance		3.5							pF
R_O	Output Resistance	I_{OUT} = ±10 mA	3	5 **10**		5	**10**	5	**6**	Ω Max
I_{S1}	Supply Current 1	R_L = ∞	15	18 **20**		18	**20**	20	**22**	mA Max
I_{S2}	Supply Current 2	R_L = ∞, V^+ = 5V	14	16 **18**		16	**18**	18	**20**	
V_{O1}	Output Swing 1	R_L = 1k	13.5	13.3 **13**		13.3	**13**	13.2	**13**	
V_{O2}	Output Swing 2	R_L = 100Ω	12.7	11.5 **10**		11.5	**10**	11	**10**	±V Min
V_{O3}	Output Swing 3	R_L = 50Ω	12	11 **9**		11	**9**	10	**9**	
V_{O4}	Output Swing 4	R_L = 50Ω V^+ = 5V (Note 8)	1.8	1.6 **1.3**		1.6	**1.4**	1.6	**1.5**	V_{pp} Min
PSSR	Power Supply Rejection Ratio	$V^{\pm}$ = ±5V to ±15V	70	60 **55**		60	**50**	60	**50**	dB Min

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	Typ	LM6121		LM6221		LM6321		Units
				Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	
SR_1	Slew Rate 1	$V_{IN} = \pm 11V$, $R_L = 1\ k\Omega$	1200							
SR_2	Slew Rate 2	$V_{IN} = \pm 11V$, $R_L = 50\Omega$ (Note 9)	800	550		550		550		V/μs Min
SR_3	Slew Rate 3	$V_{IN} = 2\ V_{pp}$, $R_L = 50\Omega$, $V^+ = 5V$ (Note 8)	50							
BW	−3 dB Bandwidth	$V_{IN} = \pm 100\ mV_{pp}$, $R_L = 50\Omega$, $C_L \leq 10\ pF$	50	30		30		30		MHz Min
t_r, t_f	Rise Time, Fall Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$, $V_O = 100\ mV_{pp}$	7.0							ns
t_{pd}	Propagation Delay Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$, $V_O = 100\ mV_{pp}$	4.0							ns
	Overshoot	$R_L = 50\Omega$, $C_L \leq 10\ pF$, $V_O = 100\ mV_{pp}$	10							%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit or thermal limit, the input current will increase if the input to output differential voltage exceeds 8V. For input to output differential voltages in excess of 8V the input current should be limited to ±20 mA.

Note 3: The LM6121 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: For operation at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max, with $T_J = T_A + \theta_{JA}PD$. θ_{JC} for the LM6121H and LM6221H is 17°C/W. The thermal impedance θ_{JA} of the device in the N package is 47°C/W when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 4, 5 and 8) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal impedance θ_{JA} of the N package is 84°C/W.

Note 5: $R_S = 50\Omega$, $V_S = \pm 15V$, unless otherwise specified. **Boldface** numbers apply over the operating temperature range. Numbers in standard typeface apply at $T_A = 25°C$. Electrical tests are performed with high-speed automated test equipment, so that $T_J = T_A$, unless otherwise noted.

Note 6: Guaranteed and 100% production tested.

Note 7: Guaranteed over the operating temperature range (but not 100% tested).

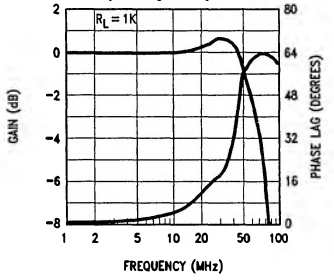
Note 8: The input is biased to 2.5V and V_{IN} swings V_{pp} about this value. The input swing is 2 V_{pp} at all temperatures except for the A_V3 test at −55°C where it is reduced to 1.5 V_{pp}.

Note 9: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/μs.

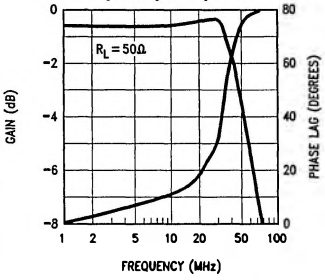
Note 10: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

Typical Performance Characteristics T_J = 25°C, unless otherwise specified

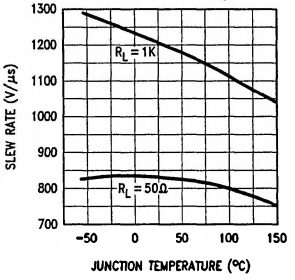
Frequency Response



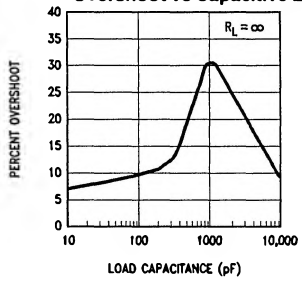
Frequency Response



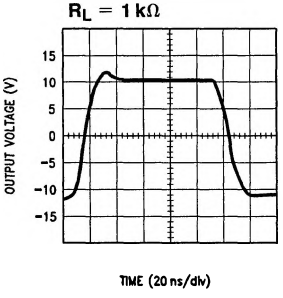
Slew Rate vs Temperature



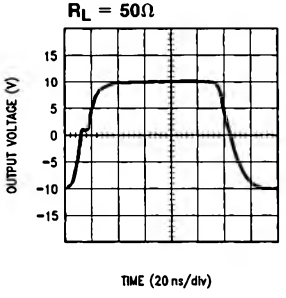
Overshoot vs Capacitive Load



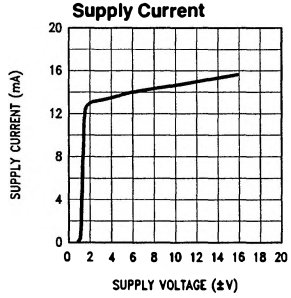
Large Signal Response
R_L = 1 kΩ



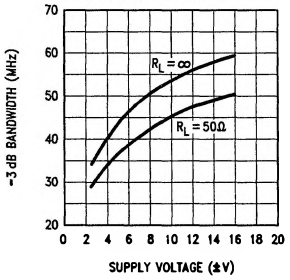
Large Signal Response
R_L = 50Ω



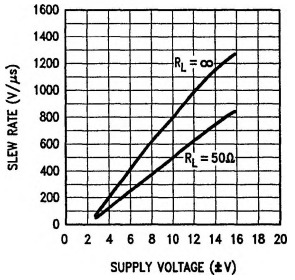
Supply Current



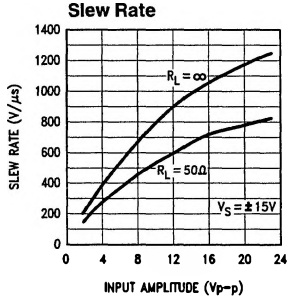
−3 dB Bandwidth



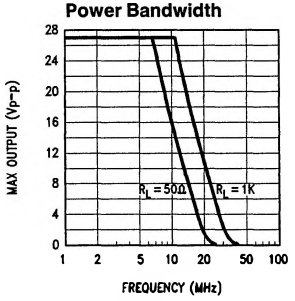
Slew Rate



Slew Rate



Power Bandwidth



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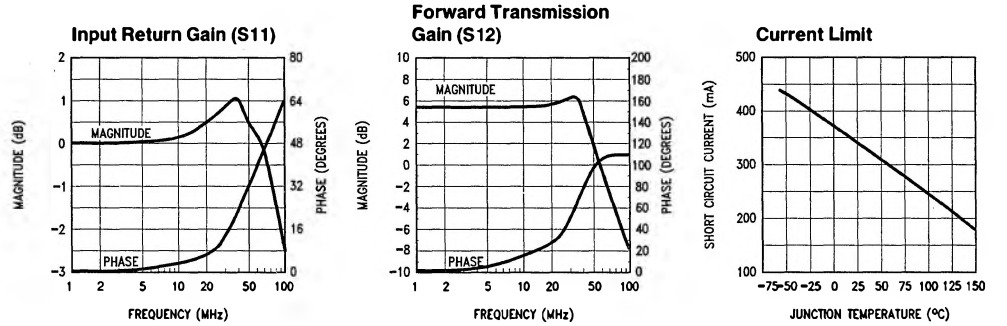
Typical Performance Characteristics T_J = 25°C, unless otherwise specified (Continued)



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Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6121 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/μs into a 50Ω load produces a di/dt of 18 A/μs. Multiplying this by a wiring inductance of 50 nH result in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 μF ceramic in parallel with one or two 2.2 μF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6121 is stable to any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

Like any high frequency buffer, the LM6121 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

OVERVOLTAGE PROTECTION

The LM6121 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6121 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. The damage is cumulative, and may eventually result in complete device failure.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6121 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.

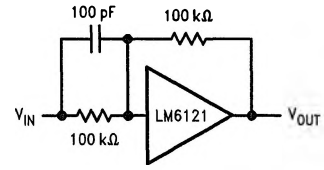

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FIGURE 1. LM6121 with Overvoltage Protection