National Semiconductor

LM614A/LM614 Quad Operational Amplifiers and Adjustable Reference

General Description

The quad operational amplifiers are a versatile common-mode-to-the-negative-supply ("single supply") type similar to the LM124 series, but with improved slew rate, improved power bandwidth, reduced cross-over distortion, and low supply current even while driven beyond swing limits. Lateral PNP input transistors enable low input currents for large differential input voltages and swings above V^+.

The voltage reference is a three-terminal shunt-type bandgap similar to the adjustable LM185 series, but with anode committed to the V^- terminal and improved voltage accuracy to ±0.4%. Two resistors program the reference from 1.24V to 6.3V. The reference features operation over a shunt current range of 16 μA to 20 mA, low dynamic impedance, broad capacitive load range, and cathode terminal voltage ranging from a diode-drop below V^- to above V^+.

As a member of National's new Super-Block™ family, the LM614 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features (Guaranteed over temperature & supply)

Op Amps

■ Low operating current	250 μA (per op amp) 16 μA (reference)
■ Large supply voltage range	4V to 36V
■ Large output swing (10k load)	(V^- + 1V) to (V^+ − 1.8V)
■ Input common-mode includes	V^- to (V^+ − 1.4V)
■ Wide input differential voltage	±36V
■ Standard quad op amp pin-out	

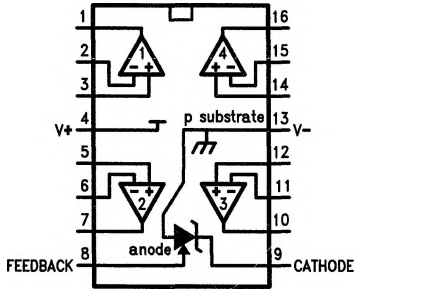
Reference

■ Adjustable output voltage	1.2V to 6.3V
■ Tight initial tolerance available	±0.4%
■ Tolerant of load capacitance	0 to ∞

Applications

- Power supplies
- Signal conditioning

Connection Diagram



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Top View

Order Number LM614IJ, LM614MJ, LM614CWM, LM614IWM, LM614AIN, LM614CN or LM614IN
See NS Package Number J16A, M16B or N16A

Order Number

Prime Military Tested at −55°C, +25°C, +125°C Drift tested at −55°C, +25°C, +125°C	LM614MJ
Prime Industrial Tested at +25°C Drift tested at −40°C, +25°C, +85°C	LM614AIN
Industrial Tested at +25°C	LM614IN LM614IJ LM614IWM
Commerical Tested at +25°C	LM614CN LM614CWM

Packages

J	Hermetic Dual-In-Line
N	Plastic Dual-In-Line
WM	Plastic Surface Mount Wide (0.3")

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin except Cathode Pin (referred to V^- pin) (Note 1) −0.3V (Min)
- Military and Industrial 36V
- Commercial 32V

Current through Any Input Pin and Cathode Pin ±20 mA

Differential Input Voltage
- Military and Industrial ±36V
- Commercial ±32V

Short Circuit Duration, Op Amp (Note 2) Continuous

Storage Temperature Range −65°C to +150°C

Maximum Junction Temperature 150°C

Operating Junction Temperature Range T_{Min} to T_{Max}
- LM614M −55°C to +125°C
- LM614I −40°C to +85°C
- LM614C 0°C to +70°C

Soldering Information
- Dual-In-Line Package (Soldering, 10 seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Package Thermal Resistance (Note 3)
- Hermetic DIP J16 100°C/W
- Molded DIP N16 95°C/W
- Molded SO M16 Wide 140°C/W

ESD Tolerance (Note 4)
- 120 pF, 1.5 kΩ ±1 kV
- 200 pF, < 1Ω ±250V

Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, I_R = 100 µA, FEEDBACK pin shorted to GND, any package, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for **T_{Min} to T_{Max}**.

Parameter	Conditions	Typical (Note 5)	LM614M Tested Limit (Note 6)	LM614M Design Limit (Note 7)	LM614AI, LM614I Tested Limit (Note 6)	LM614AI, LM614I Design Limit (Note 7)	LM614C Tested Limit (Note 6)	LM614C Design Limit (Note 7)	Units
Total Supply Current	V^+ Current, $R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ Over T_J Range (Commercial 32V)	450 **550**	900 **1000**		940	**1000**	1000	**1070**	µA max µA max
Supply Voltage Range	Meets Total Supply Current, and See V_R Change with V^+ Change Test	2.2 **2.9**	2.8 **3**		2.8	**3**	2.8	**3**	V min V min
		46 **43**	36 **36**		36	**36**	32	**32**	V max V max
OPERATIONAL AMPLIFIERS									
V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ Commercial)	±1.5 **±2.0**	±3.5 **±5.0**		±3.5	**±6.0**	±5.0	**±7.0**	mV max mV max
V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} = ($V^+ - 1.4V$), V^+ = 30V	±1.0 **±1.5**	±3.5 **±5.0**		±3.5	**±6.0**	±5.0	**±7.0**	mV max mV max
Average V_{OS} Drift	LM614M & AI, Op Amp 3 Only (Note 8)	**15**	**25**		**30**				µV/°C max
Input Bias Current	I_{B+IN} and I_{B-IN}	−10 **−11**	±20 **±25**		±25	**±30**	±35	**±40**	nA max nA max
Input Offset Current	$I_{OS} = I_{B+IN} - I_{B-IN}$	±0.2 **±0.3**	±4 **±4**		±4	**±5**	±4	**±5**	nA max nA max
Average I_{OS} Drift		**±4**							pA/°C

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, any package, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for T_{Min} to T_{Max}.

Parameter	Conditions	Typical (Note 5)	LM614M		LM614AI, LM614I		LM614C		Units
			Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	
Input Resistance	Differential: Common-Mode:	1800 3800							MΩ MΩ
Input Cap.	C-to-GND, Non-Inverting Input of Follower	5.7							pF
Voltage Noise	100 Hz, Input Referred	74							nV/√Hz
Current Noise	100 Hz Bias Current Noise	58							fA/√Hz
Common-Mode Reject Ratio	V^+ = 30V, 0V ≤ V_{CM} ≤ (V^+ − 1.4V), CMRR = 20 log {$\Delta V_{CM}/\Delta V_{OS}$}	95 **90**	85 **80**		80	**75**	75	**70**	dB min dB min
Power Supply Reject Ratio	4V ≤ V^+ ≤ 30V, $V_{CM} = V^+/2$, PSRR = 20 log {$\Delta V^+/\Delta V_{OS}$}	110 **100**	85 **80**		80	**75**	75	**70**	dB min dB min
Voltage Gain, Open Loop	R_L = 10 kΩ to GND, V^+ = 30V, 5V ≤ V_{OUT} ≤ 25V, Open-Loop $A_V = \lvert\Delta V_{OUT}/\Delta V_{INDIFF}\rvert$	500 **50**	100 **40**		100	**40**	94	**40**	V/mV min
Slew Rate	V^+ = 30V (Note 9)	±0.70 **±0.65**	±0.55 **±0.45**		±0.55	**±0.45**	±0.50	**±0.45**	V/μs min
Gain-Bandwidth	Closed Loop Gain = −1000, −3 dB Frequency × Gain, C_L = 50 pF	0.79 **0.52**							MHz
Output Voltage Swing High	R_L = 10 kΩ to GND V^+ = 36V (32V Commercial)	$V^+ - 1.4$ $\mathbf{V^+ - 1.6}$	$V^+ - 1.6$ $\mathbf{V^- - 1.8}$		$V^+ - 1.7$	$\mathbf{V^+ - 1.9}$	$V^+ - 1.8$	$\mathbf{V^+ - 1.9}$	V min V min
Output Voltage Swing Low	R_L = 10 kΩ to V^+ V^+ = 36V (32V Commercial)	$V^- + 0.8$ $\mathbf{V^- + 0.9}$	$V^- + 0.90$ $\mathbf{V^- + 1.0}$		$V^- + 0.90$	$\mathbf{V^- + 1.0}$	$V^- + 0.95$	$\mathbf{V^- + 1.0}$	V max V max
I_{OUT} Source	$V_{OUT} = V^+ - 2.5V$, V_{+IN} = 0V, V_{-IN} = −0.3V	−25 **−15**	−20 **−13**		−20	**−13**	−16	**−13**	mA max mA max

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, any package, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for T_{Min} to T_{Max}.

Parameter	Conditions	Typical (Note 6)	LM614M		LM614AI, LM614I		LM614C		Units
			Tested Limit (Note 7)	Design Limit (Note 8)	Tested Limit (Note 7)	Design Limit (Note 8)	Tested Limit (Note 7)	Design Limit (Note 8)	
I_{OUT} Sink	V_{OUT} = 1.6V, V_{+IN} = 0V, V_{-IN} = 0.3V	17 **9**	15 **8**		14	 **11**	13	 **11**	mA min mA min
Short-Circuit Current	V_{OUT} = 0V, V_{+IN} = 3V, V_{-IN} = 2V, Source:	−30 **−40**	−37 **−46**		−40	 **−48**	−43	 **−50**	mA min mA min
	V_{OUT} = 5V, V_{+IN} = 2V, V_{-IN} = 3V, Sink:	30 **32**	40 **60**		60	 **80**	70	 **90**	mA max mA max
VOLTAGE REFERENCE (Note 10)									
Reference Voltage		1.244	1.2390 1.2490 (±0.4%)		1.2365 1.2515 (±0.6%)		1.2191 1.2689 (±2%)		V min V max
Average Temp. Drift	(Note 11) LM614AI	**10**	**20**		 **20**	**80**		**150**	PPM/C max
Average Time Drift	T_J = 40°C T_J = 150°C	400 1000							PPM/kHr PPM/kHr
Hysteresis	Hyst = (Vro′ − Vro)/ΔT_J (Note 12)	**±3.2**							μV/C
V_R Change with Current	$V_{R[100\ \mu A]} - V_{R[16\ \mu A]}$	0.05 **0.1**	±1 **±1**		±1	 **±1.1**	±1	 **±1.1**	mV max mV max
	$V_{R[10\ mA]} - V_{R[100\ \mu A]}$ (Note 13)	1.5 **3.0**	5 **5**		5	 **5.5**	5	 **5.5**	mV max mV max
Resistance	$\Delta V_{R[10 \rightarrow 0.1\ mA]}$/9.9 mA: $\Delta V_{R[100 \rightarrow 16\ \mu A]}$/84 μA:	0.2 0.6		**0.51** **12**		**0.56** **13**		**0.56** **13**	Ω max Ω max
V_R Change with High V_{RO}	$V_{R[Vro = Vr]} - V_{R[Vro = 6.3V]}$ {5.06V between Anode and FEEDBACK}	2.5 **2.8**	5 **8**		7	 **10**	7	 **10**	mV max mV max
V_R Change with V^+ Change	$V_{R[V^+ = 5V]} - V_{R[V^+ = 36V]}$ (V^+ = 32V Commercial)	0.1 **0.1**	±1.2 **±1.2**		±1.2	 **±1.3**	±1.2	 **±1.3**	mV max mV max
	$V_{R[V^+ = 5V]} - V_{R[V^+ = 3V]}$	0.01 **0.01**	±1 **±1**		±1	 **±1.5**	±1	 **±1.5**	mV max mV max
FEEDBACK Bias Current	I_{FB}; $V_{ANODE} \le V_{FB} \le 5.06V$	−22 **−29**	−35 **−40**		−35	 **−40**	−50	 **−55**	nA min nA min
V_R Noise	10 Hz to 10,000 Hz, $V_{RO} = V_R$	30							μV_{RMS}

Electrical Characteristics Notes

Note 1: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltage on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 2: Simultaneous short-circuit of multiple op amps and reference while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 3: Junction temperature may be calculated using $T_J = T_A + P_D\theta_{JA}$. The given thermal resistances are worst-case for packages in sockets in still air. Nominal θ_{JA} are 85°C/W for LM614 in J package, 80°C/W for the N package, and 110°C/W for the WM package, for packages soldered to copper-clad board with dissipation from one op amp or reference output transistor.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values in standard typeface are for T_J = 25°C; values in **boldface type** apply to the military temperature range. These values represent the most likely parametric norm.

Note 6: Tested limits are guaranteed and 100% tested.

Note 7: Design limits are guaranteed via correlation, but are not 100% tested.

Note 8: Offset voltage drift is calculated from the measurement of the offset voltage at 25°C and at the temperature extremes. The drift is $\Delta V_{OS}/\Delta T$, where ΔV_{OS} is the lowest value subtracted from the highest, and ΔT is the temperature range.

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_{ro} is the Cathode-to-Anode voltage (i.e. the reference output voltage, 1.2V to 6.3V). V_f is the Cathode-to-FEEDBACK voltage (nominally 1.2V).

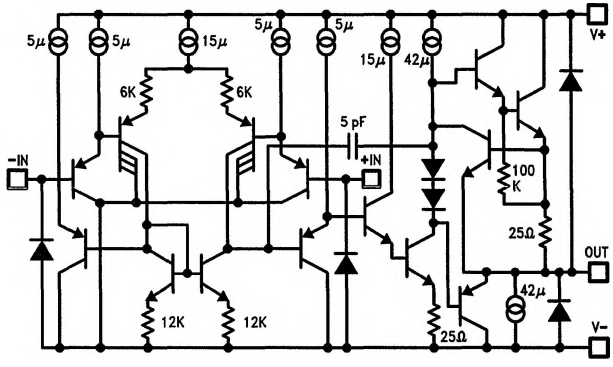
Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \cdot \Delta V_R / V_{R[25°C]} \cdot \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range.

Note 12: Hysteresis is $\Delta V_{RO}/\Delta T_J$, where ΔV_{RO} is the change in V_{RO} caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 125°C, −55°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 13: Low contact resistance is required for accurate measurement.

Simplified Schematic Diagrams

Op Amp



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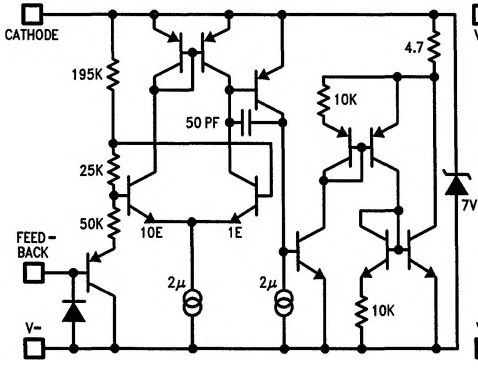
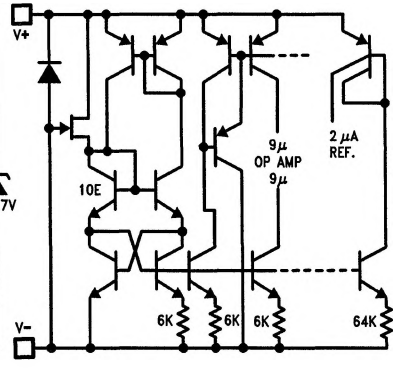
Reference



Bias



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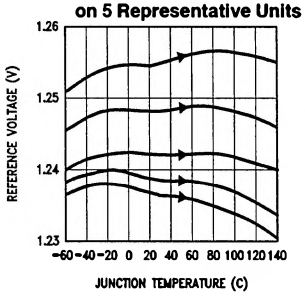
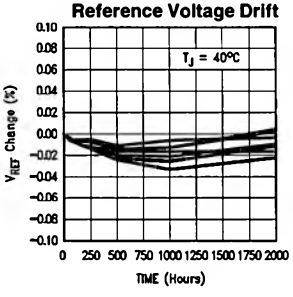
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

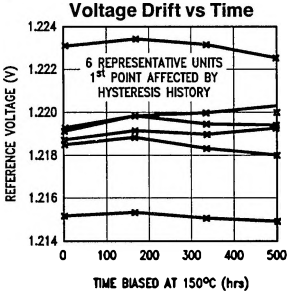
Reference Voltage vs Temperature on 5 Representative Units



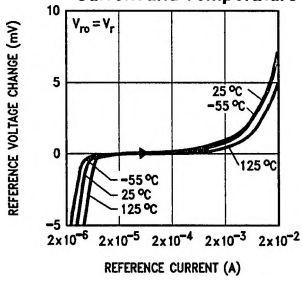
Reference Voltage Drift



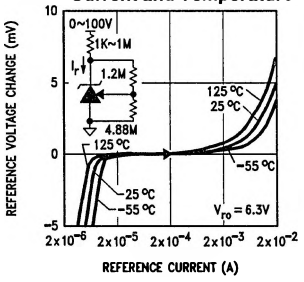
Accelerated Reference Voltage Drift vs Time



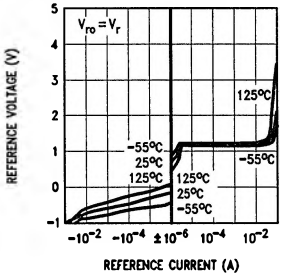
Reference Voltage vs Current and Temperature



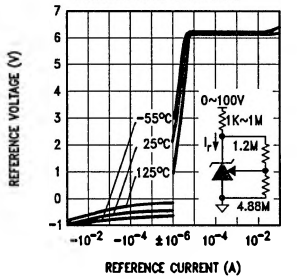
Reference Voltage vs Current and Temperature



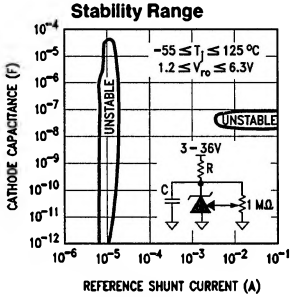
Reference Voltage vs Reference Current



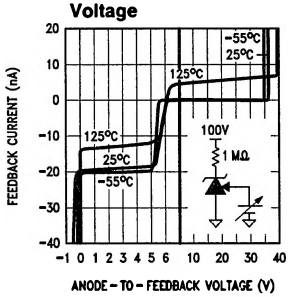
Reference Voltage vs Reference Current



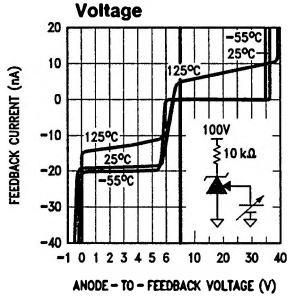
Reference AC Stability Range



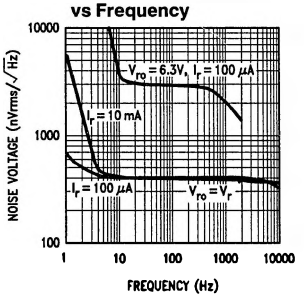
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



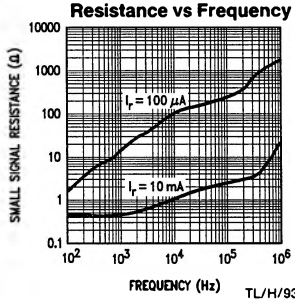
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency



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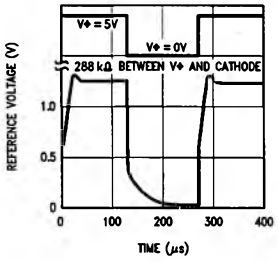
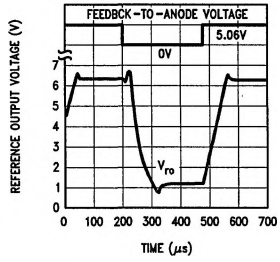
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

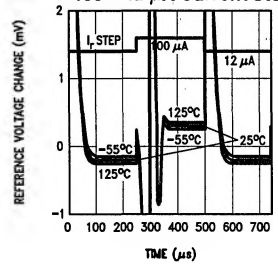
Reference Power-Up Time



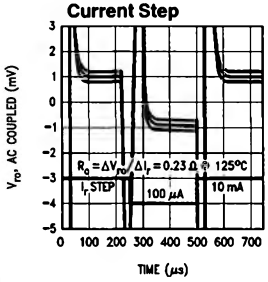
Reference Voltage with FEEDBACK Voltage Step



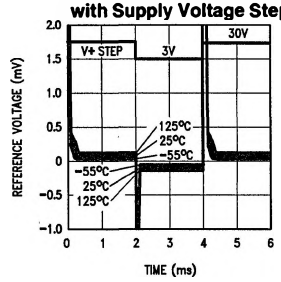
Reference Voltage with 100 ~ 12 μA Current Step



Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



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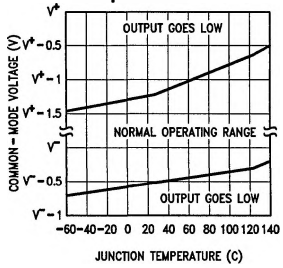
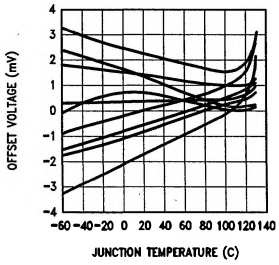
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = OV, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, T_J = 25°C, unless otherwise noted

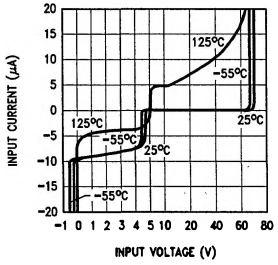
Input Common-Mode Voltage Range vs Temperature



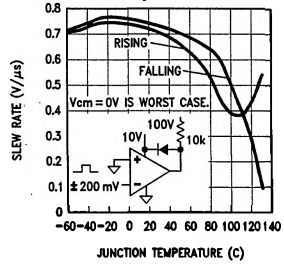
V_{OS} vs Junction Temperature on 9 Representative Units



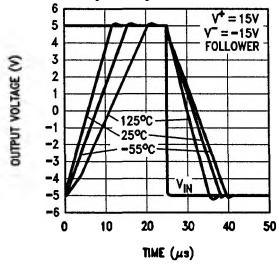
Input Bias Current vs Common-Mode Voltage



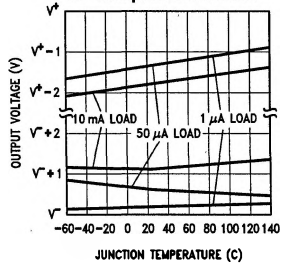
Slew Rate vs Temperature and Output Sink Current



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

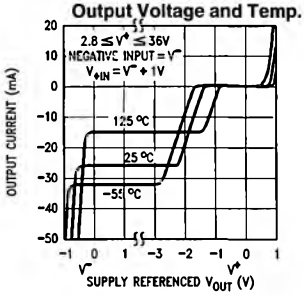


TL/H/9326-5

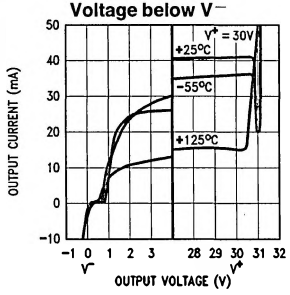
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

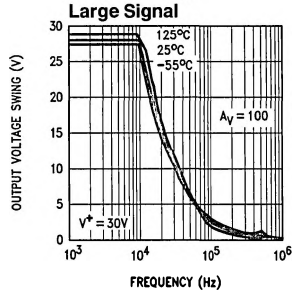
Output Sink Current vs Output Voltage and Temp.



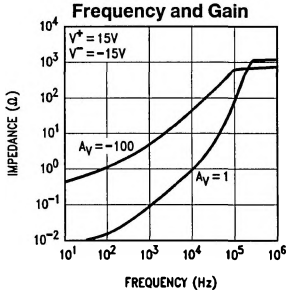
Slew Rate vs. Temp with Common-Mode Voltage below V−



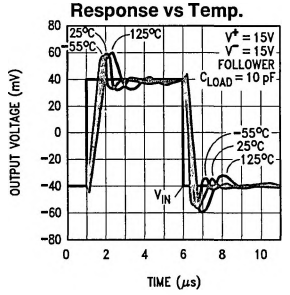
Output Swing, Large Signal



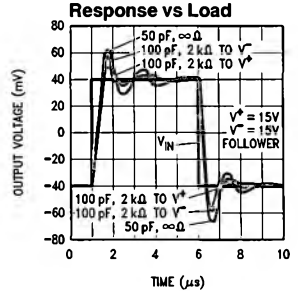
Output Impedance vs Frequency and Gain



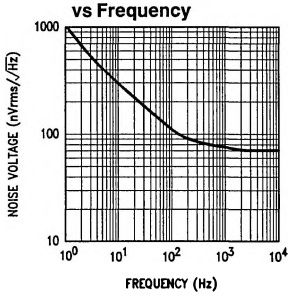
Small-Signal Pulse Response vs Temp.



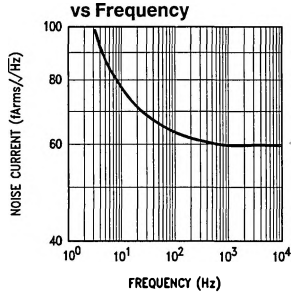
Small-Signal Pulse Response vs Load



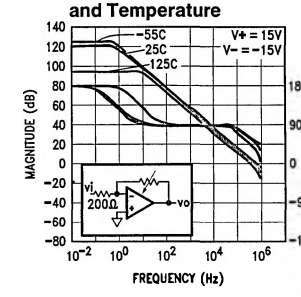
Op Amp Voltage Noise vs Frequency



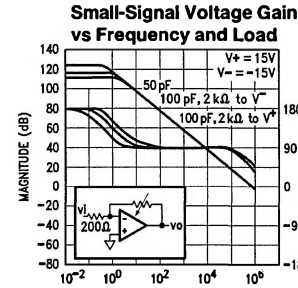
Op Amp Current Noise vs Frequency



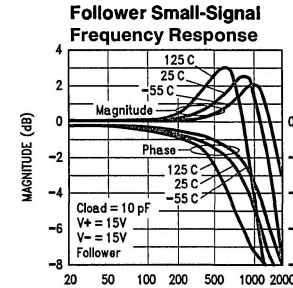
Small-Signal Voltage Gain vs Frequency and Temperature



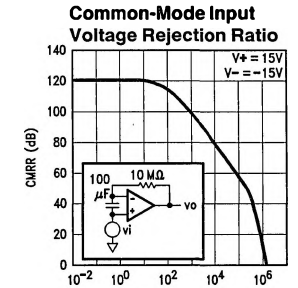
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

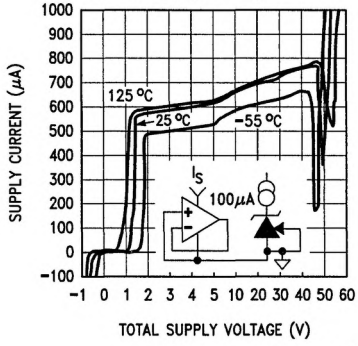


TL/H/9326–6

Typical Performance Characteristics (Op Amps) (Continued)

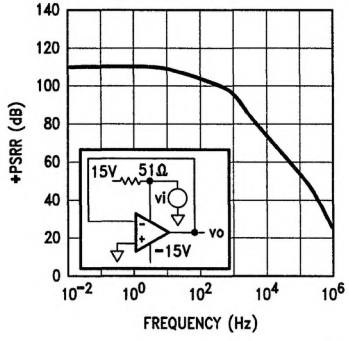
$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

Power Supply Current vs Power Supply Voltage



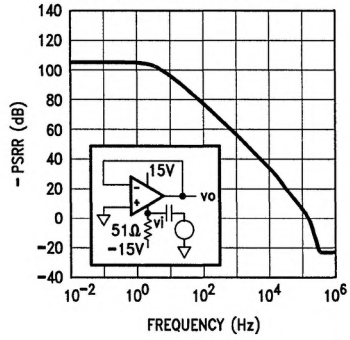
TL/H/9326-7

Positive Power Supply Voltage Rejection Ratio



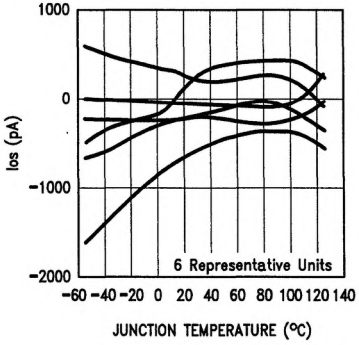
TL/H/9326-21

Negative Power Supply Voltage Rejection Ratio



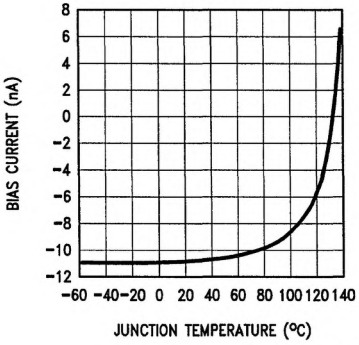
TL/H/9326-22

Input Offset Current vs Junction Temperature



TL/H/9326-24

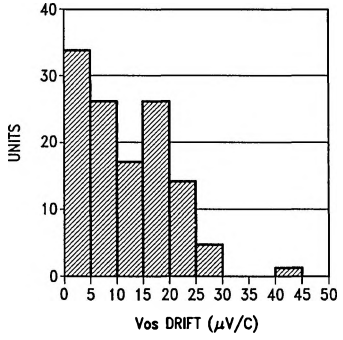
Input Bias Current vs Junction Temperature



TL/H/9326-38

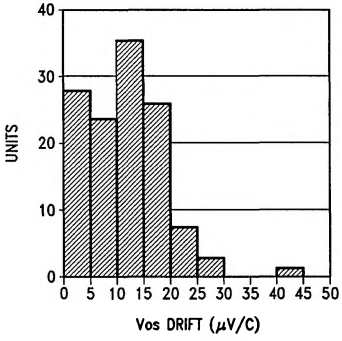
Typical Performance Distributions

Average V_{OS} Drift
Military Temperature Range



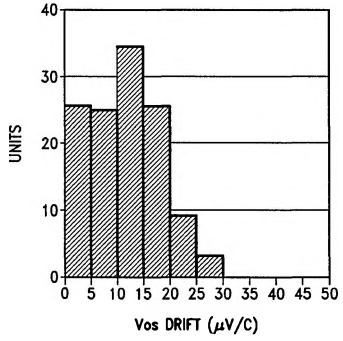
TL/H/9326-29

Average V_{OS} Drift
Industrial Temperature Range



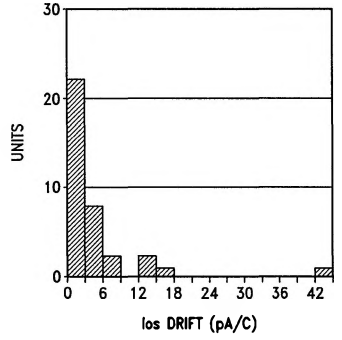
TL/H/9326-30

Average V_{OS} Drift
Commercial Temperature Range



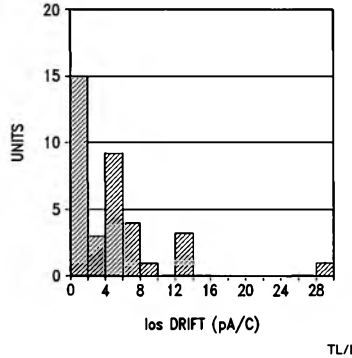
TL/H/9326-31

Average I_{OS} Drift
Military Temperature Range



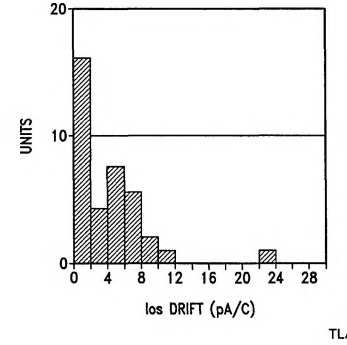
TL/H/9326-32

Average I_{OS} Drift
Industrial Temperature Range



TL/H/9326-33

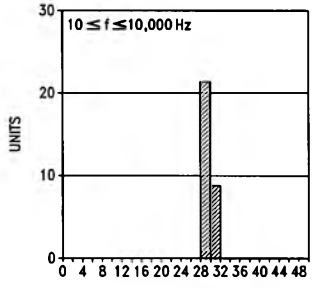
Average I_{OS} Drift
Commercial Temperature Range



TL/H/9326-34

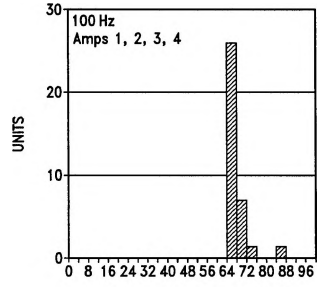
Typical Performance Distributions (Continued)

Voltage Reference Broad-Band Noise Distribution



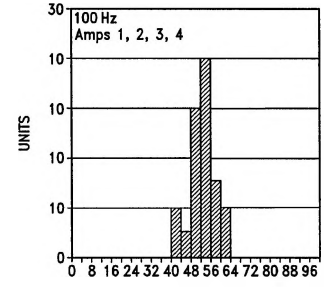
TL/H/9326-35

Op Amp Voltage Noise Distribution



TL/H/9326-36

Op Amp Current Noise Distribution



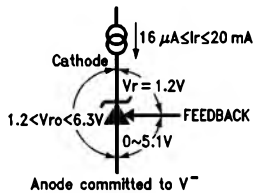
TL/H/9326-37

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with V^+ = 3V is allowed.



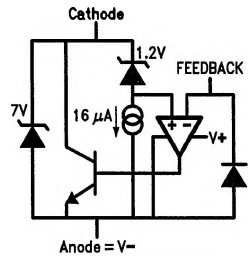
TL/H/9326-9

FIGURE 1. Voltages Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

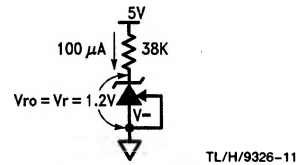
To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.



TL/H/9326-10

FIGURE 2. Reference Equivalent Circuit



TL/H/9326-11

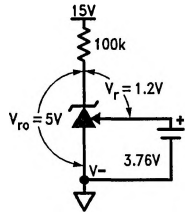
FIGURE 3. 1.2V Reference

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then V_{ro} = V_r = 1.24V. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for V_{ro} = 5V. Connecting a resistor across the constaint V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I

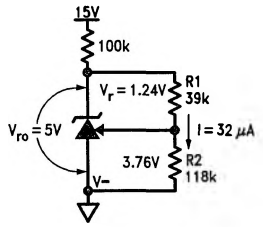
Application Information (Continued)

greater than one thousand times larger than FEEDBACK bias current for <0.1% error—I≥32 μA for the military grade over the military temperature range (I≥5.5 μA for a 1% untrimmed error for a commercial part.)



TL/H/9326–12

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



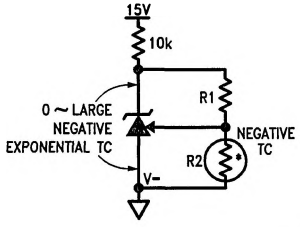
TL/H/9326–13

$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1\{(Vro/Vr) - 1\} = 39k\{(5/1.24) - 1)\} = 118k$$

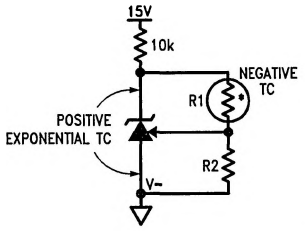
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



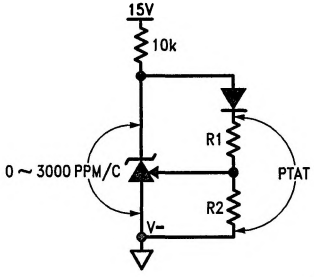
TL/H/9326–14

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



TL/H/9326–15

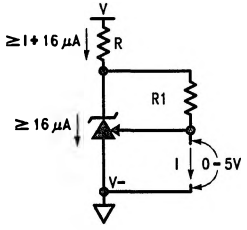
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC



TL/H/9326–16

FIGURE 8. Diode in Series with R1 Causes Voltage across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.

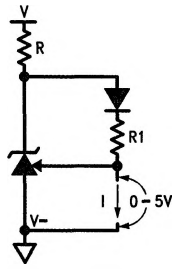


TL/H/9326–17

$$I = Vr/R1 = 1.24/R1$$

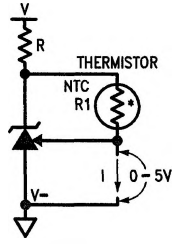
FIGURE 9. Current Source Is Programmed by R1

Application Information (Continued)



TL/H/9326–18

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9326–19

FIGURE 11. Negative-TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS

Any amp or the reference may be biased in any way with no effect on the other amps or reference, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). One amp input may be outside the common-mode range, another amp may be operated as a comparator, another with all terminals floating with no effect on the others (tying inverting input to output and non-inverting input to V^- on unused amps is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

OP Amp Output Stage

These op amps, like their LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain
2) Cross-over Distortion: The LM614 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion
3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

OP Amp Input Stage

The lateral PNP input transistors, unlike most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications

For typical applications, refer to the LM124 Op Amp and LM185 Adjustable Reference datasheets.