LM6142/LM6144 17 MHz Rail-to-Rail Input-Output Operational Amplifiers

Check for Samples: LM6142, LM6144

FEATURES

- **At V_S = 5V. Typ unless noted.**
- **Rail-to-rail input CMVR −0.25V to 5.25V**
- **Rail-to-rail output swing 0.005V to 4.995V**
- **Wide gain-bandwidth: 17MHz at 50kHz (typ)**
- **Slew rate:**
  - **Small signal, 5V/µs**
  - **Large signal, 30V/µs**
- **Low supply current 650µA/Amplifier**
- **Wide supply range 1.8V to 24V**
- **CMRR 107dB**
- **Gain 108dB with R_L = 10k**
- **PSRR 87dB**

APPLICATIONS

- **Battery operated instrumentation**
- **Depth sounders/fish finders**
- **Barcode scanners**
- **Wireless communications**
- **Rail-to-rail in-out instrumentation amps**

DESCRIPTION

Using patent pending new circuit topologies, the LM6142/LM6144 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of 1.8V to over 24V, the LM6142/LM6144 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with 650µA/Amplifier supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.

Connection Diagrams

8-Pin CDIP

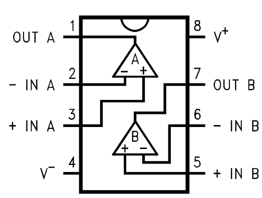


Figure 1. Top View

8-Pin DIP/SO

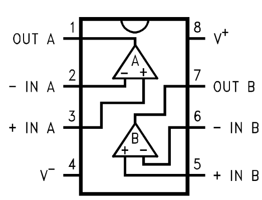


Figure 2. Top View

14-Pin DIP/SO

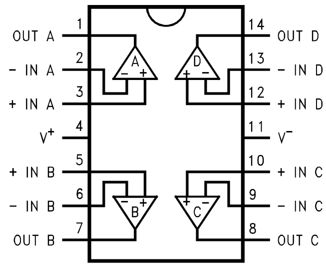


Figure 3. Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	35V
Current at Input Pin	±10mA
Current at Output Pin (3)	±25mA
Current at Power Supply Pin	50mA
Lead Temperature	
(soldering, 10 sec)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (4)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Charactenstics.
(2) Human body model, 1.5kΩ in series with 100pF.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings (1)

Supply Voltage	$1.8V \le V^+ \le 24V$
Temperature Range	
LM6142, LM6144	$-40°C \le T_A \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
N Package, 14-Pin Molded DIP	81°C/W
M Package, 14-Pin Surface Mount	126°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Charactenstics.

5.0V DC Electrical Characteristics [1]

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (2)	LM6144AI LM6142AI Limit (3)	LM6144BI LM6142BI Limit (3)	Units
V_{OS}	Input Offset Voltage		0.3	1.0	2.5	mV
				2.2	**3.3**	max
TCV_{OS}	Input Offset Voltage		**3**			μV/°C
	Average Drift					
I_B	Input Bias Current		170	250	300	nA max
		0V ≤ V_{CM} ≤ 5V	180	280		
				526	**526**	
I_{OS}	Input Offset Current		3	30	30	nA
				80	**80**	max
R_{IN}	Input Resistance, C_M		126			MΩ
CMRR	Common Mode	0V ≤ V_{CM} ≤ 4V	107	84	84	dB min
	Rejection Ratio			**78**	**78**	
		0V ≤ V_{CM} ≤ 5V	82	66	66	
			79	**64**	**64**	
PSRR	Power Supply	5V ≤ V^+ ≤ 24V	**87**	80	80	
	Rejection Ratio			**78**	**78**	
V_{CM}	Input Common-Mode		−0.25	**0**	**0**	V
	Voltage Range		5.25	**5.0**	**5.0**	
A_V	Large Signal	R_L = 10k	270	100	80	V/mV
	Voltage Gain		**70**	**33**	**25**	min
V_O	Output Swing	R_L = 100k	0.005	0.01	0.01	V
				0.013	**0.013**	max
			4.995	4.98	4.98	V
				4.93	**4.93**	min
		R_L = 10k	0.02			V max
			4.97			V min
		R_L = 2k	0.06	0.1	0.1	V
				0.133	**0.133**	max
			4.90	4.86	4.86	V
				4.80	**4.80**	min
I_{SC}	Output Short	Sourcing	13	10	8	mA
	Circuit Current			**4.9**	**4**	min
	LM6142			**35**	**35**	mA
						max
		Sinking	24	10	10	mA
				5.3	**5.3**	min
				35	**35**	mA
						max
I_{SC}	Output Short	Sourcing	8	6	6	mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where $T_J > T_A$.
(2) Typical values represent the most likely parametric norm.
(3) All limits are guaranteed by testing or statistical analysis.

5.0V DC Electrical Characteristics [1] (continued)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ [2]	LM6144AI LM6142AI Limit [3]	LM6144BI LM6142BI Limit [3]	Units
	Circuit Current			**3**	**3**	min
	LM6144			**35**	**35**	mA
						max
		Sinking	22	8	8	mA
				4	**4**	min
				35	**35**	mA
						max
I_S	Supply Current	Per Amplifier	650	800	800	μA
				880	**880**	max

5.0V AC Electrical Characteristics [(1)]

Unless Otherwise Specified, All Limits Guaranteed for T_A = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2. **Boldface limits** apply at the temperature extremes.

				LM6144AI	LM6144BI	
Symbol	**Parameter**	**Conditions**	**Typ**	**LM6142AI**	**LM6142BI**	**Units**
			(2)	**Limit**	**Limit**	
				(3)	(3)	
SR	Slew Rate	8 V_{PP} @ V^+ 12V	25	15	13	V/µs
		R_S > 1 kΩ		**13**	**11**	min
GBW	Gain-Bandwidth Product	f = 50 kHz	17	10	10	MHz
				6	**6**	min
$φ_m$	Phase Margin		38			Deg
	Amp-to-Amp Isolation		130			dB
e_n	Input-Referred	f = 1 kHz	16			$\frac{nV}{\sqrt{Hz}}$ (1)
	Voltage Noise					
i_n	Input-Referred	f = 1 kHz	0.22			$\frac{pA}{\sqrt{Hz}}$ (2)
	Current Noise					
T.H.D.	Total Harmonic Distortion	f = 10 kHz, R_L = 10 kΩ,	0.003			%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where T_J > T_A.
(2) Typical values represent the most likely parametric norm.
(3) All limits are guaranteed by testing or statistical analysis.

2.7V DC Electrical Characteristics [1]

Unless Otherwise Specified, All Limits Guaranteed for T_A = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ [2]	LM6144AI LM6142AI Limit [3]	LM6144BI LM6142BI Limit [3]	Units
V_{OS}	Input Offset Voltage		0.4	1.8	2.5	mV
				4.3	**5**	max
I_B	Input Bias Current		150	250	300	nA
				526	**526**	max
I_{OS}	Input Offset Current		4	30	30	nA
				80	**80**	max
R_{IN}	Input Resistance		128			MΩ
CMRR	Common Mode	0V ≤ V_{CM} ≤ 1.8V	90			dB min
	Rejection Ratio	0V ≤ V_{CM} ≤ 2.7V	76			
PSRR	Power Supply	3V ≤ V+ ≤ 5V	79			
	Rejection Ratio					
V_{CM}	Input Common-Mode		−0.25	0	0	V min
	Voltage Range		2.95	2.7	2.7	V max
A_V	Large Signal	R_L = 10k	55			V/mV
	Voltage Gain					min
V_O	Output Swing	R_L = 100kΩ	0.019	0.08	0.08	V
				0.112	**0.112**	max
			2.67	2.66	2.66	V
				2.25	**2.25**	min
I_S	Supply Current	Per Amplifier	510	800	800	μA
				880	**880**	max

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where T_J > T_A.
(2) Typical values represent the most likely parametric norm.
(3) All limits are guaranteed by testing or statistical analysis.

2.7V AC Electrical Characteristics [1]

Unless Otherwise Specified, All Limits Guaranteed for T_A = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$.
Boldface limits apply at the temperature extreme

				LM6144AI	LM6144BI	
Symbol	**Parameter**	**Conditions**	**Typ**	**LM6142AI**	**LM6142BI**	**Units**
			(2)	**Limit**	**Limit**	
				(3)	(3)	
GBW	Gain-Bandwidth Product	f = 50 kHz	9			MHz
φ_m	Phase Margin		36			Deg
G_m	Gain Margin		6			dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where $T_J > T_A$.
(2) Typical values represent the most likely parametric norm.
(3) All limits are guaranteed by testing or statistical analysis.

24V Electrical Characteristics (1)

Unless Otherwise Specified, All Limits Guaranteed for T_A = 25°C, V^+ = 24V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2. **Boldface** limits apply at the temperature extreme

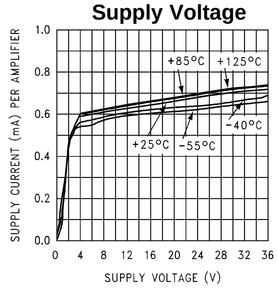
Symbol	Parameter	Conditions	Typ (2)	LM6144AI LM6142AI Limit (3)	LM6144BI LM6142BI Limit (3)	Units
V_{OS}	Input Offset Voltage		1.3	2	3.8	mV
				4.8	**4.8**	max
I_B	Input Bias Current		174			nA
						max
I_{OS}	Input Offset Current		5			nA
						max
R_{IN}	Input Resistance		288			MΩ
CMRR	Common Mode	0V ≤ V_{CM} ≤ 23V	114			dB min
	Rejection Ratio	0V ≤ V_{CM} ≤ 24V	100			
PSRR	Power Supply	0V ≤ V_{CM} ≤ 24V	87			
	Rejection Ratio					
V_{CM}	Input Common-Mode		−0.25	0	0	V min
	Voltage Range		24.25	24	24	V max
A_V	Large Signal	R_L = 10k	500			V/mV
	Voltage Gain					min
V_O	Output Swing	R_L = 10 kΩ	0.07	0.15	0.15	V
				0.185	**0.185**	max
			23.85	23.81	23.81	V
				23.62	**23.62**	min
I_S	Supply Current	Per Amplifier	750	1100	1100	μA
				1150	**1150**	max
GBW	Gain-Bandwidth Product	f = 50 kHz	18			MHz

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of the internal self heating where T_J > T_A.
(2) Typical values represent the most likely parametric norm.
(3) All limits are guaranteed by testing or statistical analysis.

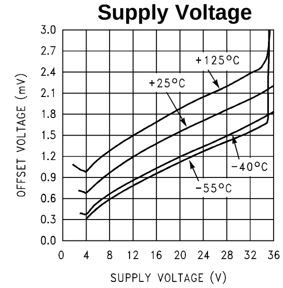
Typical Performance Characteristics

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified

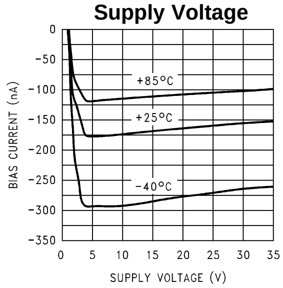
Supply Current vs. Supply Voltage



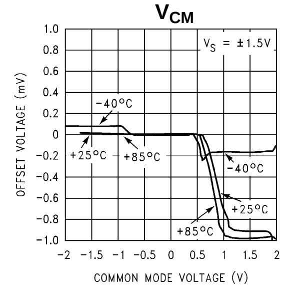
Offset Voltage vs. Supply Voltage



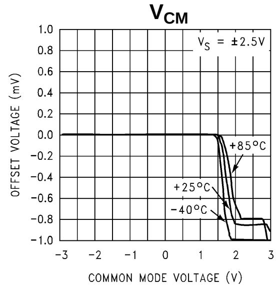
Bias Current vs. Supply Voltage



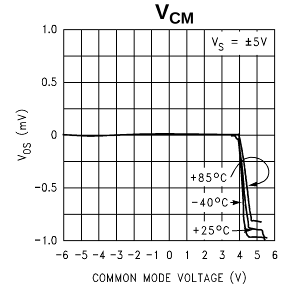
Offset Voltage vs. V_{CM}



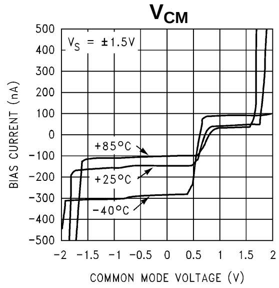
Offset Voltage vs. V_{CM}



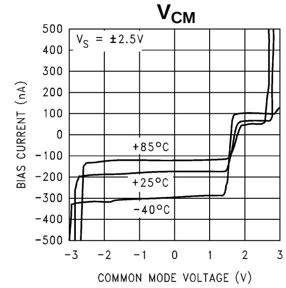
Offset Voltage vs. V_{CM}



Bias Current vs. V_{CM}



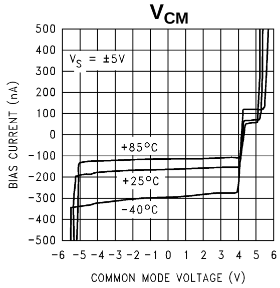
Bias Current vs. V_{CM}



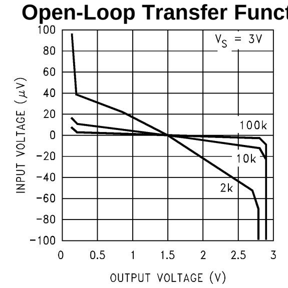
Typical Performance Characteristics (continued)

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified

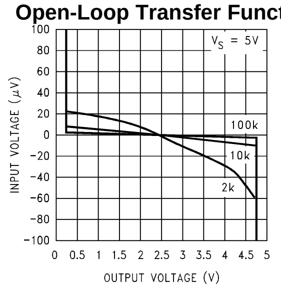
Bias Current vs. V_{CM}



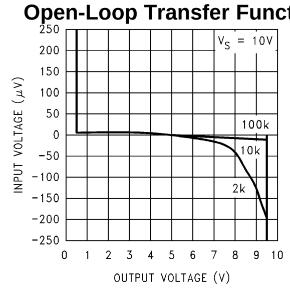
Open-Loop Transfer Function



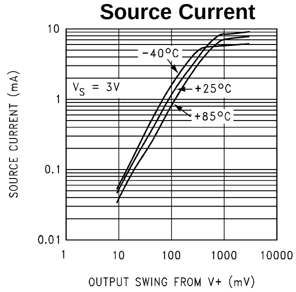
Open-Loop Transfer Function



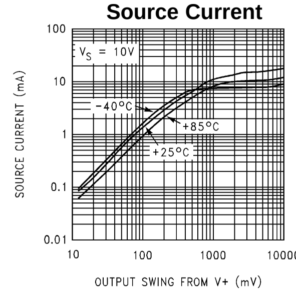
Open-Loop Transfer Function



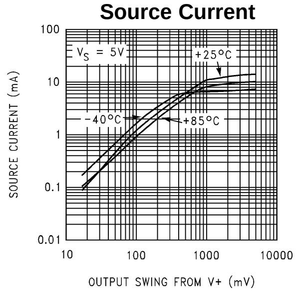
Output Voltage vs. Source Current



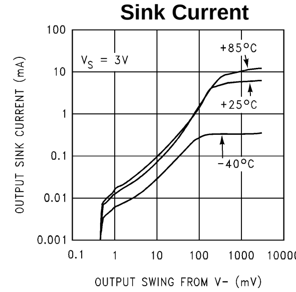
Output Voltage vs. Source Current



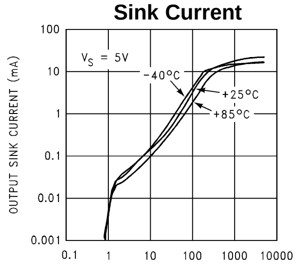
Output Voltage vs. Source Current



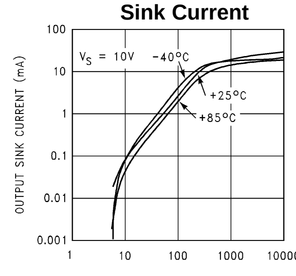
Output Voltage vs. Sink Current



Output Voltage vs. Sink Current



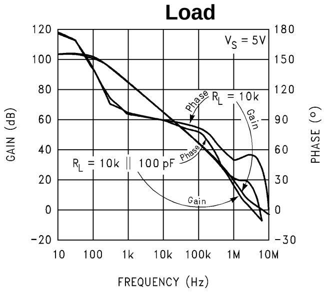
Output Voltage vs. Sink Current



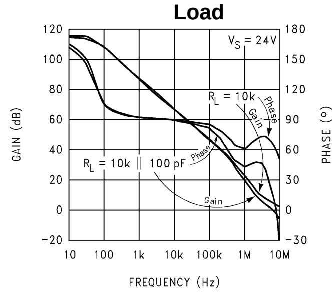
Typical Performance Characteristics (continued)

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified

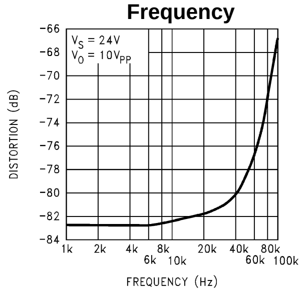
Gain and Phase vs. Load



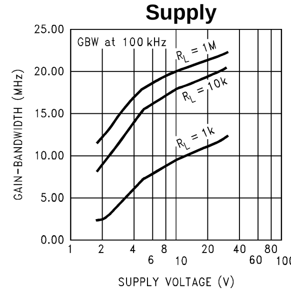
Gain and Phase vs. Load



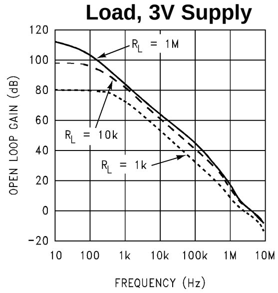
Distortion + Noise vs. Frequency



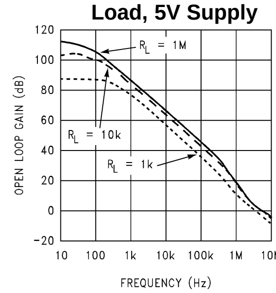
GBW vs. Supply



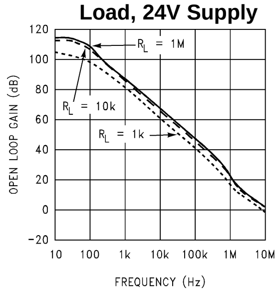
Open Loop Gain vs. Load, 3V Supply



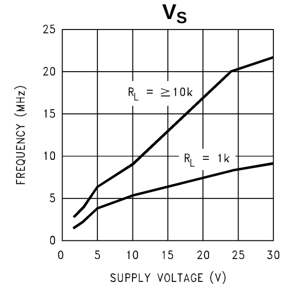
Open Loop Gain vs. Load, 5V Supply



Open Loop Gain vs. Load, 24V Supply



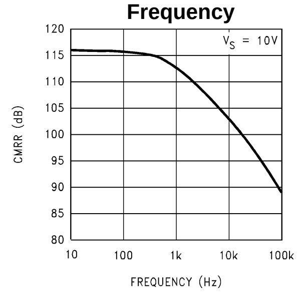
Unity Gain Frequency vs. V_S



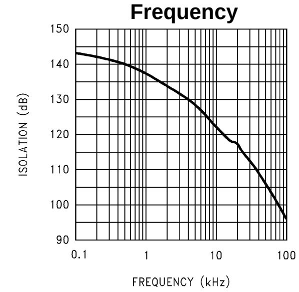
Typical Performance Characteristics (continued)

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified

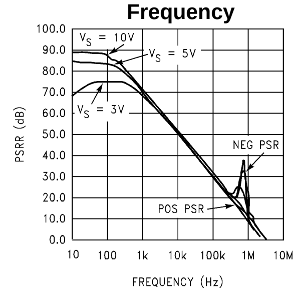
CMRR vs. Frequency



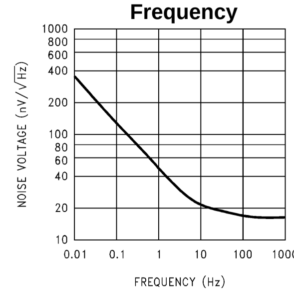
Crosstalk vs. Frequency



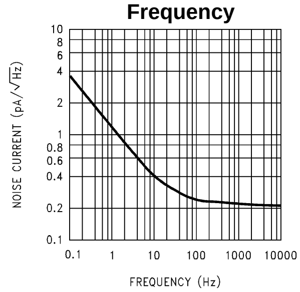
PSRR vs. Frequency



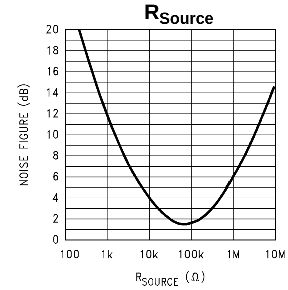
Noise Voltage vs. Frequency



Noise Current vs. Frequency



NF vs. R_{Source}



LM6142/LM6144 Application Ideas

The LM6142 brings a new level of ease of use to op amp system design.

With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption, previously reduced battery life to unacceptable levels.

To take advantage of these features, some ideas should be kept in mind.

ENHANCED SLEW RATE

Unlike most bipolar op amps, the unique phase reversal prevention/speed-up circuit in the input stage causes the slew rate to be very much a function of the input signal amplitude.

Figure 6 shows how excess input signal, is routed around the input collector-base junctions, directly to the current mirrors.

The LM6142/LM6144 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1–Q2, Q3–Q4 when the input levels are normal.

If the input signal exceeds the slew rate of the input stage, the differential input voltage rises above two diode drops. This excess signal bypasses the normal input transistors, (Q1–Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.

This rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See Figure 5.)

As the overdrive increases, the op amp reacts better than a conventional op amp. Large fast pulses will raise the slew- rate to around 30V to 60V/µs.

Figure 4. Slew Rate vs. Δ V_{IN}
V_S = ±5V

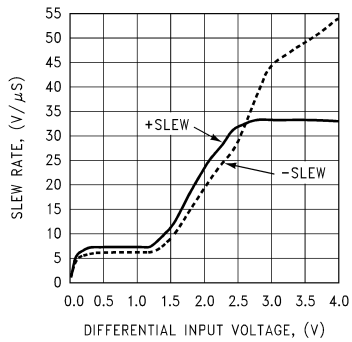


Figure 5.

This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large.

This new input circuit also eliminates the phase reversal seen in many op amps when they are overdriven.

This speed-up action adds stability to the system when driving large capacitive loads.

DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all op amps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most op amps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6142, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.

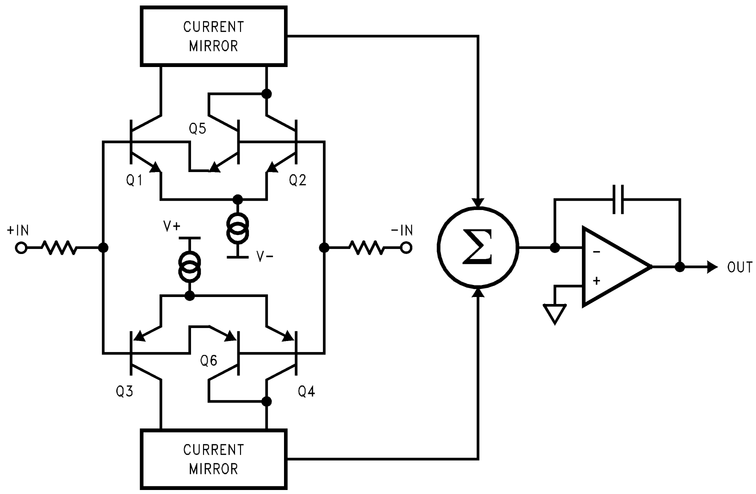


Figure 6.

These features allow the LM6142 to drive capacitive loads as large as 1000pF at unity gain and not oscillate. The scope photos (Figure 7 and Figure 8) above show the LM6142 driving a l000pF load. In Figure 7, the upper trace is with no capacitive load and the lower trace is with a 1000pF load. Here we are operating on ±12V supplies with a 20 V_{PP} pulse. Excellent response is obtained with a C_f of l0pF. In Figure 8, the supplies have been reduced to ±2.5V, the pulse is 4 V_{PP} and C_f is 39pF. The best value for the compensation capacitor is best established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.

Another effect that is common to all op amps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.

The circuit shown in Figure 9 was used for these scope photos.

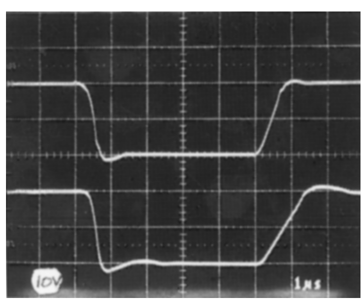


Figure 7.

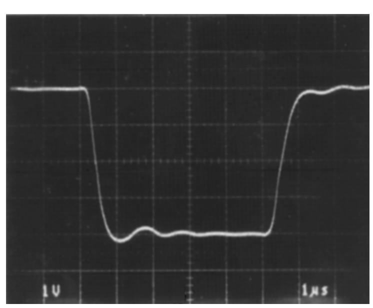


Figure 8.

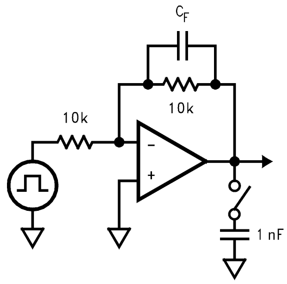


Figure 9.

Typical Applications

FISH FINDER/ DEPTH SOUNDER.

The LM6142/LM6144 is an excellent choice for battery operated fish finders. The low supply current, high gain-bandwidth and full rail to rail output swing of the LM6142 provides an ideal combination for use in this and similar applications.

ANALOG TO DIGITAL CONVERTER BUFFER

The high capacitive load driving ability, rail-to-rail input and output range with the excellent CMR of 82 dB, make the LM6142/LM6144 a good choice for buffering the inputs of A to D converters.

3 OP AMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using the LM6144, a 3 op amp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6144, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage (Figure 10). These buffers assure that the input impedance is over 100MΩ and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.

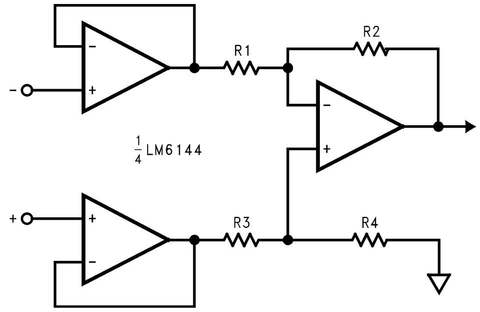


Figure 10.

The gain is set by the ratio of R2/R1 and R3 should equal R1 and R4 equal R2. Making R4 slightly smaller than R2 and adding a trim pot equal to twice the difference between R2 and R4 will allow the CMR to be adjusted for optimum.

With both rail to rail input and output ranges, the inputs and outputs are only limited by the supply voltages. Remember that even with rail-to-rail output, the output can not swing past the supplies so the combined common mode voltage plus the signal should not be greater than the supplies or limiting will occur.

SPICE MACROMODEL

A SPICE macromodel of this and many other National Semiconductor op amps is available at no charge from the NSC Customer Response Group at 800-272-9959.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM6142AIM	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM614 2AIM	Samples
LM6142AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM614 2AIM	Samples
LM6142AIMX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM614 2AIM	Samples
LM6142AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM614 2AIM	Samples
LM6142BIM	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM614 2BIM	Samples
LM6142BIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM614 2BIM	Samples
LM6142BIMX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM614 2BIM	Samples
LM6142BIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM614 2BIM	Samples
LM6142BIN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM6142 BIN	Samples
LM6144AIM	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM6144 AIM	Samples
LM6144AIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM6144 AIM	Samples
LM6144AIMX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM6144 AIM	Samples
LM6144AIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM6144 AIM	Samples
LM6144BIM	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM6144 BIM	Samples
LM6144BIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM6144 BIM	Samples
LM6144BIMX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM6144 BIM	Samples
LM6144BIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM6144 BIM	Samples

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM6144BIN	ACTIVE	PDIP	NFF	14	25	TBD	SNPB	Level-1-NA-UNLIM	-40 to 85	LM6144BIN	Samples
LM6144BIN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LM6144BIN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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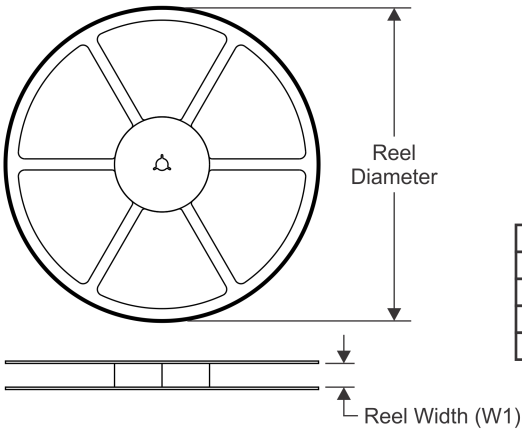
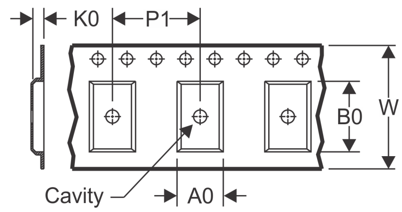
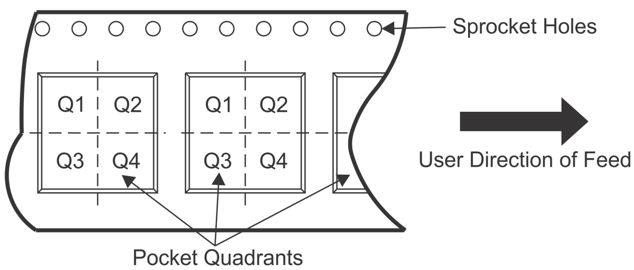


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

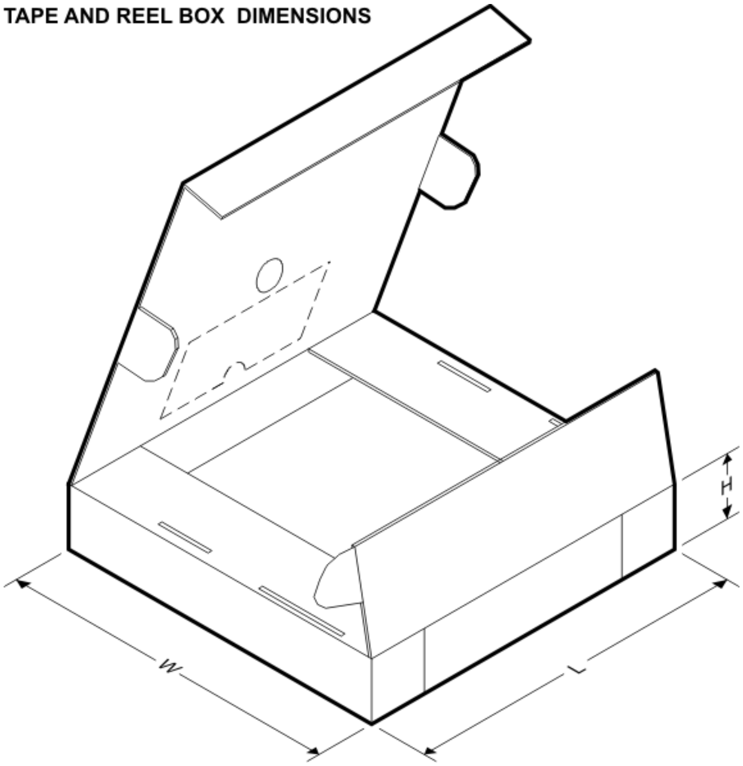
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6142AIMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6142AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6142BIMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6142BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6144AIMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM6144AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM6144BIMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM6144BIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

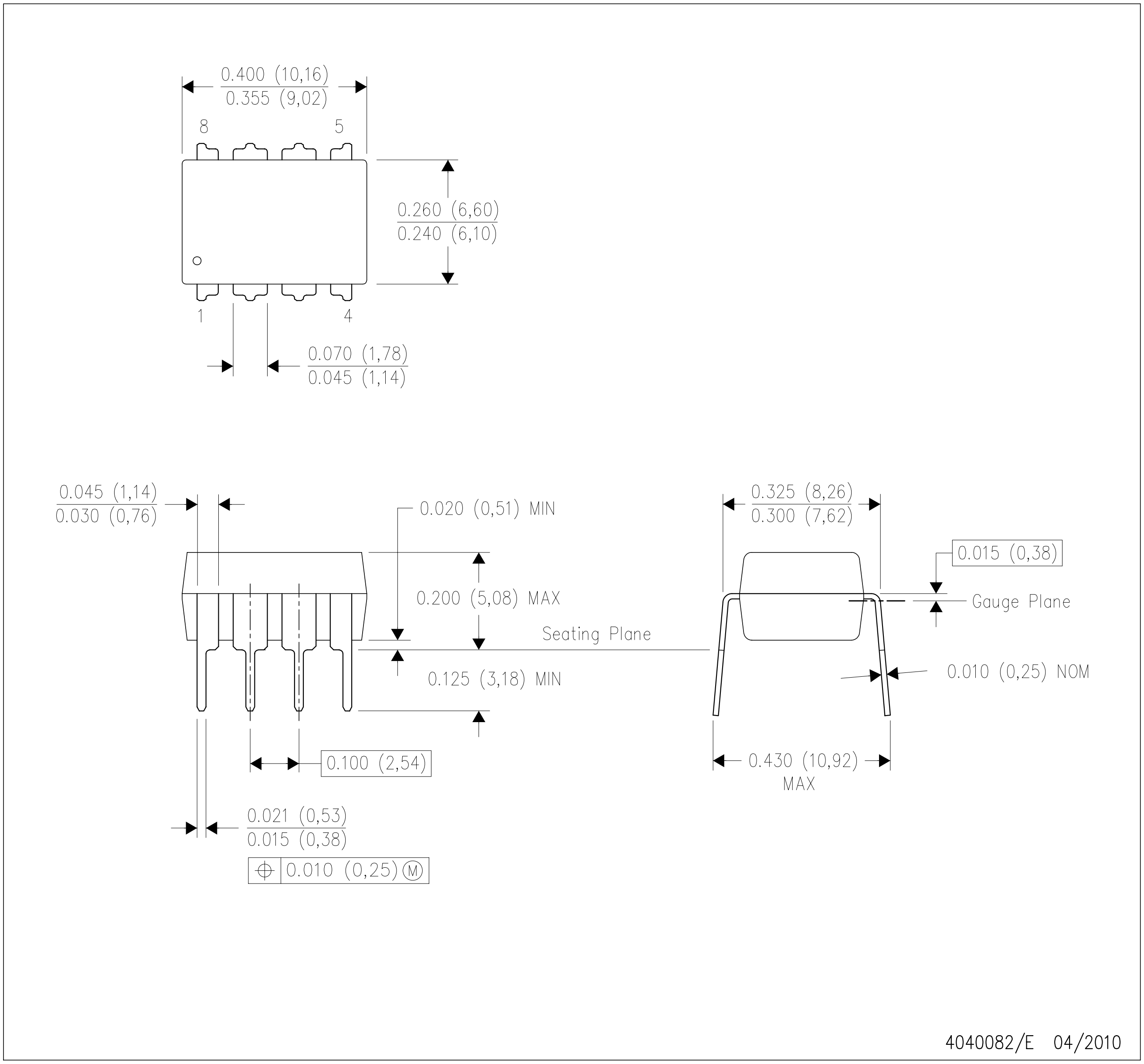
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6142AIMX	SOIC	D	8	2500	349.0	337.0	45.0
LM6142AIMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM6142BIMX	SOIC	D	8	2500	349.0	337.0	45.0
LM6142BIMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM6144AIMX	SOIC	D	14	2500	349.0	337.0	45.0
LM6144AIMX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0
LM6144BIMX	SOIC	D	14	2500	349.0	337.0	45.0
LM6144BIMX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
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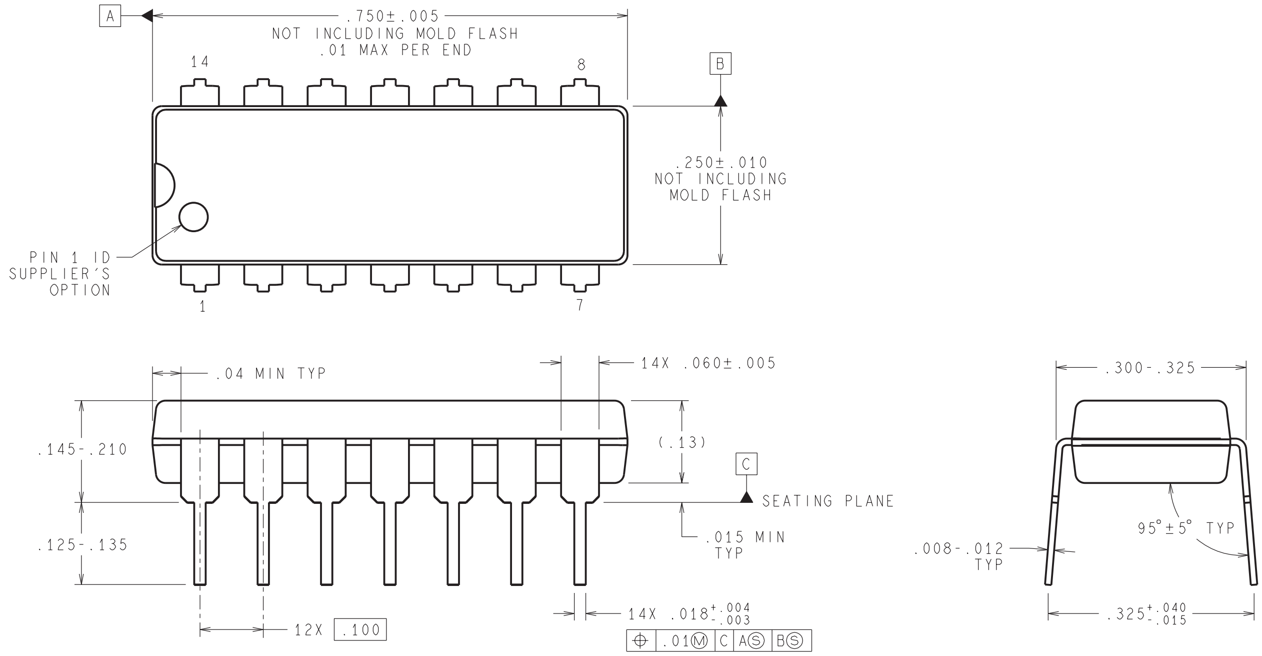
NFF0014A



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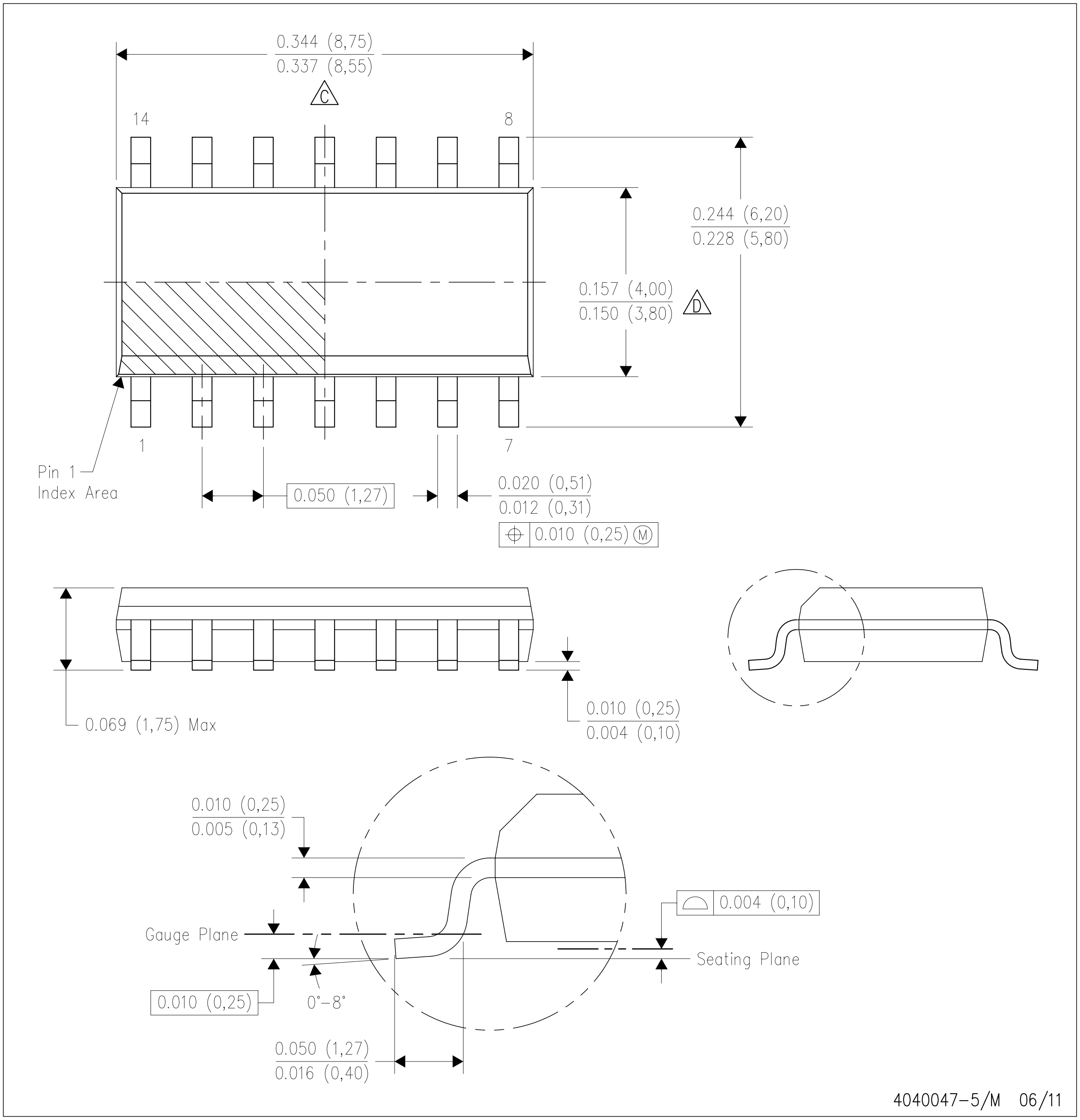
N14A (Rev G)

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



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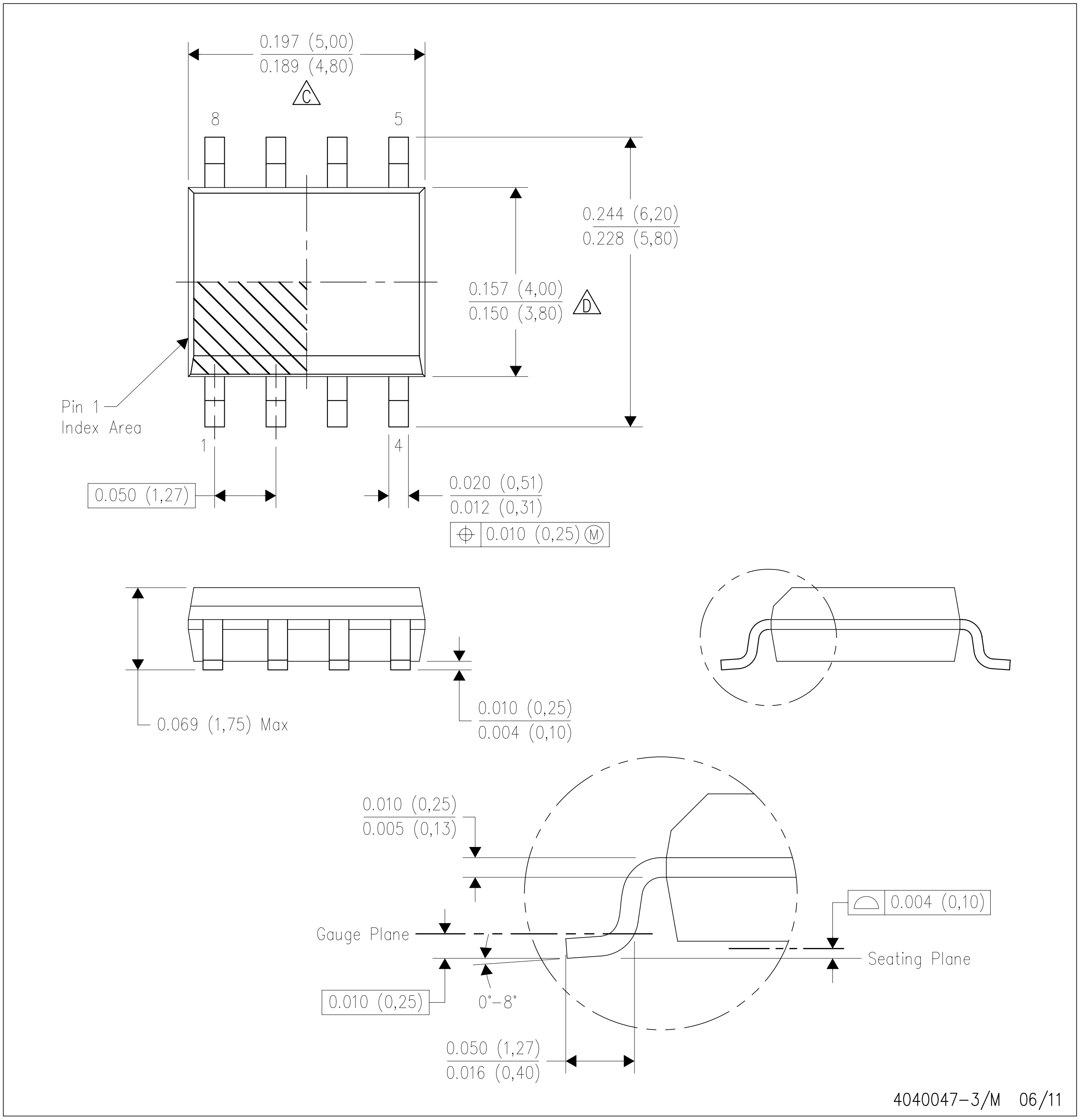
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
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- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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