LM6152/LM6154 Dual and Quad 75 MHz GBW Rail-to-Rail I/O Operational Amplifiers

Check for Samples: LM6152, LM6154

FEATURES

- At V_S = 5V, typical unless noted.
- Greater than rail-to-rail input CMVR −0.25V to 5.25V
- Rail-to-rail output swing 0.01V to 4.99V
- Wide gain-bandwidth 75 MHz @ 100 kHz
- Slew rate
- Small signal 5 V/μs
- Large signal 45 V/μs
- Low supply current 1.4 mA/amplifier
- Wide supply range 2.7V to 24V
- Fast settling time of 1.1 μs for 2V step (to 0.01%)
- PSRR 91 dB
- CMRR 84 dB

APPLICATIONS

- Portable high speed instrumentation
- Signal conditioning amplifier/ADC buffers
- Barcode scanners

DESCRIPTION

Using patented circuit topologies, the LM6152/LM6154 provides new levels of speed vs. power performance in applications where low voltage supplies or power limitations previously made compromise necessary. With only 1.4 mA/amplifier supply current, the 75 MHz gain bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life. The slew rate of the devices increases with increasing input differential voltage, thus allowing the device to handle capacitive loads while maintaining large signal amplitude.

The LM6152/LM6154 can be driven by voltages that exceed both power supply rails, thus eliminating concerns about exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

Operating on supplies from 2.7V to over 24V, the LM6152/LM6154 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

Connection Diagram

8-Pin SOIC

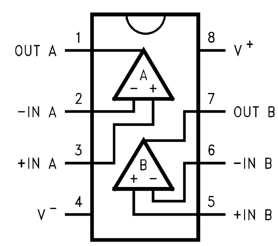


Figure 1. Top View

14-Pin SOIC

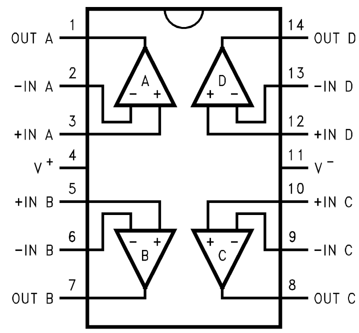


Figure 2. Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [(1)]

ESD Tolerance [(2)]	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) -0.3V$
Supply Voltage ($V^+ - V^-$)	35V
Current at Input Pin	±10 mA
Current at Output Pin [(3)]	±25 mA
Current at Power Supply Pin	50 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature [(4)]	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Human body model is 1.5 kΩ in series with 100 pF.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}–T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings [(1)]

Supply Voltage	$2.7V \leq V^+ \leq 24V$
Junction Temperature Range	
LM6152,LM6154	$0°C \leq T_J \leq +70°C$
Thermal Resistance (θ_{JA})	
8-pin SOIC	193°C/W
14-pin SOIC	126°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LM6154AC LM6152AC Limit (2)	LM6154BC LM6152BC Limt (2)	Units
V_{OS}	Input Offset Voltage		0.54	2 **4**	5 **7**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**10**			μV/°C
I_B	Input Bias Current	0V ≤ V_{CM} ≤ 5V	500 **750**	980 **1500**	980 **1500**	nA max
I_{OS}	Input Offset Current		32 **40**	100 **160**	100 **160**	nA max
R_{IN}	Input Resistance, CM	0V ≤ V_{CM} ≤ 4V	30			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4V	94	70	70	dB min
		0V ≤ V_{CM} ≤ 5V	84	60	60	
PSRR	Power Supply Rejection Ratio	5V ≤ V^+ ≤ 24V	91	80	80	dB min
V_{CM}	Input Common-Mode Voltage Range	Low	−0.25	0	0	V
		High	5.25	**5.0**	**5.0**	V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ	214	50	50	V/mV min
V_O	Output Swing	R_L = 100 kΩ	0.006	0.02 **0.03**	0.02 **0.03**	V max
			4.992	4.97 **4.96**	4.97 **4.96**	V min
		R_L = 2 kΩ	0.04	0.10 **0.12**	0.10 **0.12**	V max
			4.89	4.80 **4.70**	4.80 **4.70**	V min
I_{SC}	Output Short Circuit Current	Sourcing	6.2	3 **2.5**	3 **2.5**	mA min
				27 **17**	27 **17**	mA max
		Sinking	16.9	7 **5**	7 **5**	mA min
				40	40	mA max
I_S	Supply Current	Per Amplifier	1.4	2 **2.25**	2 **2.25**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

5.0V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LM6154AC LM6152AC Limit (2)	LM6154BC LM6152BC Limt (2)	Units
SR	Slew Rate	±4V Step @ V_S = ±6V, R_S < 1 kΩ	30	24 **15**	24 **15**	V/µs min
GBW	Gain-Bandwidth Product	f = 100 kHz	75			MHz
	Amp-to-Amp Isolation	R_L = 10 kΩ	125			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	9			$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.34			$pA/\sqrt{Hz}$
T.H.D	Total Harmonic Distortion	f = 100 kHz, R_L = 10 kΩ A_V = −1, V_O = 2.5 V_{PP}	−65			dBc
ts	Settling Time	2V Step to 0.01%	1.1			µs

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LM6154AC LM6152AC Limit (2)	LM6154BC LM6152BC Limt (2)	Units
V_{OS}	Input Offset Voltage		0.8	2 **5**	5 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**10**			μV/°C
I_B	Input Bias Current		500			nA
I_{OS}	Input Offset Current		50			nA
R_{IN}	Input Resistance, CM	0V ≤ V_{CM} ≤ 1.8V	30			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.8V	88			dB
		0V ≤ V_{CM} ≤ 2.7V	78			
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 5V	69			dB
V_{CM}	Input Common-Mode Voltage Range	Low	−0.25	0	0	V
		High	2.95	2.7	2.7	V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ	5.5			V/mV
V_O	Output Swing	R_L = 10 kΩ	0.032	0.07 **0.11**	0.07 **0.11**	V max
			2.68	2.64 **2.62**	2.64 **2.62**	V min
I_S	Supply Current	Per Amplifier	1.35			mA

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LM6154AC LM6152AC Limit (2)	LM6154BC LM6152BC Limt (2)	Units
GBW	Gain-Bandwidth Product	f = 100 kHz	80			MHz

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

24V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for $T_J = 25°C$, $V^+ = 24V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LM6154AC LM6152AC Limit (2)	LM6154BC LM6152BC Limt (2)	Units
V_{OS}	Input Offset Voltage		0.3	2 **4**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**10**			µV/°C
I_B	Input Bias Current		500			nA
I_{OS}	Input Offset Current		32			nA
R_{IN}	Input Resistance, CM	$0V \le V_{CM} \le 23V$	60			Meg Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 23V$	94			dB
		$0V \le V_{CM} \le 24V$	84			
PSRR	Power Supply Rejection Ratio	$0V \le V_{CM} \le 24V$	95			dB
V_{CM}	Input Common-Mode Voltage Range	Low	−0.25	0	0	V
		High	24.25	24	24	V
A_V	Large Signal Voltage Gain	$R_L = 10\ k\Omega$	55			V/mV
V_O	Output Swing	$R_L = 10\ k\Omega$	0.044	0.075 **0.090**	0.075 **0.090**	V max
			23.91	23.8 **23.7**	23.8 **23.7**	V min
I_S	Supply Current	Per Amplifier	1.6	2.25 **2.50**	2.25 **2.50**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

24V AC Electrical Characteristics

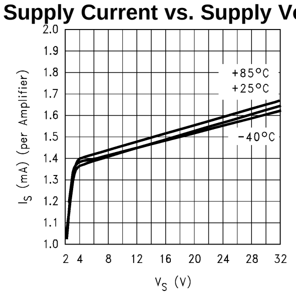
Unless otherwise specified, all limits are guaranteed for T_J = 25°C, V^+ = 24V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LM6154AC LM6152AC Limit (2)	LM6154BC LM6152BC Limt (2)	Units
GBW	Gain-Bandwidth Product	f = 100 kHz	80			MHz

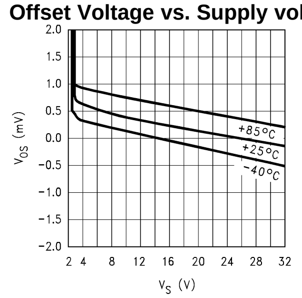
(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

Typical Performance Characteristics

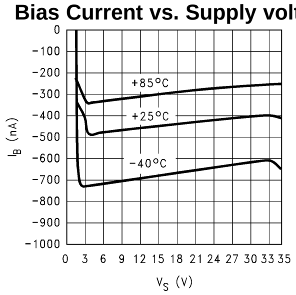
Supply Current vs. Supply Voltage



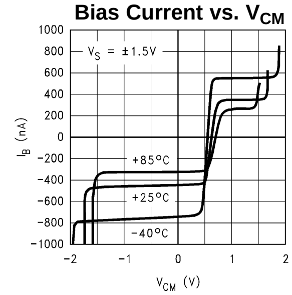
Offset Voltage vs. Supply voltage



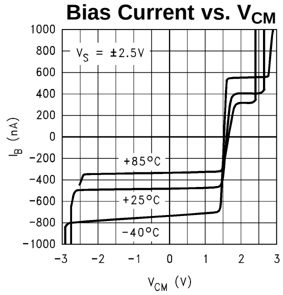
Bias Current vs. Supply voltage



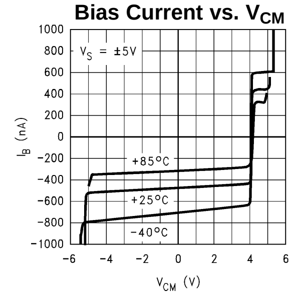
Bias Current vs. V_{CM}



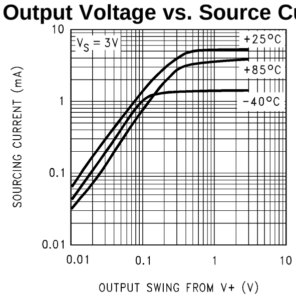
Bias Current vs. V_{CM}



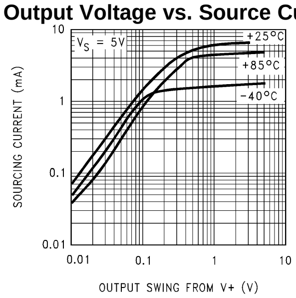
Bias Current vs. V_{CM}



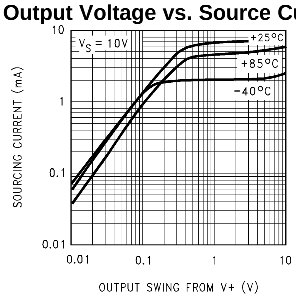
Output Voltage vs. Source Current



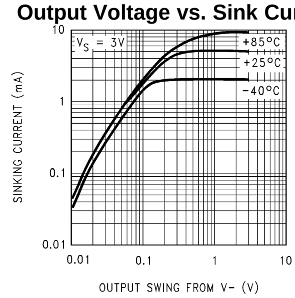
Output Voltage vs. Source Current



Output Voltage vs. Source Current

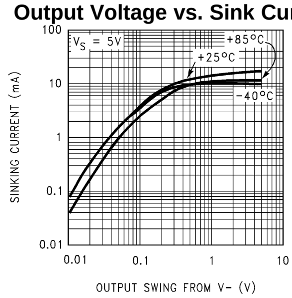


Output Voltage vs. Sink Current

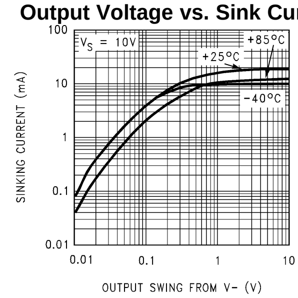


Typical Performance Characteristics (continued)

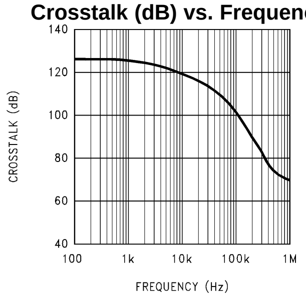
Output Voltage vs. Sink Current



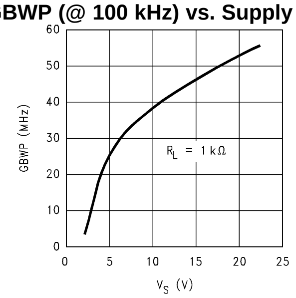
Output Voltage vs. Sink Current



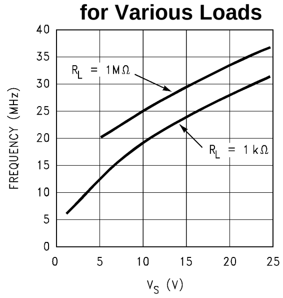
Crosstalk (dB) vs. Frequency



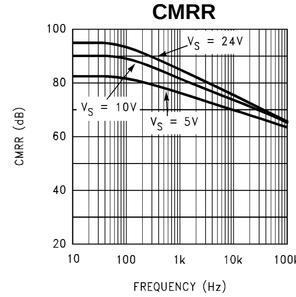
GBWP (@ 100 kHz) vs. Supply Voltage



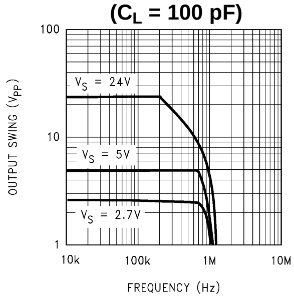
Unity Gain Frequency vs. Supply Voltage for Various Loads



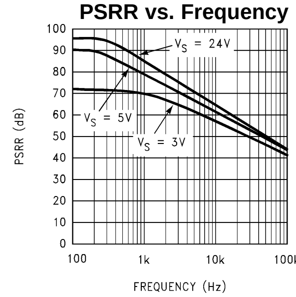
CMRR



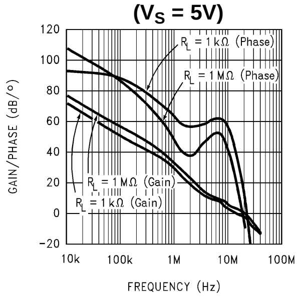
Voltage Swing vs. Frequency (C_L = 100 pF)



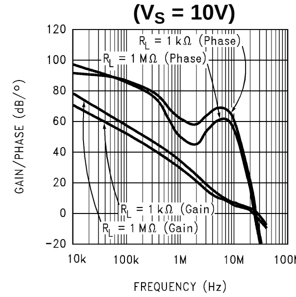
PSRR vs. Frequency



Open Loop Gain/Phase (V_S = 5V)

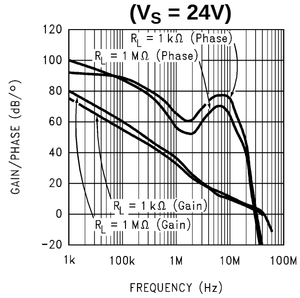


Open Loop Gain/Phase (V_S = 10V)

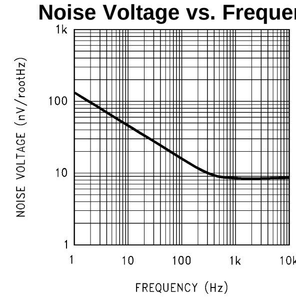


Typical Performance Characteristics (continued)

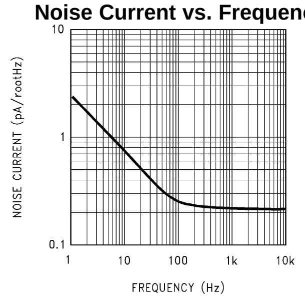
Open Loop Gain/Phase (V_S = 24V)



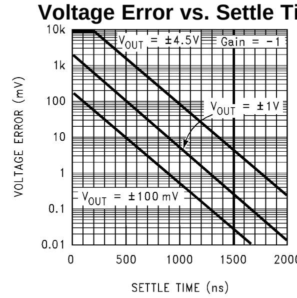
Noise Voltage vs. Frequency



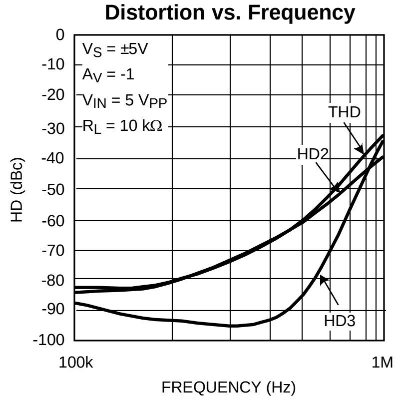
Noise Current vs. Frequency



Voltage Error vs. Settle Time



Distortion vs. Frequency



Application Information

The LM6152/LM6154 is ideally suited for operation with about 10 kΩ (Feedback Resistor, R_F) between the output and the negative input terminal.

With R_F set to this value, for most applications requiring a close loop gain of 10 or less, an additional small compensation capacitor (C_F) (see Figure 3) is recommended across R_F in order to achieve a reasonable overshoot (10%) at the output by compensating for stray capacitance across the inputs.

The optimum value for C_F can best be established experimentally with a trimmer cap in place since its value is dependant on the supply voltage, output driving load, and the operating gain. Below, some typical values used in an inverting configuration and driving a 10 kΩ load have been tabulated for reference:

Table 1. Typical BW (−3 dB) at Various Supply Voltage and Gains

V_S Volts	Gain	C_F pF	BW (−3 dB) MHz
3	−1	5.6	4
	−10	6.8	1.97
	−100	None	0.797

Table 1. Typical BW (−3 dB) at Various Supply Voltage and Gains (continued)

24	−1	2.2	6.6
	−10	4.7	2.2
	−100	None	0.962

In the non-inverting configuration, the LM6152/LM6154 can be used for closed loop gains of +2 and above. In this case, also, the compensation capacitor (C_F) is recommended across R_F (= 10 kΩ) for gains of 10 or less.

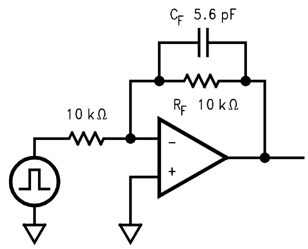


Figure 3. Typical Inverting Gain Circuit A_V = −1

Because of the unique structure of this amplifier, when used at low closed loop gains, the realizable BW will be much less than the GBW product would suggest.

The LM6152/LM6154 brings a new level of ease of use to op amp system design.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications where higher power consumption previously reduced battery life to unacceptable levels.

The ability to drive large capacitive loads without oscillating functional removes this common problem.

To take advantage of these features, some ideas should be kept in mind.

The LM6152/LM6154, capacitive loads do not lead to oscillations, in all but the most extreme conditions, but they will result in reduced bandwidth. They also cause increased settling time.

Unlike most bipolar op amps, the unique phase reversal prevention/speed-up circuit in the input stage, caused the slew rate to be very much a function of the input pulse amplitude. This results in a 10 to 1 increase in slew rate when the differential input signal increases. Large fast pulses will raise the slew-rate to more than 30 V/µs.

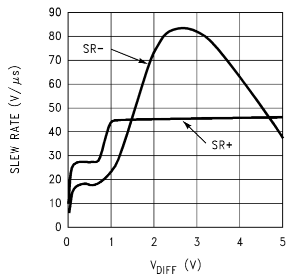


Figure 4. Slew Rate vs. V_{DIFF}

The speed-up action adds stability to the system when driving large capacitive loads.

A conventional op amp exhibits a fixed maximum slew-rate even though the differential input voltage rises due to the lagging output voltage. In the LM6152/LM6154, increasing lag causes the differential input voltage to increase but as it does, the increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. As a result, the LM6152/LM6154 can drive capacitive loads as large as 470 pF at gain of 2 and above, and not oscillate.

Capacitive loads decrease the phase margin of all op amps. This can lead to overshoot, ringing and oscillation. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase shift network. The LM6152/6154 senses this phase shift and partly compensates for this effect.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LM6152ACM	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	
LM6152ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LM6152ACMX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LM6152ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LM6152BCM	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	
LM6152BCM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LM6152BCMX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LM6152BCMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LM6154BCM	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	
LM6154BCM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LM6154BCMX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LM6154BCMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

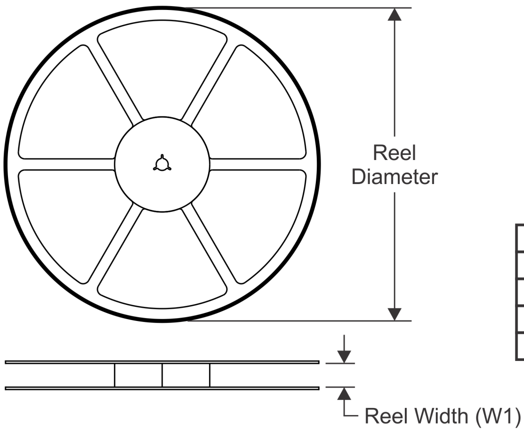
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

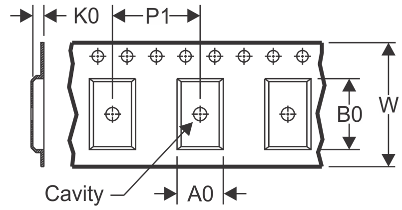
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

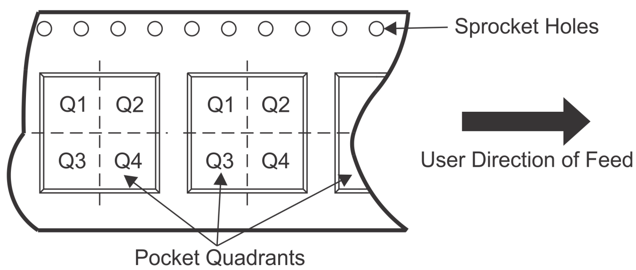


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

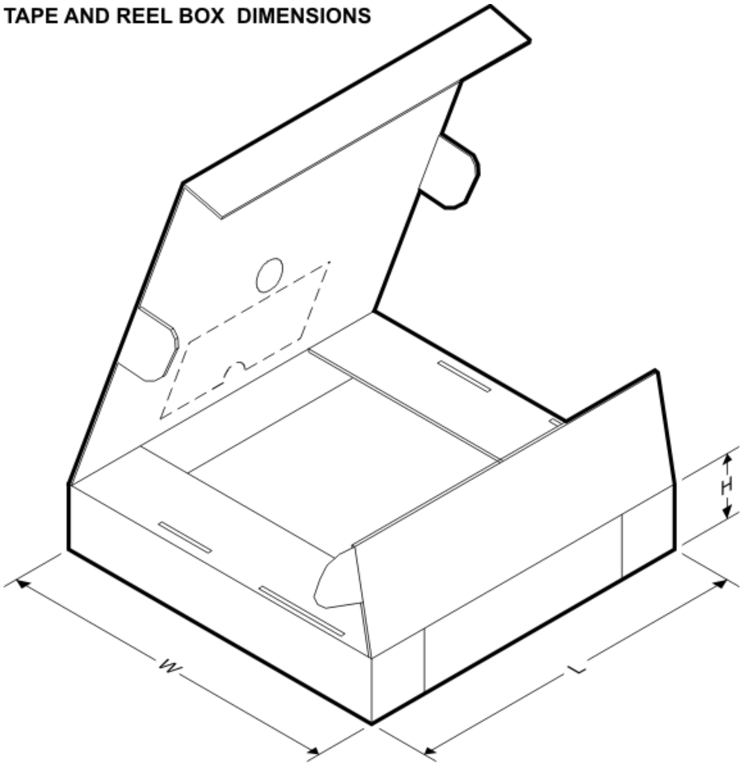
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6152ACMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6152ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6152BCMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6152BCMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6154BCMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM6154BCMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

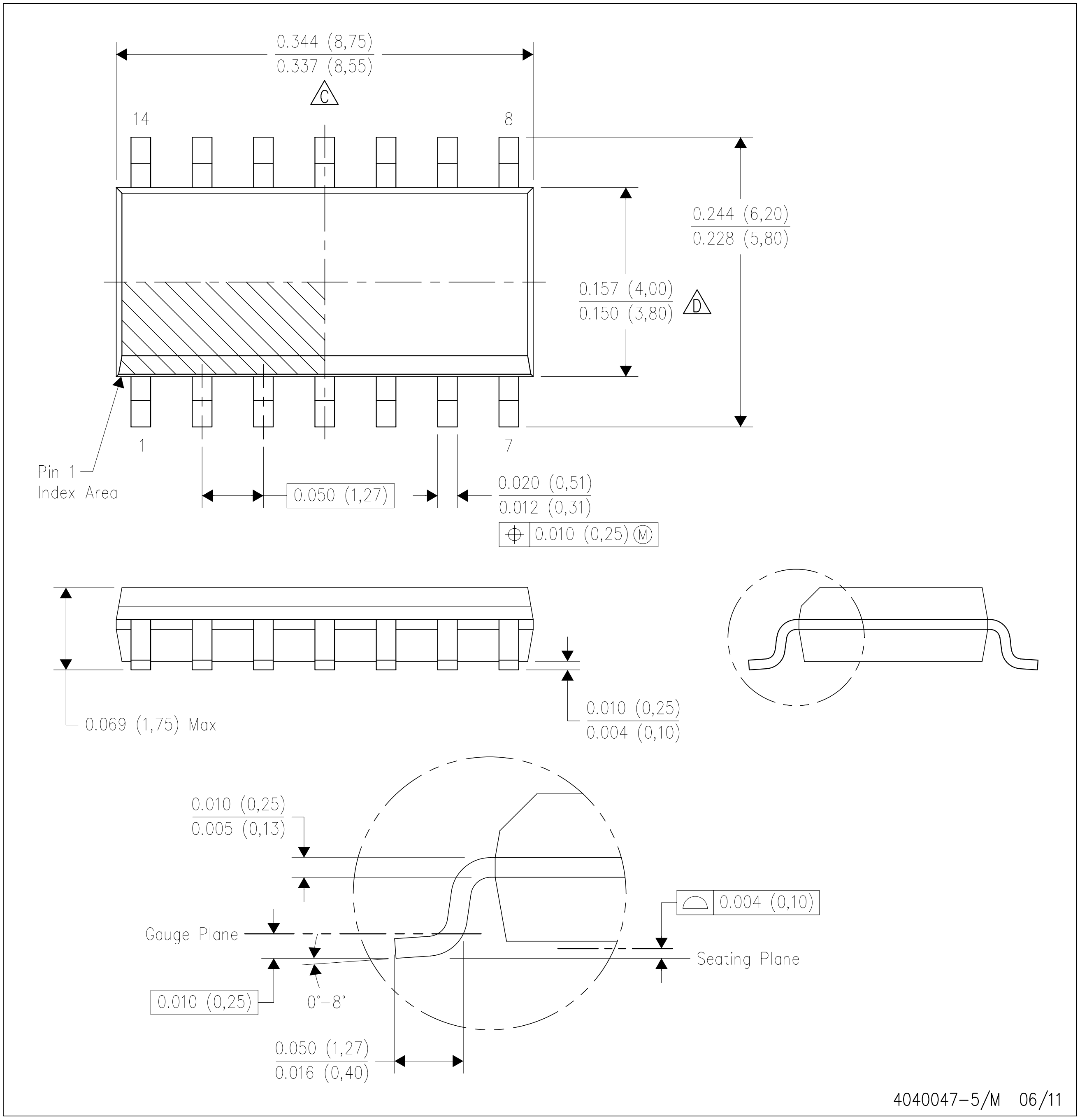
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

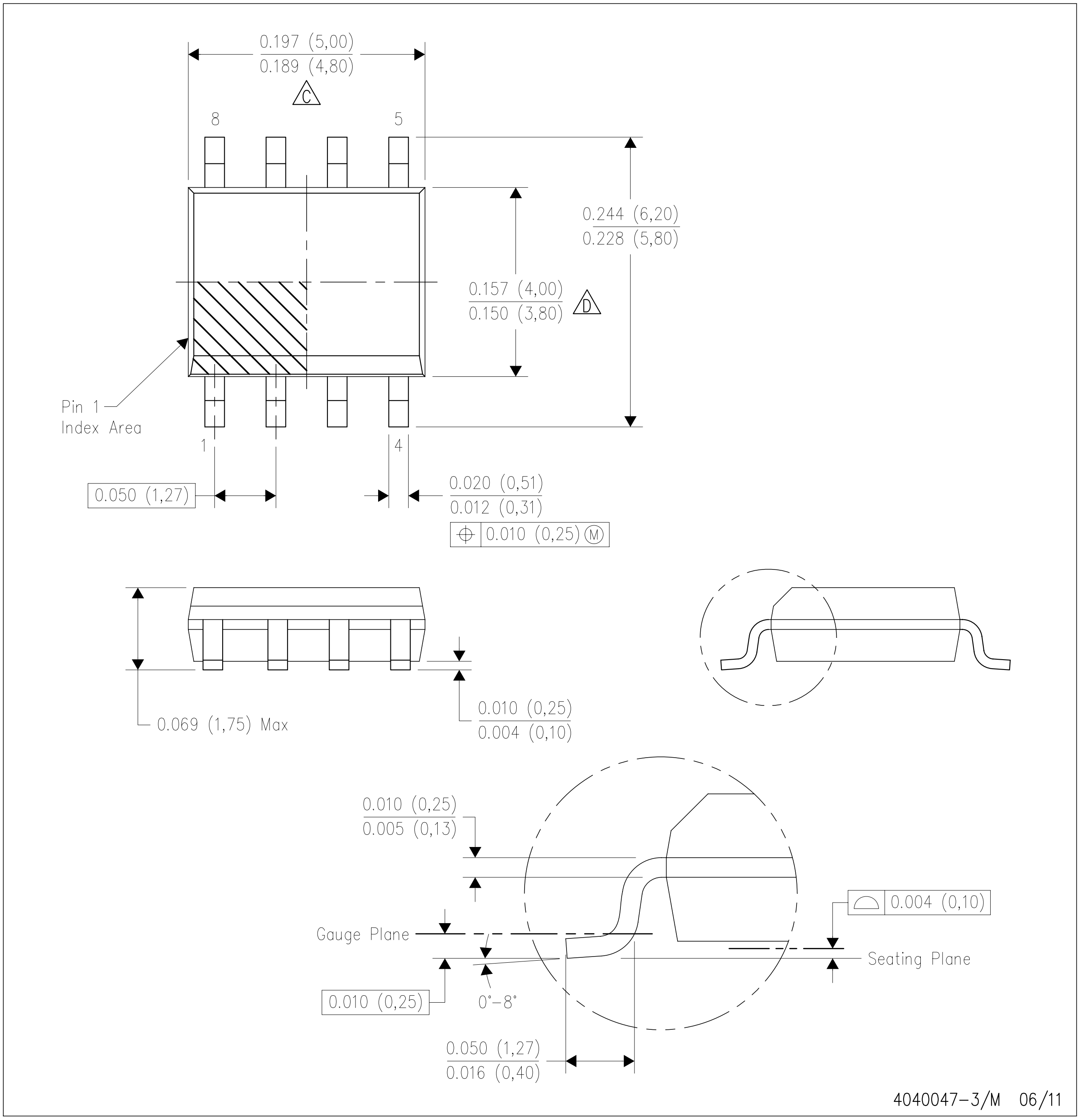
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6152ACMX	SOIC	D	8	2500	349.0	337.0	45.0
LM6152ACMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM6152BCMX	SOIC	D	8	2500	349.0	337.0	45.0
LM6152BCMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM6154BCMX	SOIC	D	14	2500	349.0	337.0	45.0
LM6154BCMX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

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