National Semiconductor Corporation

PRELIMINARY

LM6164/LM6264/LM6364 High Speed Operational Amplifier

General Description

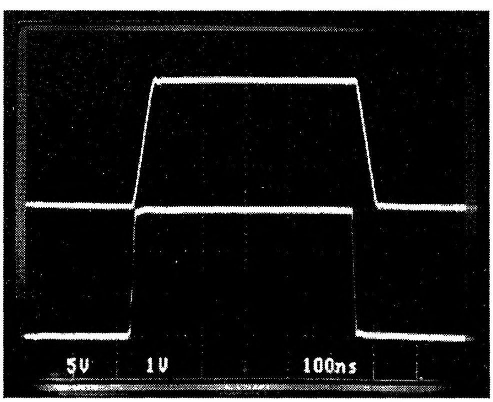
The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per μs and 175 MHz GBW (stable to a gain of +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's new VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

■ High Slew Rate	300 V/μs
■ High GBW Product	175 MHz
■ Low Supply Current	5 mA
■ Fast settling	100 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	<0.1°
■ Wide Supply Range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved; easy to apply	

Typical AC Characteristics



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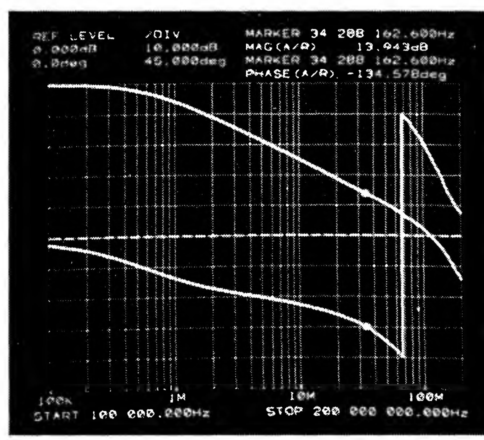
Step Response; $A_V = +5$



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Gain & Phase; $A_V = +300$

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
CM Input Voltage	(V^+ − 0.7V) to (V^- − 7V)
Output Short Circuit to Gnd (Note 1)	Continuous
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range (Note 2)	
LM6164	−55°C to +125°C
LM6264	−25°C to +85°C
LM6364	0°C to +70°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 8 & 9)	±700V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LM6164 Tested Limit (Note 4)	LM6164 Design Limit (Note 5)	LM6264 Tested Limit (Note 4)	LM6264 Design Limit (Note 5)	LM6364 Tested Limit (Note 4)	LM6364 Design Limit (Note 5)	Units
Input Offset Voltage		2	4 **6**		4	**6**	9	**11**	mV max
Input Offset Voltage Average Drift		6							μV/°C
Input Bias Current		2.5	3 **6**		3	**5**	5	**6**	μA max
Input Offset Current		150	350 **800**		350	**600**	1500	**1900**	nA max
Input Offset Current Average Drift		0.3							nA/°C
Input Resistance	Differential	100							kΩ
Input Capacitance		3.0							pF
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 11)	2.5	1.8 **0.9**		1.8	**1.2**	1.3	**1.1**	V/mV min
	R_L = 10 kΩ	9							
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9	**+13.8**	+13.8	**+13.7**	V min
		−13.5	−13.3 **−13.1**		−13.3	**−13.1**	−13.2	**−13.1**	V min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9	**3.8**	3.8	**3.7**	V min
		1.5	1.7 **1.9**		1.7	**1.9**	1.8	**1.9**	V max
Common-Mode Rejection Ratio	−10V ≤ V_{CM} ≤ +10V	105	86 **80**		86	**82**	80	**78**	dB min
Power Supply Rejection Ratio	±10V ≤ V± ≤ ±16V	96	86 **80**		86	**82**	80	**78**	dB min
Output Voltage Swing	Supply = ±15V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**		+13.5	**+13.3**	+13.4	**+13.3**	V min
		−13.4	−13.0 **−12.7**		−13.0	**−12.8**	−12.9	**−12.8**	V min
	Supply = +5V and R_L = 2 kΩ (Note 6)	4.2	3.5 **3.3**		3.5	**3.3**	3.4	**3.3**	V min
		1.3	1.7 **2.0**		1.7	**1.9**	1.8	**1.9**	V max

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LM6164 Tested Limit (Note 4)	LM6164 Design Limit (Note 5)	LM6264 Tested Limit (Note 4)	LM6264 Design Limit (Note 5)	LM6364 Tested Limit (Note 4)	LM6364 Design Limit (Note 5)	Units
Output Short Circuit Current	Source	65	30 **20**		30	**25**	30	**25**	mA min
	Sink	65	30 **20**		30	**25**	30	**25**	mA min
Supply Current		5.0	6.5 **6.8**		6.5	**6.7**	6.8	**6.9**	mA max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LM6164 Tested Limit (Note 4)	LM6164 Design Limit (Note 5)	LM6264 Tested Limit (Note 4)	LM6264 Design Limit (Note 5)	LM6364 Tested Limit (Note 4)	LM6364 Design Limit (Note 5)	Units
Gain-Bandwidth Product	@ F = 20 MHz	175	140 **100**		140	**120**	120	**100**	MHz min
	$V+ = \pm 5V$	120							
Slew Rate	$A_V = +20$ (Note 10)	300	225 **200**		225	**210**	200	**180**	V/μs min
	$V+ = \pm 5V$	200							
Power Bandwidth	$V_{OUT} = 20\ V_{PP}$	4.5							MHz
Setting Time	10V Step to 0.1% $A_V = -4$, $R_L = 2\ k\Omega$	100							ns
Phase Margin	$A_V = +5$	45							Deg
Differential Gain	NTSC, $A_V = +10$	<0.1							%
Differential Phase	NTSC, $A_V = +10$	<0.1							Deg
Input Noise Voltage	F = 10 kHz	8							$nV/\sqrt{Hz}$
Input Noise Current	F = 10 kHz	1.5							$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, the cerdip (J) package is 125°C/Watt, and the TO-5 (H) package is 155°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guranteed for $T_A = T_J = 25°C$ with supply voltage = ±15V, $V_{CM} = 0V$, and $R_L \geq 100\ k\Omega$. **Boldface** limits apply over the range listed under "Operating Temperature Range".

Note 4: Guaranteed and 100% production tested. These limits are used to calculate outgoing AQL levels.

Note 5: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 6: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, $V_{CM} = 2.5V$, $V_{OUT} = 2.5V$. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 7: $C_L \leq 5$ pF.

Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

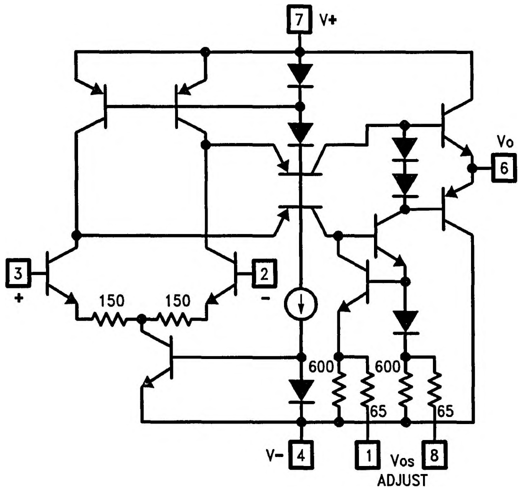
Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 10: V_{IN} = 4V step. For V+ = ±5V, V_{IN} = 1V step.

Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Simplified Schematic & Pin Assignments

Dual-In-Line Package



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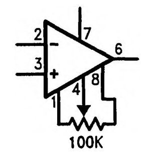
Order Number LM6264J, LM6164J, LM6364N or LM6264N
See NS Package Number J08A or N08E

V_{OS} Adjust Circuit



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