National Semiconductor

LM6118/LM6218A/LM6218
Fast Settling Dual Operational Amplifier

General Description

The LM6118 series are monolithic fast-settling unity-gain-compensated dual operational amplifiers with ±20 mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is ±5V to ±20V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIP™ (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

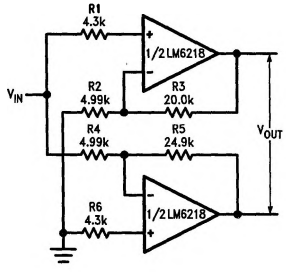
Features

	Typical
■ Low offset voltage	0.2 mV
■ 0.01% settling time	400 ns
■ Slew rate $A_V = -1$	140 V/μs
■ Slew rate $A_V = +1$	75 V/μs
■ Gain bandwidth	17 MHz
■ Total supply current	5.5 mA
■ Output drives 50Ω load (±1V)	
■ Well-behaved, easy to use	

Applications

- D/A converters
- Fast integrators
- Active filters

Typical Applications

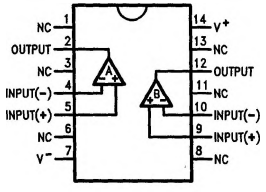


TL/H/10254–1

Single ended input to differential output
A_V = 10, BW = 3.2 MHz
40 V_{p-p} Response = 1.4 MHz
V_S = ±15V

Wide-Band, Fast-Settling 40 V_{p-p} Amplifier

Small Outline Package (WM)



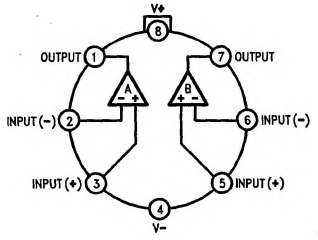
TL/H/10254–3

Top View

Order Number LM6218AWM or LM6218WM
See NS Package Number M14B

Connection Diagrams and Order Information

Metal Can Package (H)



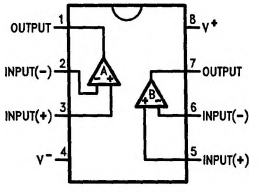
TL/H/10254–2

Top View

Note: Pin 4 connected to case

Order Number LM6118H or LM6218AH
See NS Package Number H08A

Dual-In-Line Package (J or N)



TL/H/10254–4

Top View

Order Number LM6118J, LM6218AJ, LM6218AN or LM6218N
See NS Package Number J08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	42V
Input Voltage	(Note 2)
Differential Input Current (Note 3)	±10 mA
Output Current (Note 4)	Internally Limited
Power Dissipation (Note 5)	500 mW
ESD Tolerance (C = 100 pF, R = 1.5 kΩ)	±2 kV
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Temp. Range

LM6118	−55°C to +125°C
LM6218A	−40°C to +85°C
LM6218	−40°C to +85°C

Electrical Characteristics

$\pm 5V \le V_S \le \pm 20V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $I_{OUT} = 0A$, unless otherwise specified. Limits with standard type face are for $T_J = 25°C$, and **Bold Face Type** are for **Temperature Extremes.**

Parameter	Conditions	Typ 25°C	LM6118 Limits (Note 6)	LM6218A Limits (Note 7)	LM6218 Limits (Note 7)	Units
Input Offset Voltage	$V_S = \pm 15V$	0.2	1 **2**	1 **2**	3 **4**	mV (max)
Input Offset Voltage	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	0.3	1.5 **2.5**	1.5 **2.5**	3.5 **4.5**	mV (max)
Input Offset Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	20	50 **100**	50 **100**	100 **200**	nA (max)
Input Bias Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	200	350 **950**	350 **950**	500 **1250**	nA (max)
Input Common Mode Rejection Ratio	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$ $V_S = \pm 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Positive Power Supply Rejection Ratio	$V^- = -15V$ $5V \le V^+ \le 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Negative Power Supply Rejection Ratio	$V^+ = 15V$ $-20V \le V^- \le -5V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Large Signal Voltage Gain	$V_{out} = \pm 17V$ $R_L = 10k$ $V_S = \pm 20V$	500	150 **100**	150 **100**	100 **70**	V/mV (min)
	$V_{out} = \pm 10V$ $R_L = 500$ $V_S = \pm 15V$ (±20 mA)	200	50 **30**	50 **30**	40 **25**	V/mV (min)
Total Supply Current	$V_S = \pm 15V$	5.5	7 **7.5**	7 **7.5**	7 **7.5**	mA (max)
Output Current Limit	$V_S = \pm 15V$, Pulsed	65	80	80	80	mA (max)
Slew Rate, Av = −1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	140	100 **50**	100 **50**	100 **50**	V/μs (min)
Slew Rate, Av = +1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	75	50 **30**	50 **30**	50 **30**	V/μs (min)
Gain-Bandwidth Product	$V_S = \pm 15V$, $f_o = 200$ kHz	17	14	14	13	MHz (min)
0.01% Settling Time $A_V = -1$	$\Delta V_{out} = 10V$, $V_S = \pm 15V$, $R_S = R_f = 2k$, $C_f = 10$ pF	400				ns
Input Capacitance	Inverter	5				pF
	Follower	3				pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage range is ($V^+ - 1V$) to (V^-).

Note 3: The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

Note 4: Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

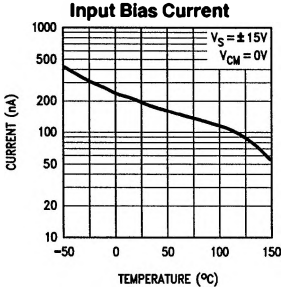
Note 5: Devices must be derated using a thermal resistance of 150°C/W junction to ambient for the H package, 90°C/W for the N, J and WM packages. If a heat sink is used on the H package, use a thermal resistance of 45°C/W junction to case.

Note 6: All limits are 100% production tested at 25°C and at temperature extremes. All limits are used to calculate AOQL, (Average Outgoing Quality Level).

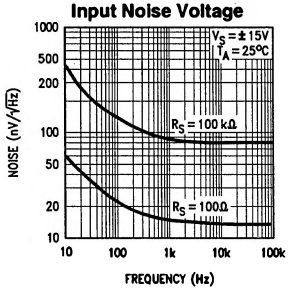
Note 7: 25°C limits are 100% production tested. Temperature extreme limits are guaranteed via correlation using accepted SQC (Statistical Quality Control) methods. All limits are used to calculate AOQL.

Typical Performance Characteristics

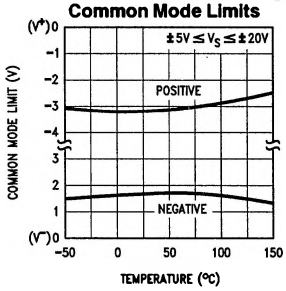
Input Bias Current



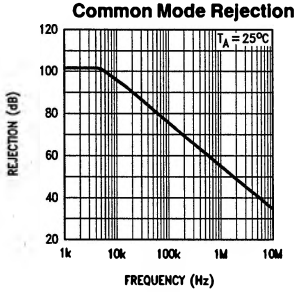
Input Noise Voltage



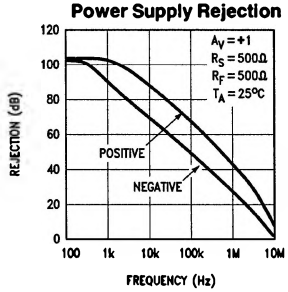
Common Mode Limits



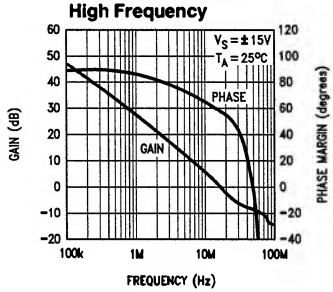
Common Mode Rejection



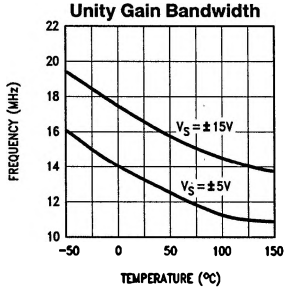
Power Supply Rejection



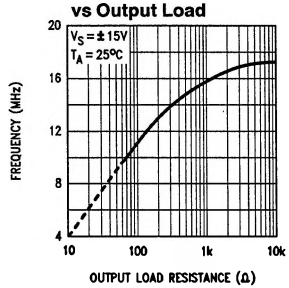
Frequency Response High Frequency



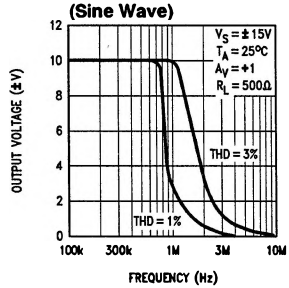
Unity Gain Bandwidth



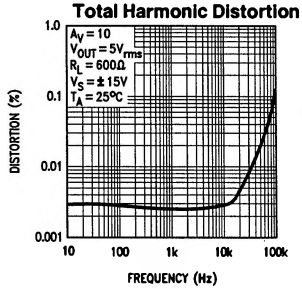
Unity Gain Bandwidth vs Output Load



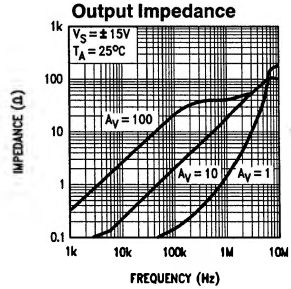
Large Signal Response (Sine Wave)



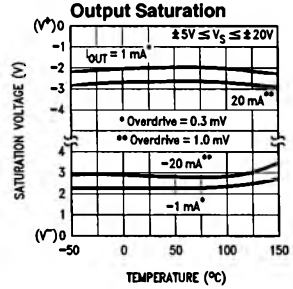
Total Harmonic Distortion



Output Impedance



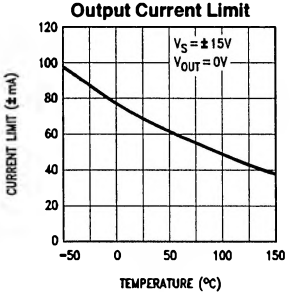
Output Saturation



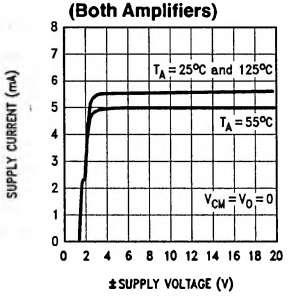
TL/H/10254–5

Typical Performance Characteristics (Continued)

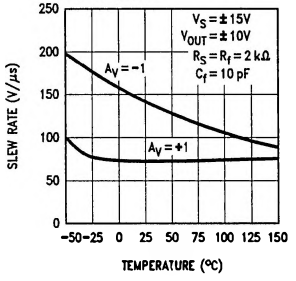
Output Current Limit



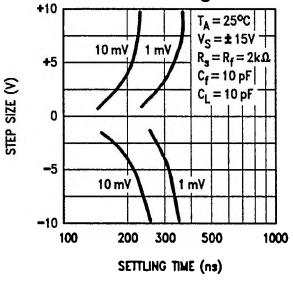
Supply Current (Both Amplifiers)



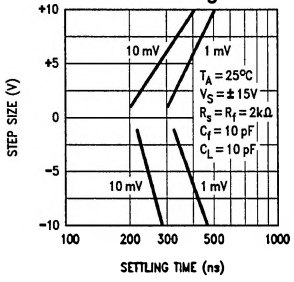
Slew Rate



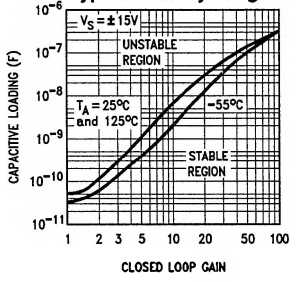
Inverter Settling Time



Follower Settling Time

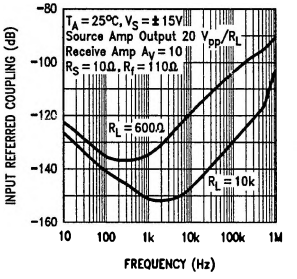


Typical Stability Range



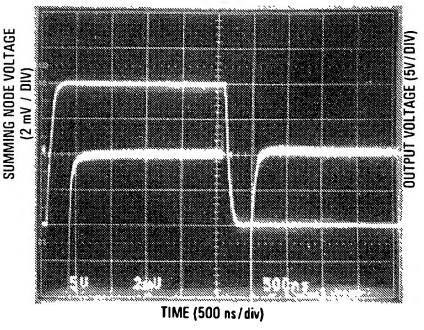
TL/H/10254–6

Amplifier to Amplifier Coupling



TL/H/10254–23

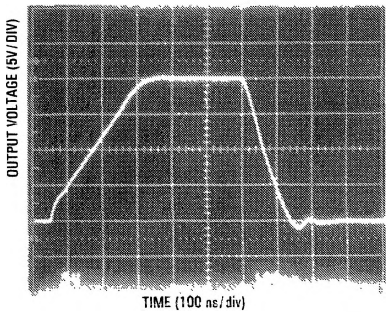
Settling Time, Vs = ±15V



TL/H/10254–7

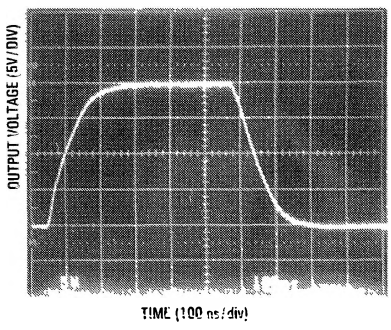
Typical Performance Characteristics (Continued)

Step Response, Av = +1, Vs = ±15V



TL/H/10254–8

Step Response, Av = −1, Vs = ±15V



TL/H/10254–9

Application Information

General

The LM6118 series are high-speed, fast-settling dual op-amps. To insure maximum performance, circuit board layout is very important. Minimizing stray capacitance at the inputs and reducing coupling between the amplifier's input and output will minimize problems.

Supply Bypassing

To assure stability, it is recommended that each power supply pin be bypassed with a 0.1 µF low inductance capacitor near the device. If high frequency spikes from digital circuits or switching supplies are present, additional filtering is recommended. To prevent these spikes from appearing at the output, R-C filtering of the supplies near the device may be necessary.

Power Dissipation

These amplifiers are specified to 20 mA output current. If accompanied with high supply voltages, relatively high power dissipation in the device will occur, resulting in high junction temperatures. In these cases the package thermal resistance must be taken into consideration. (See Note 5 under Electrical Characteristics.) For high dissipation, an H package with a heat sink or a N package with large areas of copper on the pc board is recommended.

Amplifier Shut Down

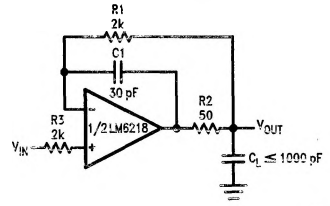
If one of the amplifiers is not used, it can be shut down by connecting both the inverting and non-inverting inputs to the V^- pin. This will reduce the power supply current by approximately 25%.

Capacitive Loading

Maximum capacitive loading is about 50 pF for a closed-loop gain of +1, before the amplifier exhibits excessive ringing and becomes unstable. A curve showing maximum capacitive loads, with different closed-loop gains, is shown in the Typical Performance Characteristics section.

To drive larger capacitive loads at low closed-loop gains, isolate the amplifier output from the capacitive load with 50Ω. Connect a small capacitor directly from the amplifier output to the inverting input. The feedback loop is closed from the isolated output with a series resistor to the inverting input.

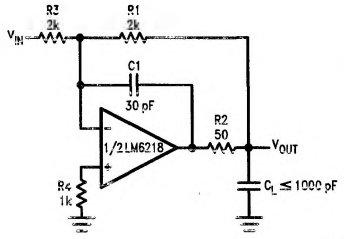
Voltage Follower



TL/H/10254–10

For C_L = 1000 pF, Small signal BW = 5 MHz
20 V_{p-p} BW = 500 kHz

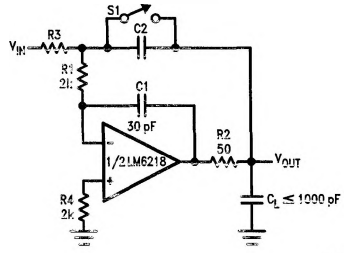
Inverter



TL/H/10254–11

Settling time to 0.01%, 10V Step
For C_L = 1000 pF, settling time ≈ 1500 ns
For C_L = 300 pF, settling time ≈ 500 ns

Integrator



TL/H/10254–12

Application Information (Continued)

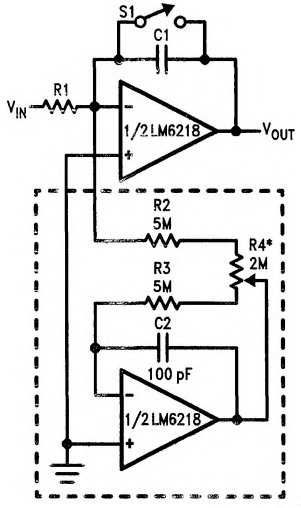
Examples of unity gain connections for a voltage follower, inverter, and integrator driving capacitive loads up to 1000 pF are shown here. Different R1–C1 time constants and capacitive loads will have an effect on settling times.

Input Bias Current Compensation

Input bias current of the first op amp can be reduced or balanced out by the second op amp. Both amplifiers are laid out in mirror image fashion and in close proximity to each other, thus both input bias currents will be nearly identical and will track with temperature. With both op amp inputs at the same potential, a second op amp can be used to convert bias current to voltage, and then back to current feeding the first op amp using large value resistors to reduce the bias current to the level of the offset current.

Examples are shown here for an inverting application, (a) where the inputs are at ground potential, and a second circuit (b) for compensating bias currents for both inputs.

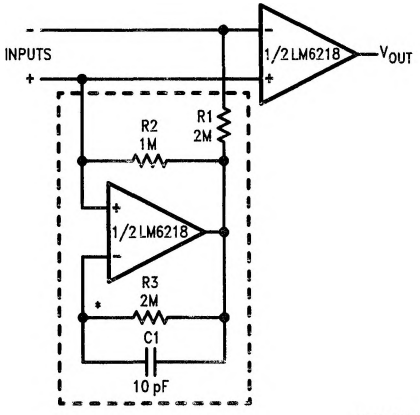
Bias Current Compensation



*adjust for zero integrator drift

TL/H/10254–13

(a) Inverting Input Bias Compensation for Integrator Application

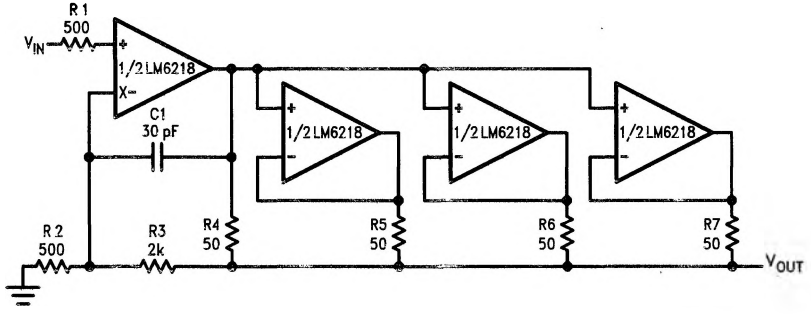


TL/H/10254–14

*mount resistor close to input pin to minimize stray capacitance

(b) Compensation to Both Inputs

Amplifier/Parallel Buffer

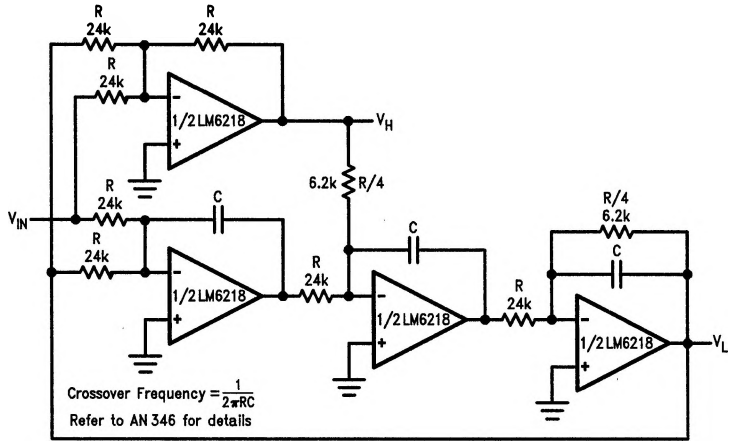


TL/H/10254–15

A_V = +5, $I_{OUT} \leq$ 80 mA
V_S = ±15V, $C_L \leq$ 0.01 μF
Large and small signal B.W. = 1.3 MHz (THD = 3%)

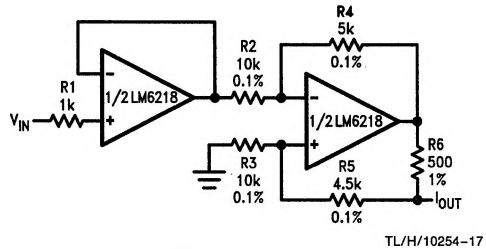
Application Information (Continued)

Constant-Voltage Crossover Network With 12 dB/Octave Slope



TL/H/10254–16

Bilateral Current Source



TL/H/10254–17

V_S = ±15V, −10 ≤ V_{IN} ≤ 10V

$\frac{I_{OUT}}{V_{IN}} = \frac{R4}{R2\,R6} = \frac{1\text{ mA}}{1\text{V}}$

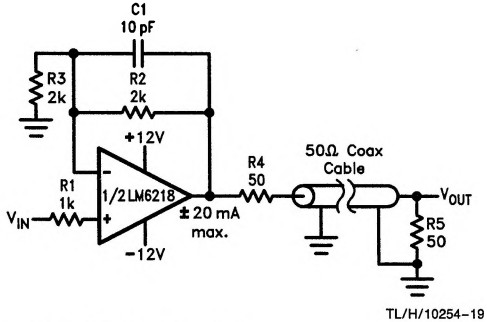
Output dynamic range = 10V − R6 $|I_{OUT}|$

R_L = 500Ω, small signal BW = 6 MHz

Large signal response = 800 kHz

C_{out} equiv. = $\frac{R2 + R4}{2\pi\, f_O\, R2\, R6}$ = 32 pF (f_O = 15 MHz)

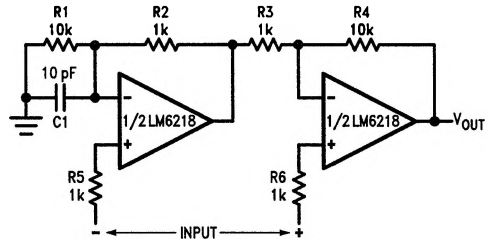
Coaxial Cable Driver



TL/H/10254–19

Small signal (200 mV_{p-p}) BW ≈ 5 MHz

Instrumentation Amplifier

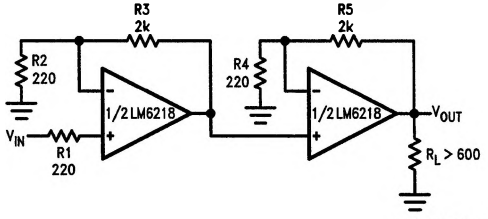


TL/H/10254–18

A_V = 10, V_S = ±15V, All resistors 0.01%

Small signal and large signal (20 V_{P-P}) B.W. ≈ 800 kHz

150 MHz Gain-Bandwidth Amplifier



TL/H/10254–20

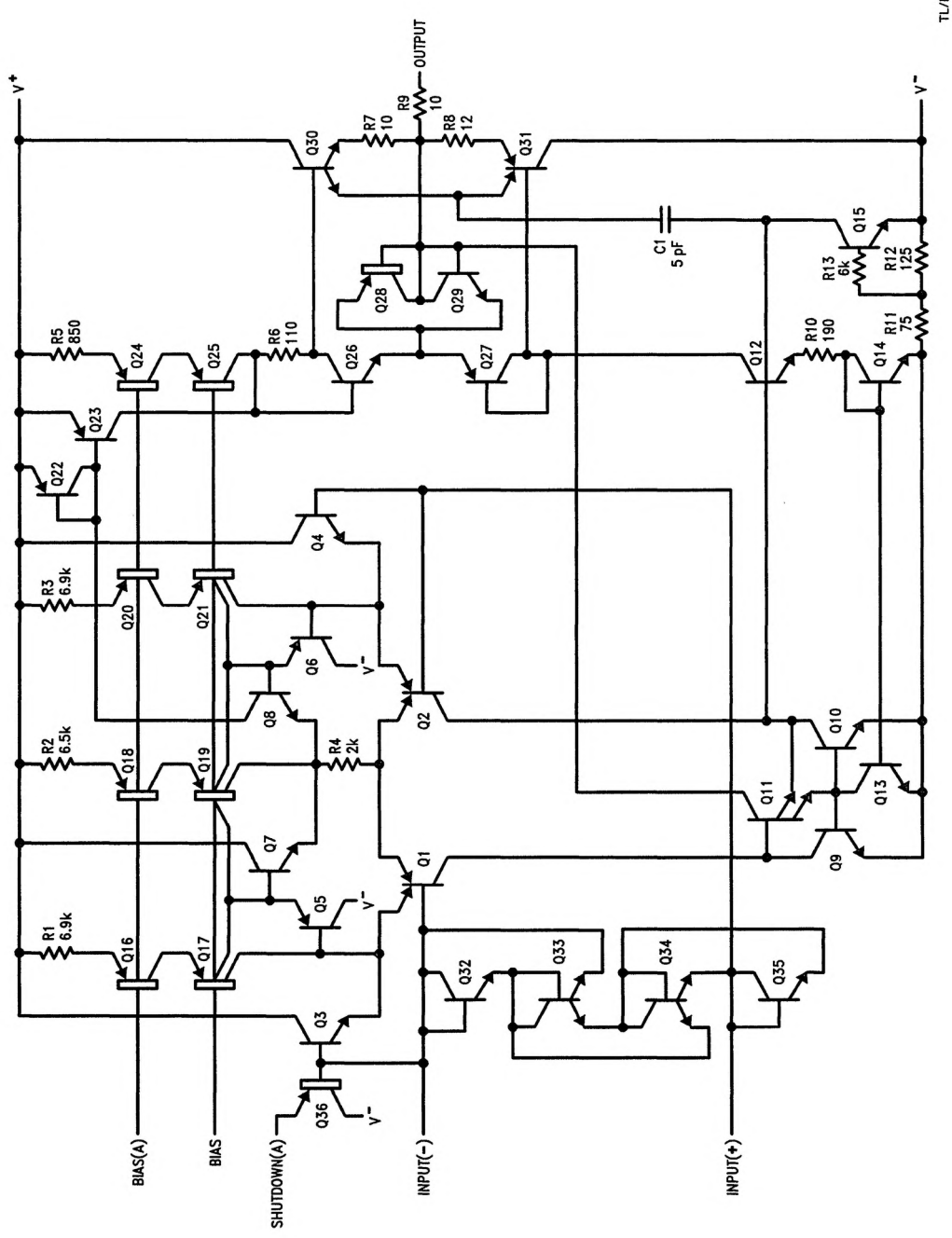
A_V = 100, V_S = ±15V,

Small signal BW ≈ 1.5 MHz

Large signal BW (20 V_{p-p}) ≈ 800 kHz

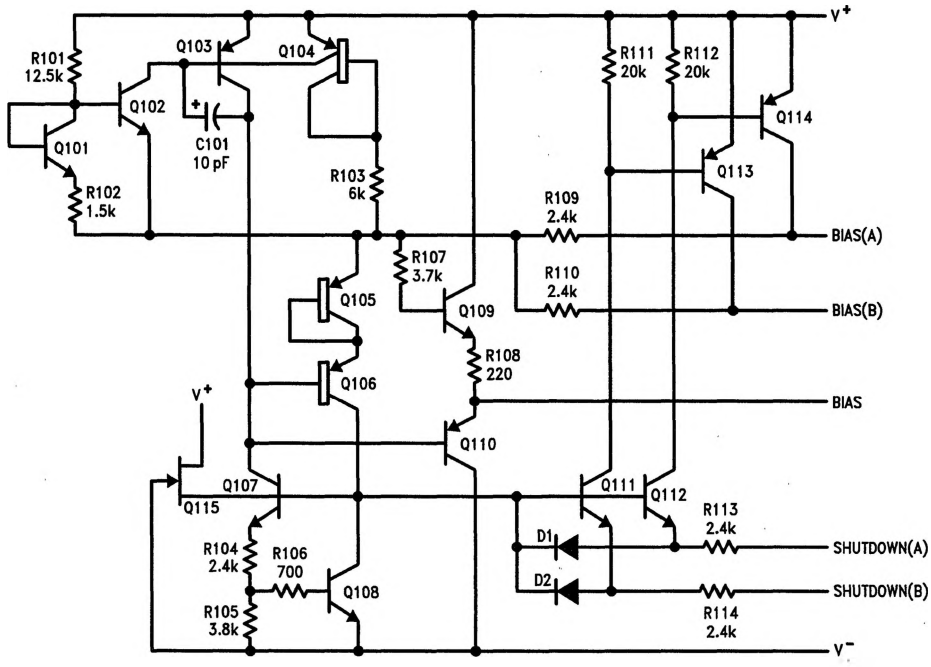
Schematic Diagram

½ LM6118 (Op Amp A)



Schematic Diagram (Continued)

Bias Circuit



TL/H/10254–22