LM6511 180 ns 3V Comparator

Check for Samples: LM6511

FEATURES

- **(Typical unless otherwise noted)**
- **Operates at +2.7V, +3V, +3.3V, +5V**
- **Low Power consumption <9.45 mW @ V^+ = 2.7V (max)**
- **Fast Response Time of 180 ns**

APPLICATIONS

- **Portable Equipment**
- **Cellular Phones**
- **Digital Level Shifting**

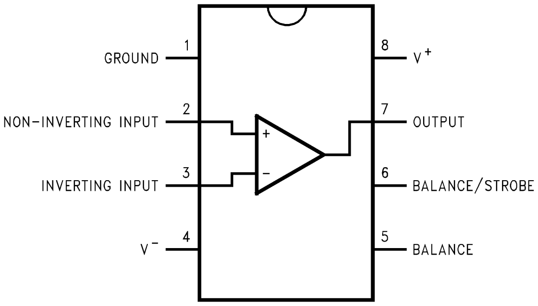
DESCRIPTION

The LM6511 voltage comparator is ideal for analog-digital interface circuitry when only a +3V or +3.3V supply is available. The open-collector output permits signal compatibility with a wide variety of digital families: +5V CMOS, +3V CMOS, TTL and so on. Supply voltage may range from 2.7V to 36V between supply voltage leads. The LM6511 operates with little power consumption (P_{diss} < 9.45 mW at V^+ = +2.7V and V^- = 0V).

This voltage comparator offers many features that are available in traditional sub-microsecond comparators: output sync strobe, inputs and output may be isolated from system ground, and wire-ORing. Also, the LM6511 uses the industry-standard, single comparator pinout configuration.

Connection Diagram

Figure 1. 8-Pin SO



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage	−0.3 to +36V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Differential Input Voltage	±30V
Input Voltage	(Note 2)
Storage Temperature Range	−65°C to +150°C
Soldering Information:	
SO Package (Vapor Phase in 60 sec) SO Package (Infrared in 15 sec)	215°C 220°C
Power Dissipation	500 mW
Output Short Circuit Duration	10s
Junction Temperature	150°C
ESD Rating	
(C = +100 pF, R = 1.5 kΩ)	300V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Operating Ratings (1)

Supply Voltage	2.5V to 30V
Temperature Range	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
SO Package	170°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 2.7V$, $V^- = 0V$, $50\Omega \le R_L \le 50k\Omega$, and $I_L = 1.0$ mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I	Units (Limits)
				Limit	
V_{OS}	Offset Voltage	$R_S \le 50$ kΩ (1)	1.5	5	mV
				8	max
I_B	Input Bias Current		38	130	nA max
				200	
I_{OS}	Input Offset Current	$R_S \le 50$ kΩ (1)	1.5	20	nA max
				50	
I_S	Positive Supply Current		2.7	3.5	mA max
				5	
	Negative Supply Current		1.5	2.0	
				2.5	
V_{SAT}	Saturation Voltage	$V_{IN} \le 10$ mV $I_{SINK} = 8$ mA	0.23	0.4	V
				0.4	max
A_V	Large Signal Voltage Gain	$\Delta V_{OUT} = 2V$	40		V/mV
CMRR	Common Mode Rejection Ratio		72		dB
I_{STROBE}	Strobe ON Current (2)		2.0	5.0	mA max
V_{IN}	Input Voltage Range			0.50	V min
				$V^+ - 1.25$	V max
	Output Leakage Current	$V_{IN} \ge 10$ mV, $V_{OUT} = 35V$, $I_{STROBE} = 3$ mA	0.2		nA max

(1) The offset voltage and offset current limits are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Therefore, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

(2) This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 mA to 5 mA.

AC Electrical Characteristics

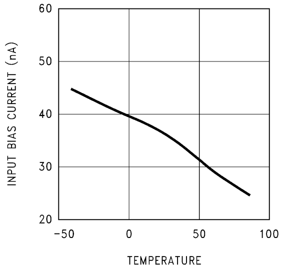
Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 2.7V$, $V^- = 0V$, $50\Omega \le R_L \le 50k\Omega$, and $I_L = 1.0$ mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I	Units (Limits)
				Limit	
T_R	Response Time	(Note 4)	180		ns

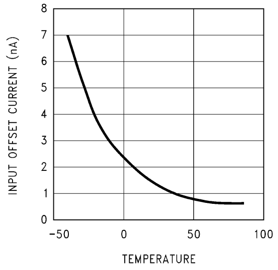
LM6511 Typical Performance Characteristics

V_S = 3V unless otherwise noted

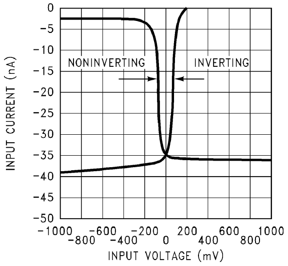
Input Bias Current



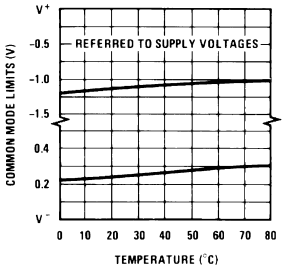
Input Offset Current



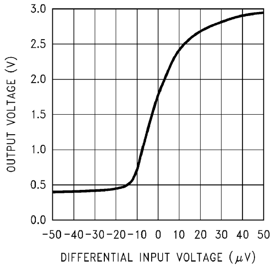
Input Current vs. Input Voltage



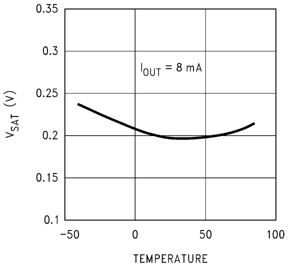
Common Mode Limits



Transfer Function

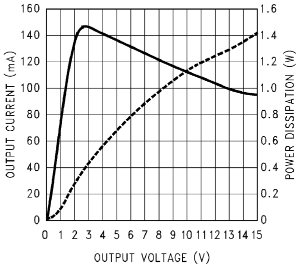


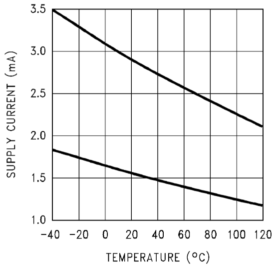
Output Saturation Voltage



Supply Current vs. Temperature

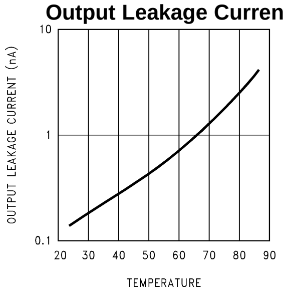
Output Current Limiting

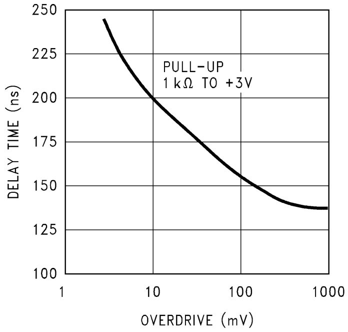




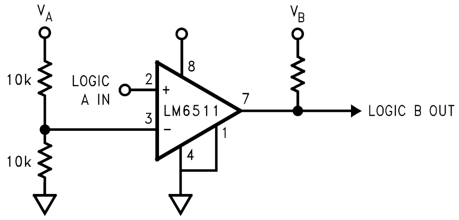
LM6511 Typical Performance Characteristics (continued)

V_S = 3V unless otherwise noted


Output Leakage Current


Propagation Delay vs. Overdrive

Typical Application



Notes: Because of the very wide operating and output voltage range, the LM6511 may be used to shift logic levels from 3V to TTL or CMOS to the other way around. By biasing the input to ½ of the input logic supply (V_A), this assures that this input remains within the input voltage range. The pull-up resistor should go to the output logic supply (V_B).

Figure 2. Universal Logic Level Shifter

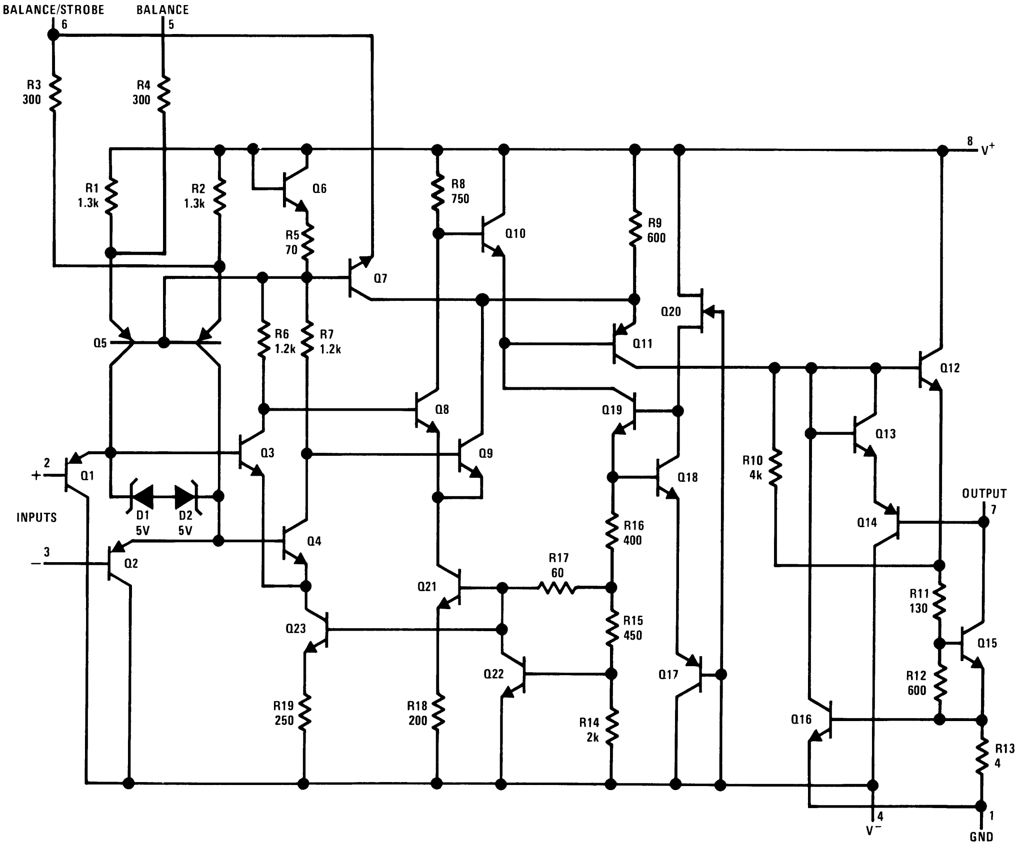

BALANCE/STROBE
6
BALANCE
5
R3
300
R4
300
8
V+
R1
1.3k
R2
1.3k
Q6
R8
750
R5
70
Q10
R9
600
Q7
Q20
Q5
R6
1.2k
R7
1.2k
Q11
Q12
Q8
Q19
Q13
2
+
Q1
Q3
Q9
R10
4k
Q18
OUTPUT
7
INPUTS
D1
5V
D2
5V
Q14
R16
400
3
−
Q4
Q2
R17
60
R11
130
Q21
R15
450
Q15
Q23
Q22
Q17
R12
600
R19
250
R18
200
R14
2k
Q16
R13
4
4
V−
1
GND

Figure 3.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LM6511IM	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	
LM6511IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LM6511IMX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LM6511IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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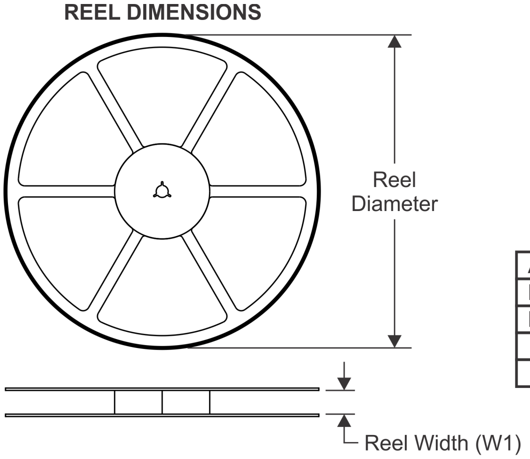
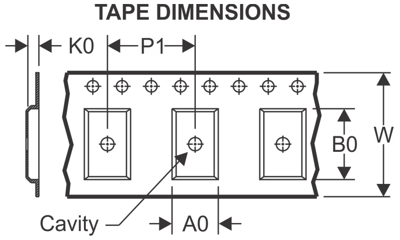
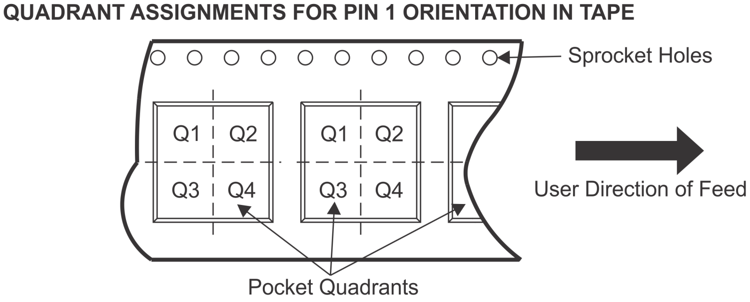




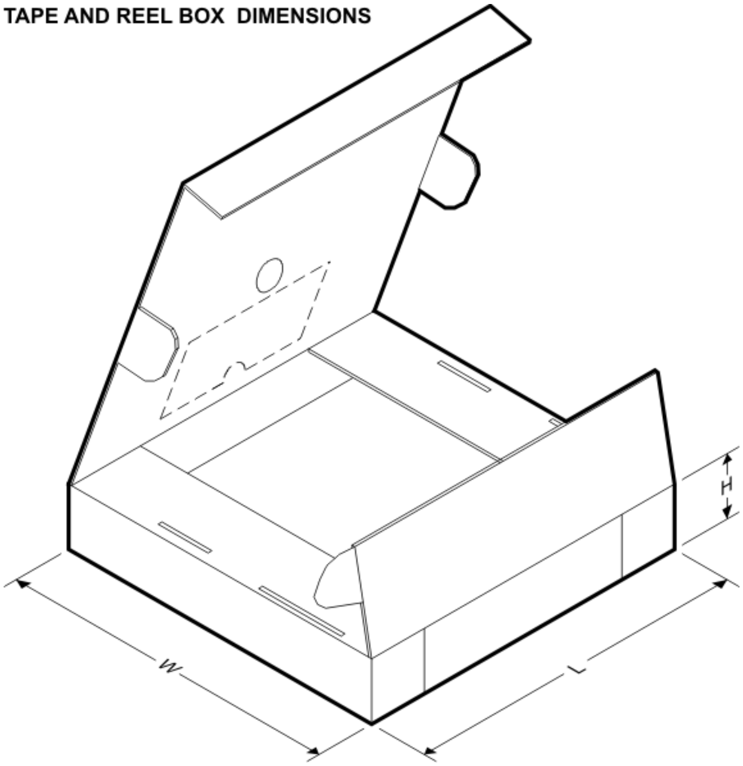
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6511IMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6511IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

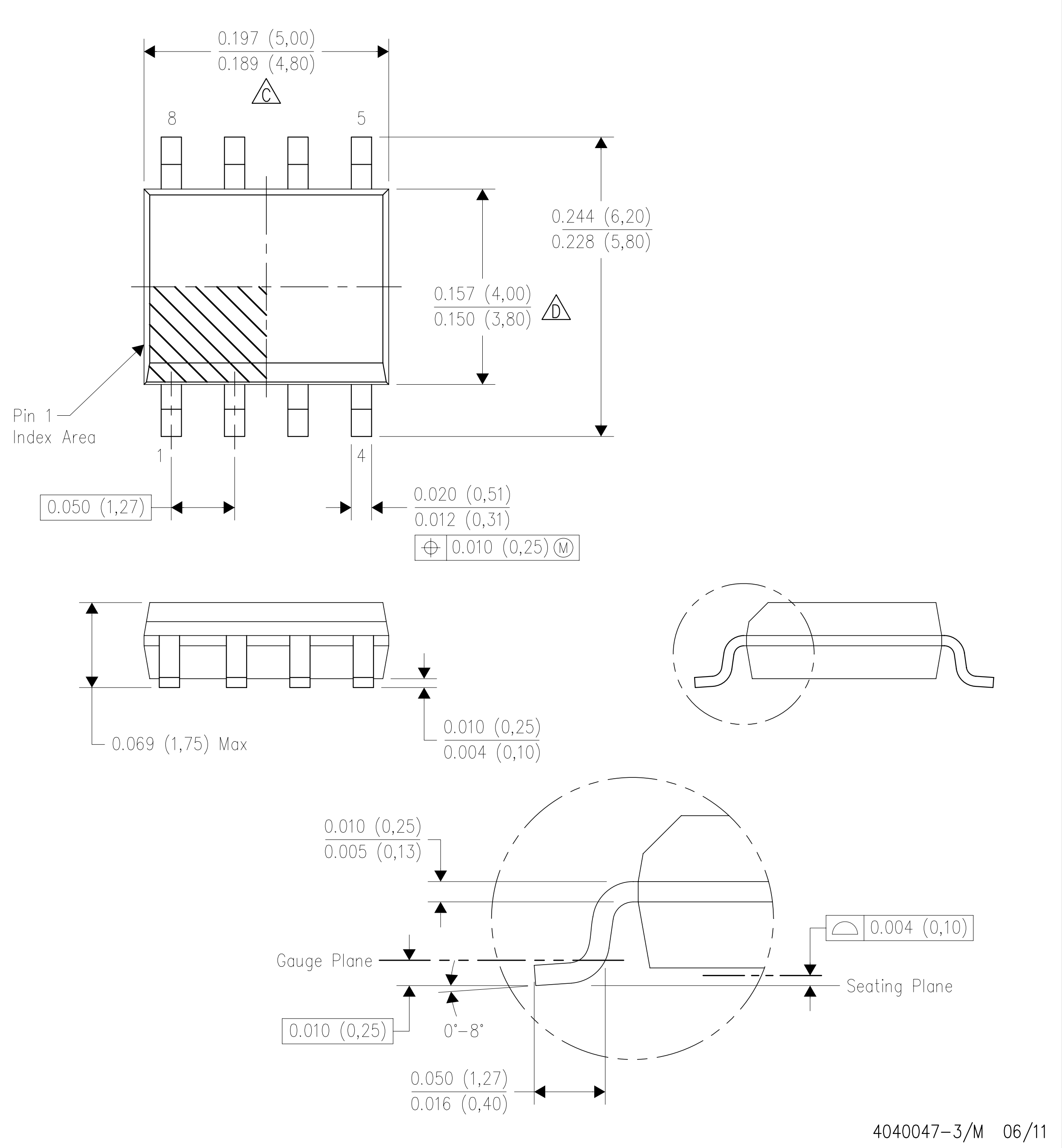
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6511IMX	SOIC	D	8	2500	349.0	337.0	45.0
LM6511IMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

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