Voltage Comparators/Buffers

LM711 dual comparator

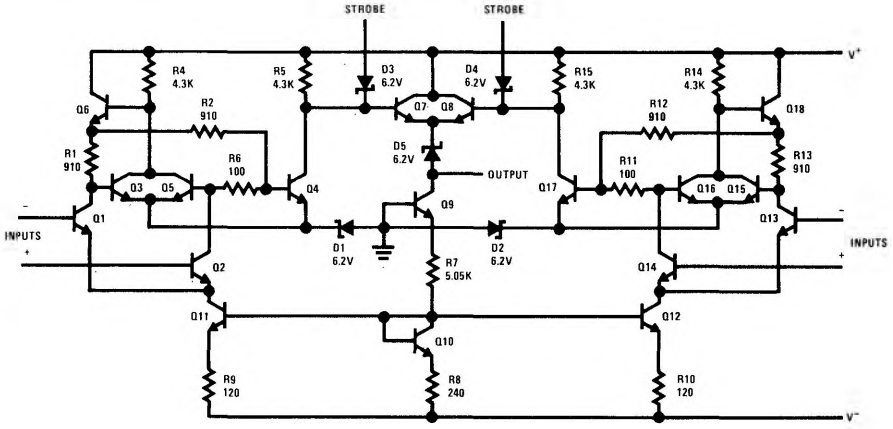
general description

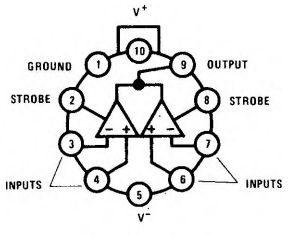
The LM711 contains two voltage comparators with separate differential inputs, a common output and provision for strobing each side independently. Similar to the LM710, the device features low offset and thermal drift, a large input voltage range, low power consumption, fast recovery from large overloads and compatibility with most integrated logic circuits.

With the addition of an external resistor network, the LM711 can be used as a sense amplifier for core memories. The input thresholding, combined with the high gain of the comparator, eliminates many of the inaccuracies encountered with conventional sense amplifier designs. Further, it has the speed and accuracy needed for reliably detecting the outputs of cores as small as 20 mils.

The LM711 is also useful in other applications where a dual comparator with OR'ed outputs is required, such as a double-ended limit detector. By using common circuitry for both halves, the device can provide high speed with lower power dissipation than two single comparators. The LM711 is available in either an 10-lead low profile TO-5 header or a 1/4" by 1/4" metal flat package.

schematic and connection diagrams

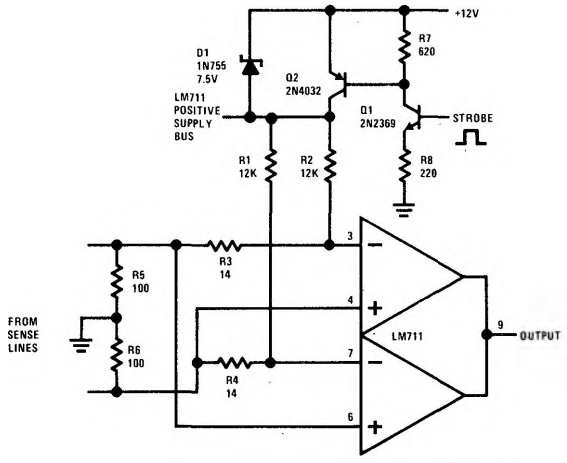




NOTE: Pin 5 connected to case

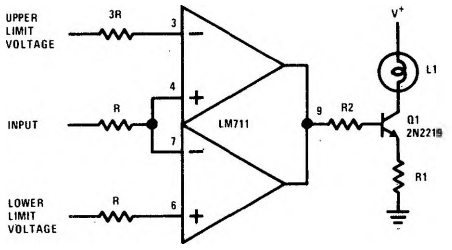
typical applications

Sense Amplifier With Supply Strobing for Reduced Power Consumption*



*Standby dissipation is about 40 mW

Double-Ended Limit Detector With Lamp Driver



absolute maximum ratings

Positive Supply Voltage	+14.0V
Negative Supply Voltage	-7.0V
Peak Output Current	50 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Strobe Voltage	0 to +6.0V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 60 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0$		1.0	3.5	mV
	$R_S \leq 200\Omega$		1.0	5.0	mV
Input Offset Current			0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{IN} \geq 10$ mV, $I_O = 5$ mA	2.5	3.5		V
Negative Output Level	$V_{IN} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3V$	-1.0		0	V
Output Sink Current	$V_{IN} \geq 10$ mV, $V_{OUT} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{STROBE} = 0$		1.2	2.5	mA
Positive Supply Current	$V_{OUT} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage (Note 3)	$R_S \leq 200\Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Average Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

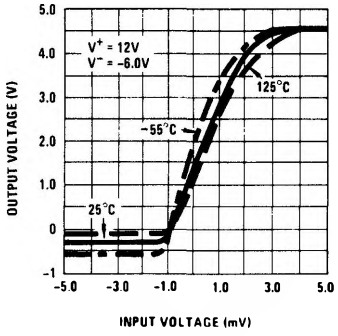
Note 1: For operation at elevated temperatures, the device must be derated based on a 160°C maximum junction temperature and a thermal resistance of 45°C/W junction to case or 150°C/W junction to ambient for the metal-can package. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick, epoxy-glass board with ten, 0.03-inch-wide, 2-ounce copper conductors (see curve).

Note 2: These specifications apply for $V^+ = 12.0V$, $V^- = -6.0V$, $T_A = 25°C$ and for a logic threshold voltage of 1.8V at -55°C, 1.4V at 25°C and 1.0V at 125°C unless otherwise stated.

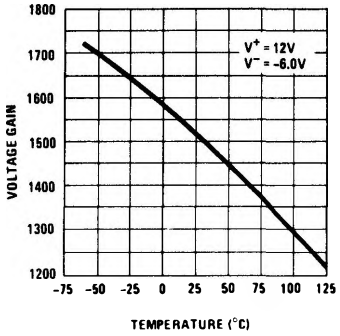
Note 3: The response time specified is for a 100 mV input step with 5 mV overdrive (see definitions).

typical performance characteristics

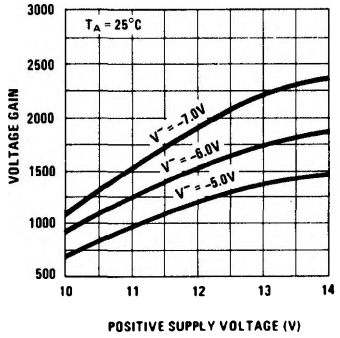
Transfer Function



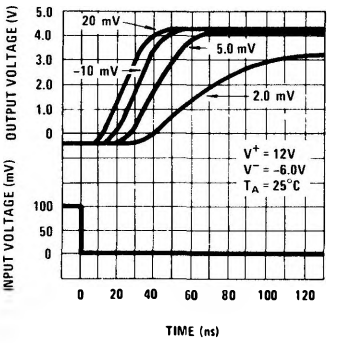
Voltage Gain



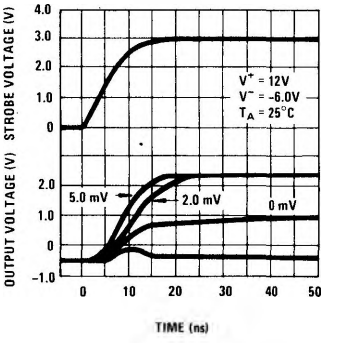
Voltage Gain



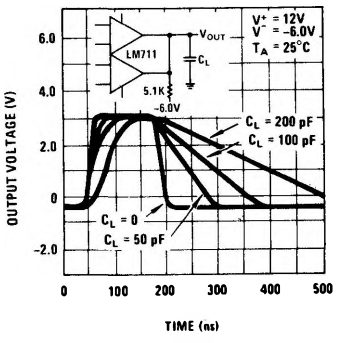
Response Time for Various Input Overdrives



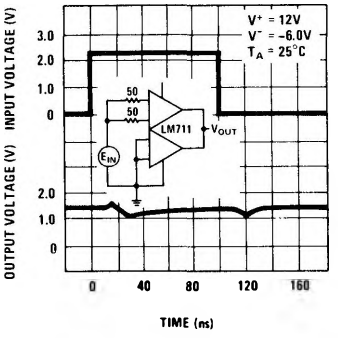
Strobe Release Time for Various Input Overdrives



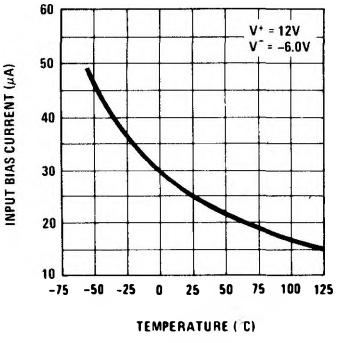
Output Pulse Stretching With Capacitive Loading



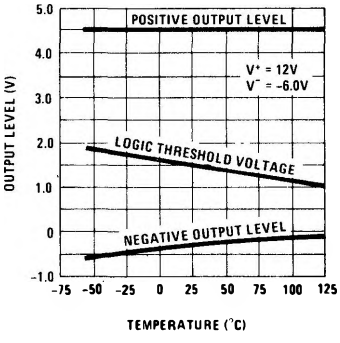
Common Mode Pulse Response



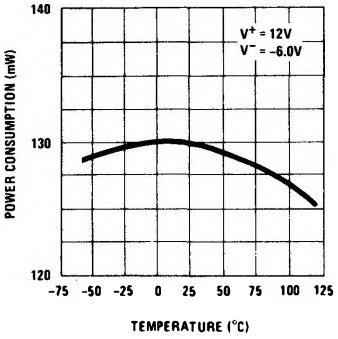
Input Bias Current



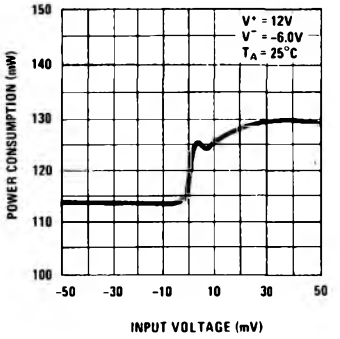
Output Voltage Level



Power Consumption



Power Consumption



Maximum Power Dissipation