LM5538/LM7538 and LM5539/LM7539
electrical characteristics

LM5538/LM5539: The following apply for $-55°C \leq T_A \leq 125°C$, $V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF. INPUT	STROBE INPUT	LOGIC OUTPUT	SUPPLY VOLT.	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5.25V	±5V ±5%	Logic Output <250 μA
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	+20 mA	±5V ±5%	Logic Output <0.4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5.25V	±5V ±5%	Logic Output <250 μA
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V ±5%	Logic Output <0.4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5.25V		±5.25V	
LM7538/LM7539: The following apply for $0°C \leq T_A \leq 70°C$, $V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$										
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5.25V	±5V ±5%	Logic Output <250 μA
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+20 mA	±5V ±5%	Logic Output <0.4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5.25V	±5V ±5%	Logic Output <250 μA
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V ±5%	Logic Output <0.4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5.25V		±5.25V	
LM5538/LM5539: The following apply for $-55°C \leq T_A \leq 125°C$, $V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$ LM7538/LM7539: The following apply for $0°C \leq T_A \leq 70°C$, $V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$										
Diff. Input Offset Current		0.5		μA	0V	0V	+5.25V		±5.25V	
Logic "1" Input Voltage	2			V	40 mV	20 mV	+2V	+20 mA	±4.75V	Logic Output <0.4V
Logic "0" Input Voltage			0.8	V	40 mV	20 mV	+0.8V	+5.25V	±4.75V	Logic Output <250 μA
Logic "0" Input Current		-1	-1.6	mA	40 mV	20 mV	+0.4V		±5.25V	
Logic "1" Input Current		5	40	μA	0V	20 mV	+2.4V		±5.25V	
		0.02	1	mA	0V	20 mV	+5.25V		±5.25V	
Logic "0" Output Voltage		0.25	0.40	V	40 mV	20 mV	+2.0V	+20 mA	±4.75V	
Output Leakage Current		0.01	250	μA	40 mV	20 mV	+0.8V	+5.25V	±4.75V	
V^+ Supply Current		28	38	mA	0V	20 mV	0V		±5.25V	
V^- Supply Current		-13	-18	mA	0V	20 mV	0V		±5.25V	
LM5538/LM5539 and LM7538/LM7539: The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$										
AC Common-Mode Input Firing Voltage		±2.5		V	PULSE	20 mV	+5V	SCOPE		
Propagation Delays:										
Differential Input to Logical "1" Output		24		ns		20 mV				AC Test Circuit
Differential Input to Logical "0" Output		20	40	ns		20 mV				AC Test Circuit
Strobe Input to Logical "1" Output		16		ns		20 mV				AC Test Circuit
Strobe Input to Logical "0" Output		10	30	ns		20 mV				AC Test Circuit
Differential Input Overload Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time		5		ns						
Min. Cycle Time		200		ns						

Note 1: For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5538 and LM5539 are guaranteed the same as LM7538 and LM7539 respectively.

Note 2: Limits in parentheses pertain to LM5539, other limits pertain to LM5538.

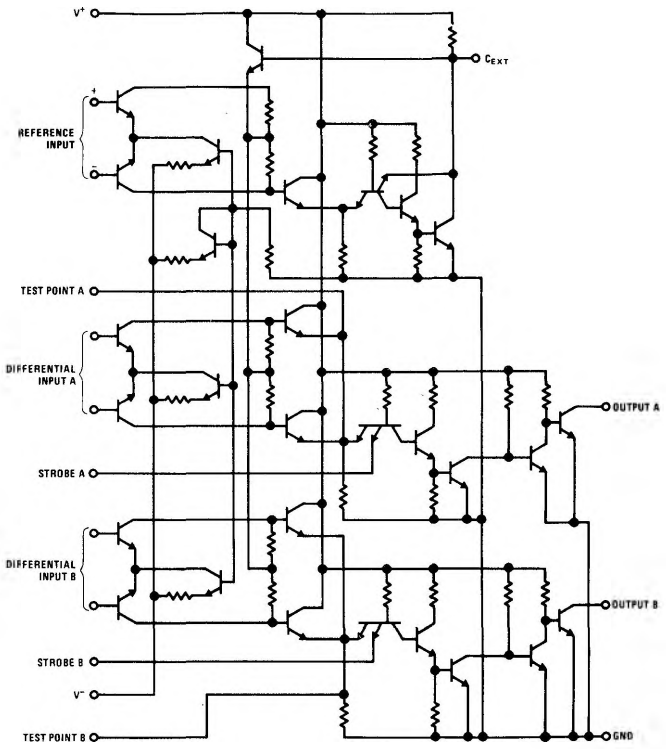
Note 3: Limits in parentheses pertain to LM7539, other limits pertain to LM7538.

Note 4: Positive current is defined as current into the referenced pin.

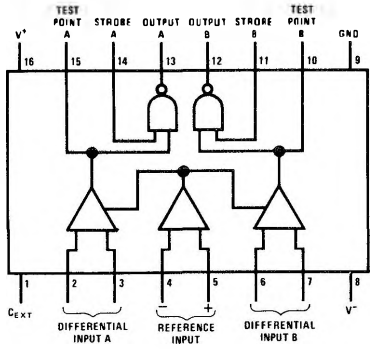
Note 5: Pin 1 to have $\geq$ 100 pF capacitor connected to ground.

Note 6: Each test point to have $\leq$ 15 pF capacitive load to ground.

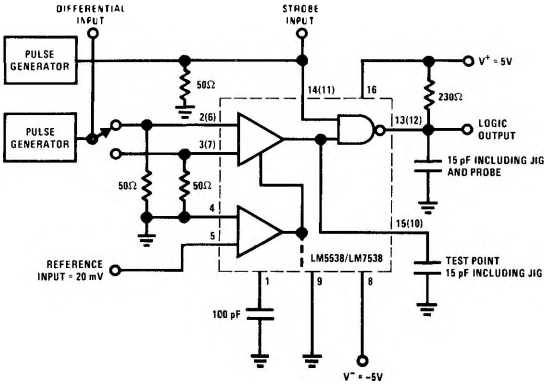
schematic diagram



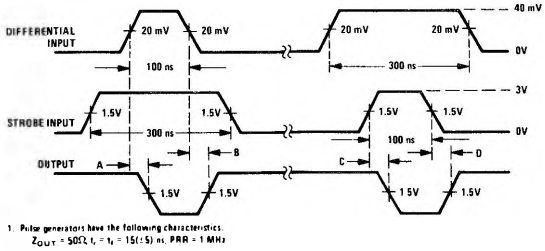
connection diagram



AC test circuit



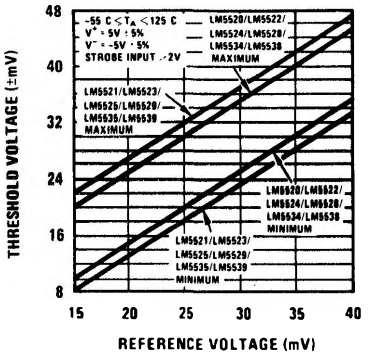
voltage waveforms



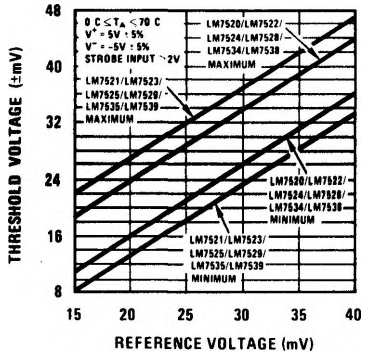
1. Pulse generators have the following characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15(±5) ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "0" output
   B = Differential input to logical "1" output
   C = Strobe input to logical "0" output
   D = Strobe input to logical "1" output

guaranteed performance

Differential Input Threshold Voltage

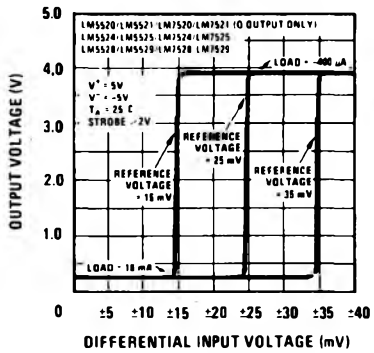


Differential Input Threshold Voltage

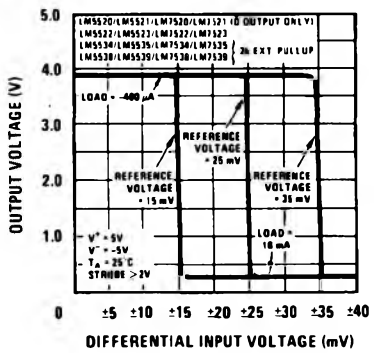


typical performance

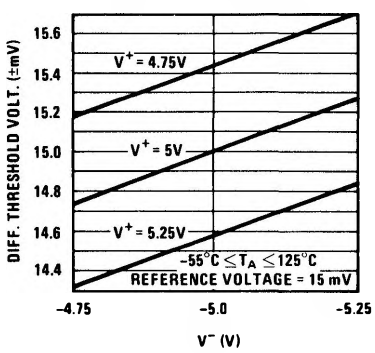
Transfer Characteristics



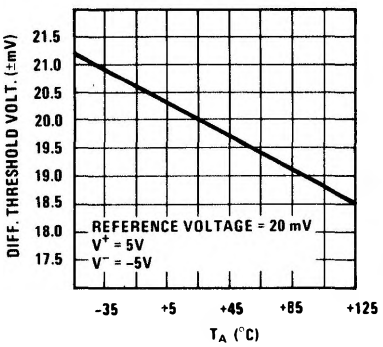
Transfer Characteristics



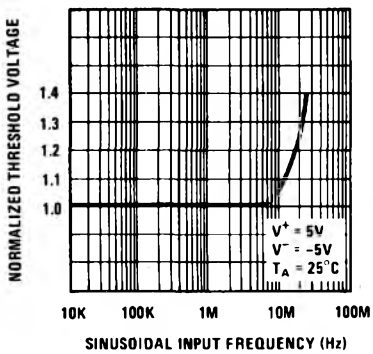
Power Supply Rejection



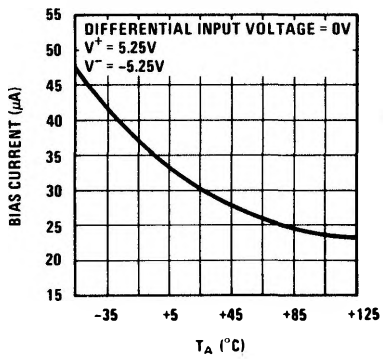
Temperature Coefficient



Differential Input Frequency Response

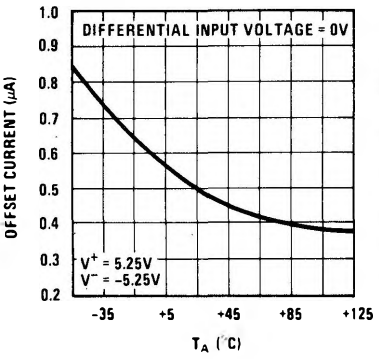


Differential Input Bias Current

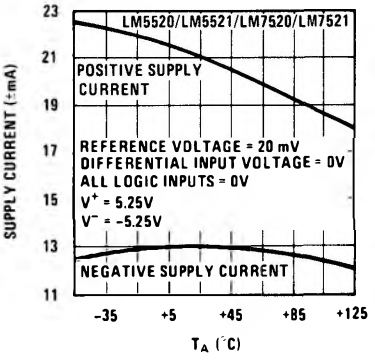


typical performance (cont.)

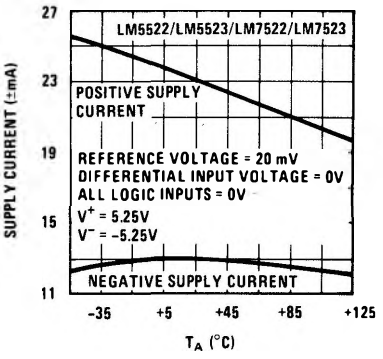
Differential Input Offset Current



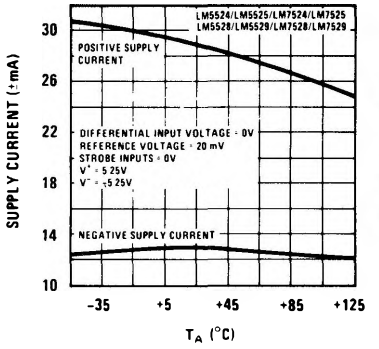
Power Supply Currents



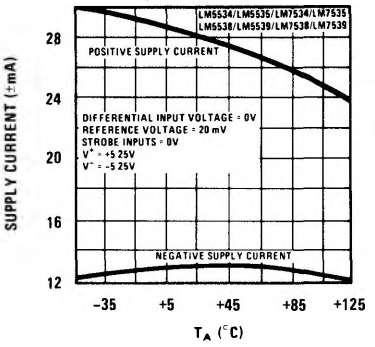
Power Supply Currents



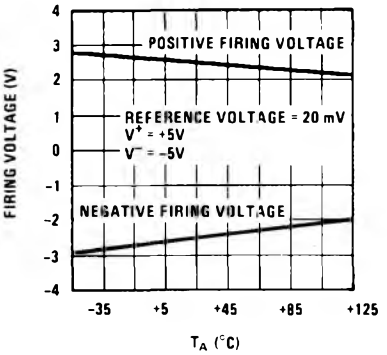
Power Supply Currents



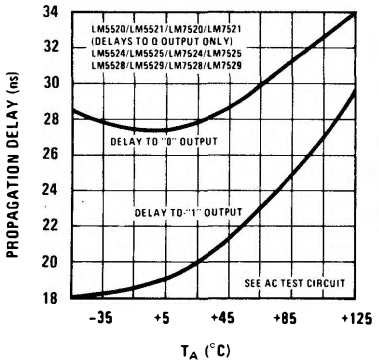
Power Supply Currents



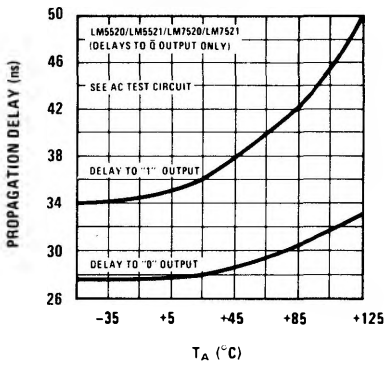
AC Common-Mode Firing Voltage



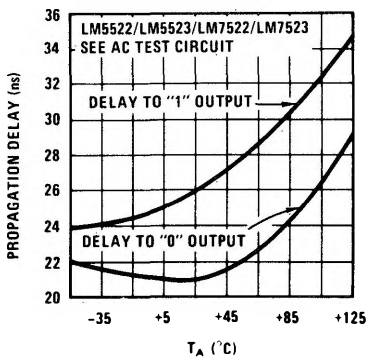
Differential Input to Output Propagation Delays



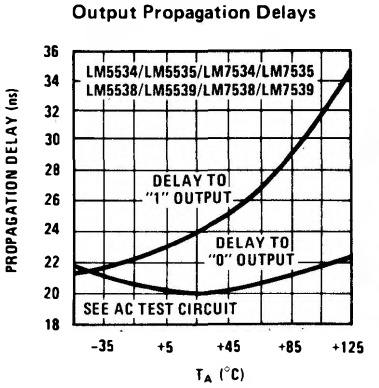
Differential Input to Output Propagation Delays



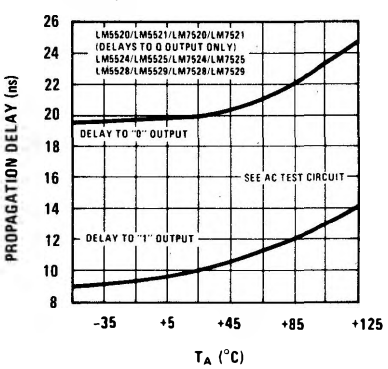
Differential Input to Output Propagation Delays



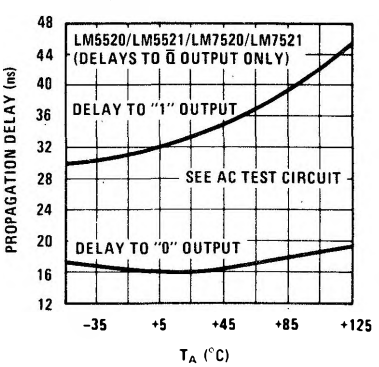
Differential Input to Output Propagation Delays



Strobe to Output Propagation Delays

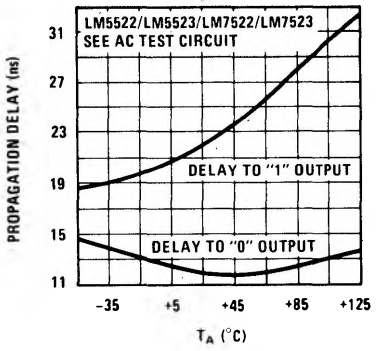


Strobe to Output Propagation Delays

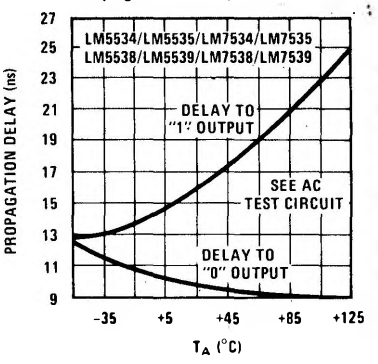


typical performance (cont.)

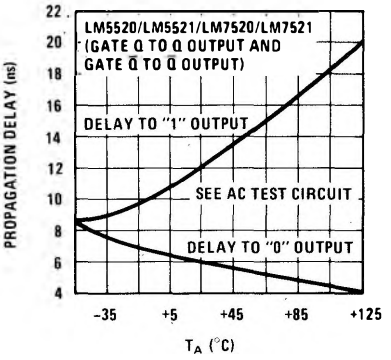
Strobe to Output Propagation Delays



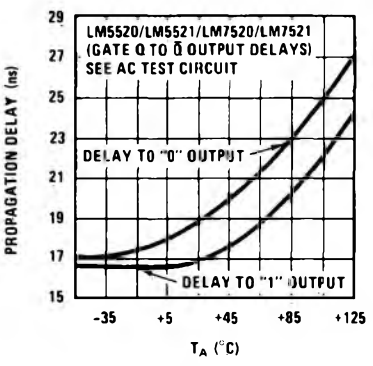
Strobe to Output Propagation Delays



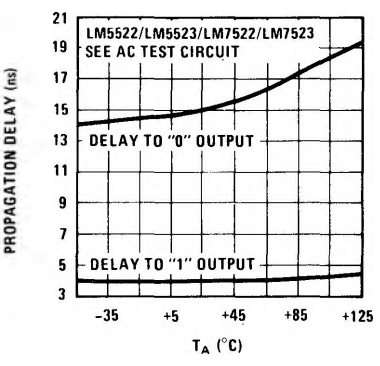
Gate to Output Propagation Delays



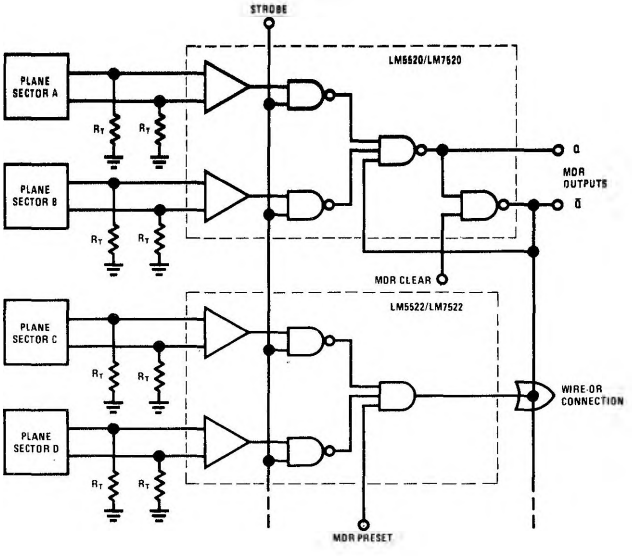
Gate to Output Propagation Delays



Gate to Output Propagation Delays

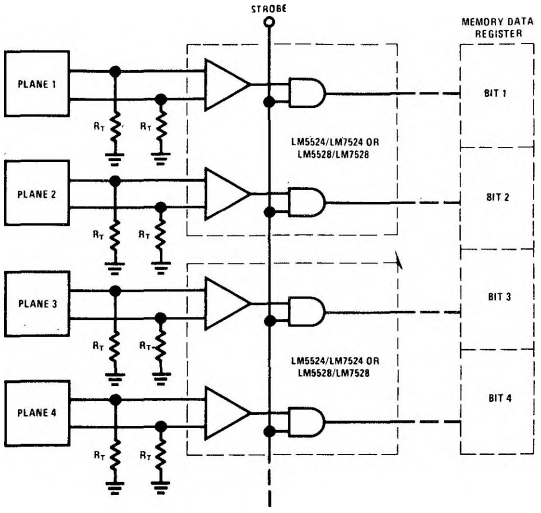


typical applications

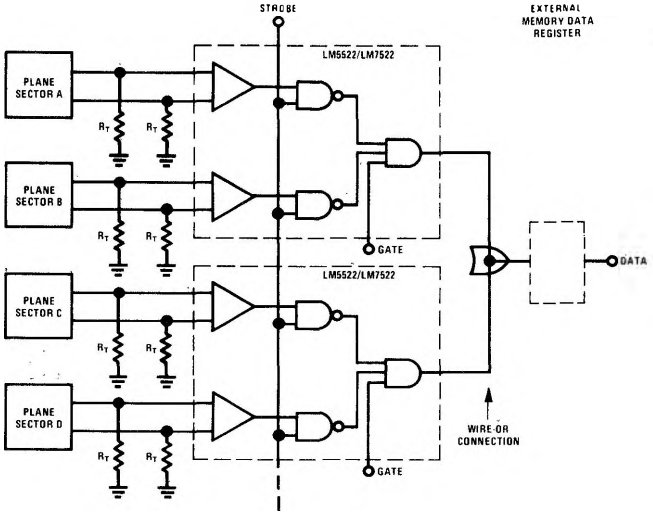


Large Memory System with Sectored Core Planes

typical applications (cont.)



Small Memory System



Large Memory System