National Semiconductor Corporation

ADVANCED INFORMATION

LMC1992/LMC1993 Computer Controlled Tone and Volume Circuits

General Description

The LMC1992/3 is a tone (bass/treble), volume and fader (front/rear) circuit for stereo hi fi audio. Control is accomplished by means of a three wire microprocessor interface. Its applications include car radio, TV and remote audio systems.

The LMC1992/3 provides stereo source selection switching, volume, fade and tone controls with very few external components. On-chip op amps enable these functions to be accomplished in a 28-pin package with minimal external components. In addition, the LMC1993 provides a loudness function with one less input source per channel.

The LMC1992/3 was designed with most capacitors less than 0.1 μF to allow use of chip capacitors. The signal path is comprised of analog switches and thin-film silicon-chromium resistor networks for very low noise and distortion. Additional tone control can be included by use of LMC843/835 digitally-controlled stereo 3/7-band graphic equalizer circuits.

Features

- 28-pin package
- Low noise and distortion
- Serial programmable: standard MICROWIRE™ interface
- Protection address (similar to DS 8906)
- TTL, CMOS logic compatible
- Inputs DC coupled
- Full boost and cut treble and bass tone control
- 40 Volume levels including mute
- Front/back fade control
- 20 Fader levels
- All attenuators 2 dB/step
- Single supply operation
- Wide supply voltage range
- Minimal external components
- Provisions for connection to DNR® and/or equalizer
- LMC1992 has 4 stereo source selection without loudness, LMC1993 has 3 with loudness
- Provisions for more stereo inputs
- Powers up with flat tone and min volume/fader

Equivalent Schematic (one channel shown) [LMC1993-loudness device]

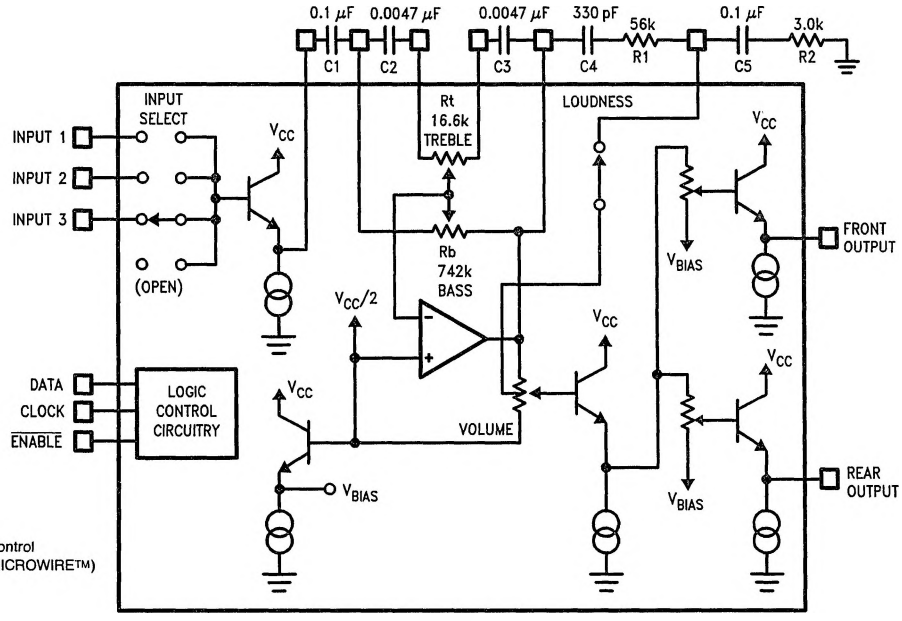

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FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage $+V_S$ Referred to $-V_S$ Ground	$+18V$
Maximum Operational Supply Voltage	$+15V$
Logical Input Voltage	$+V_S$, $-V_S$
Operating Temperature Range LMC1992, LMC1993	$T_{MIN} < T_A < T_{MAX}$ $-40°C$ to $+85°C$
Storage Temperature Range	$-60°C$ to $+150°C$
Maximum Junction Temperature	125°C
Lead Temperature (Soldering, 10 sec.)	300°C

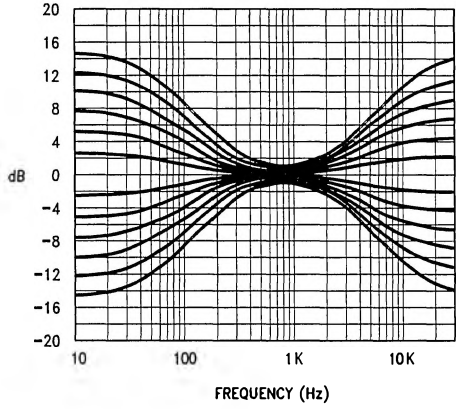
ESD rating is to be determined.

Electrical Characteristics $V^+ = 8V$, $T_A = +25°C$ unless otherwise noted

Parameter	Conditions Volume = 0 dB, Faders = 0 dB unless specified	LMC1992			Units
		Typ	Tested Limit	Design Limit	
Supply Current		15			mA
Reference Voltage	Pin 27	4.7			Vdc
Maximum Input Signal	Clipping Level (1% THD)	2.3			Vrms
Maximum Output Signal	Clipping Level (1% THD)	1.0			Vrms
THD 1 kHz	0.3 Vrms Input Volume = 0 dB	0.2			%
THD 1 kHz	0.3 Vrms Input Volume = −20 dB	0.03			%
Max Noise	CCIR, Flat Tone, Volume = 0 dB	7.0			μVrms
Min Noise	CCIR, Flat Tone, Volume = −80 dB	4.5			μVrms
Bass Range	Boost and Cut @ 50 Hz	12			±dB
Treble Range	Boost and Cut @ 15 kHz	12			±dB
Volume Range	Maximum Attenuation	80			dB
Fader Range	Maximum Attenuation	40			dB
Tracking	Attenuator Tracking	0.5			dB
Freq Response	High Frequency − 1 dB point	450			kHz
Separation	Channel Separation 1 kHz	80			dB
Isolation	Input-Input Isolation	90			dB
PSRR	100 Hz, 200 mVrms	40			dB
F_{clk}	Maximum Clock Frequency	1.0		0.50	MHz

Typical Performance Characteristics

Bass Max Treble Max / Bass Min Treble Min



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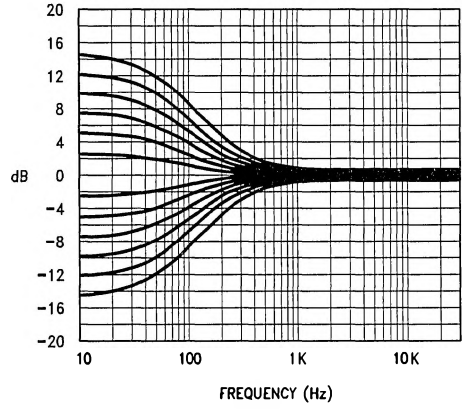
Bass Max Treble Flat / Bass Min Treble Flat



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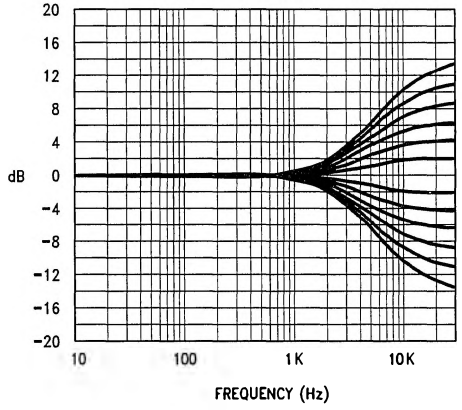
Bass Flat Treble Max / Bass Flat Treble Min



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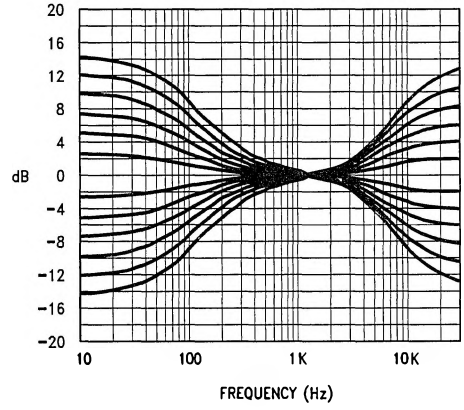
Bass Min Treble Max / Bass Max Treble Min



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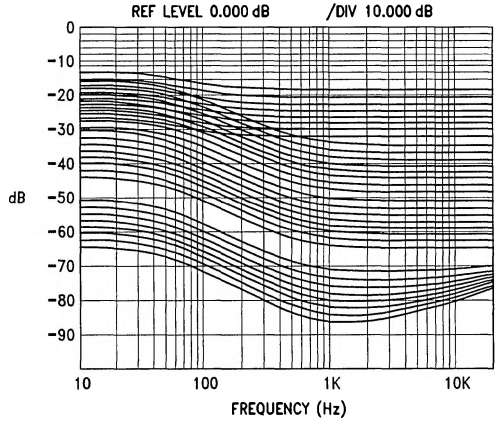
Loudness Contours LMC1993 Only



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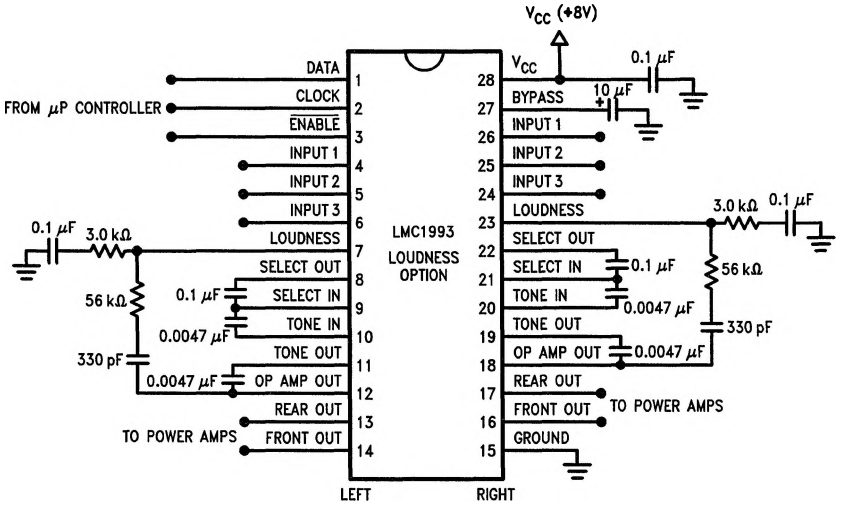
Note: Above graphs are tentative and thus subject to change.

Typical Applications



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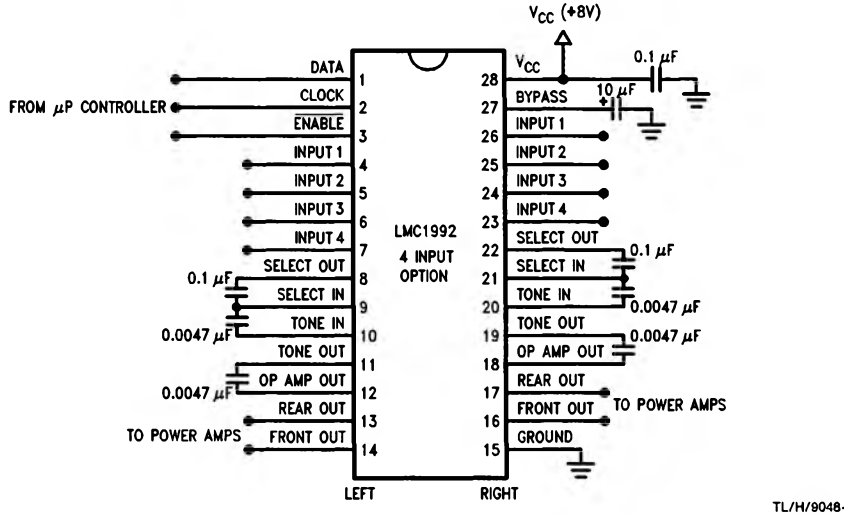

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FIGURE 7. Connection Diagrams Options with Minimal External Components
Order Number LMC1993 (loudness device), LMC1992 (4 input device)
See NS Package Number N28B

General Information

The LMC1992/3 is a CMOS/bipolar high quality building block intended for high fidelity audio signal processing. While the LMC1992/3 is manufactured with CMOS processing, unique NPN transistors exist which are used to build low noise op amps. The combination of CMOS switches, bipolar op amps and sichrome resistors make it possible to achieve an order of magnitude quality improvement over standard bipolar circuits.

The LMC1992/3 has internal logic decoding which allows a computer (μP) to communicate directly to the audio control circuitry through a standard MICROWIRE interface. This 3 wire interface consists of DATA input line, a CLOCK input line, and an $\overline{\text{ENABLE}}$ line. When the $\overline{\text{ENABLE}}$ line is low, data can be shifted (serially) from the controller into the audio control circuit. As the $\overline{\text{ENABLE}}$ line goes through the low to high transition, data entry is disabled and data present in the internal shift register is latched and the instruction is executed.

From the controller 11 bit serial data stream, the first two bits address the device (LMC1992/3) permitting other devices (ie: PLL, equalizer) to share the same 3 wire bus. Of the remaining 9 bits, the next 3 bits are used for the function select (ie: volume, fader . . .). The remaining 6 bits are data for the function being addressed.

Serial Data Entry into the LMC1992/3

Serial information entry into the LMC1992/3 is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One bit is accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low preceding the negative transition of the $\overline{\text{ENABLE}}$ input.

The first two bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as an address. If these bits are **not** 1,0 no further information will be accepted from the DATA input, while the data latches will remain unchanged when the $\overline{\text{ENABLE}}$ line returns high.

If the first two bits are 1,0 then all succeeding bits are accepted as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Application Hints—Digital

In addition, a 12 bit data stream can be used if needed. The first two bits and last nine bits remain the same while any number of don't care bits can be inserted preceding the MSB of the three bit function select. Since these don't care bits are just shifted out internally, any number can be inserted to allow ease of programming. Thus the data stream word length becomes simply 11 + (number of extra bits).

When the $\overline{\text{ENABLE}}$ input returns high, any further serial data input is inhibited. Upon this positive transition of the $\overline{\text{ENABLE}}$, the data in the internal shift register is transferred into the data latches. Note that until this time, the states of the internal data latches have remained unchanged.

SERIAL DATA FORMAT

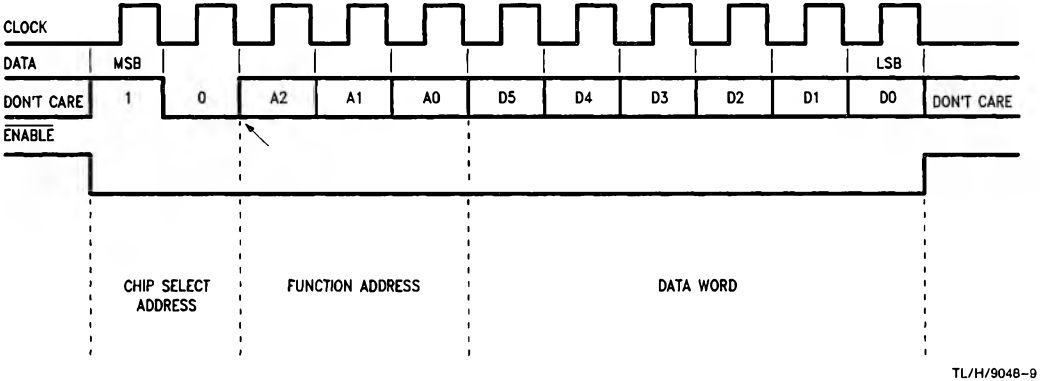
The serial data format, bit assignment and sequence is shown in Table I. Not shown in Table I are the protection address bits (1, 0) which as discussed earlier must precede the nine bit data word.

Note that not all the allotted data bits are used for all functions excluding volume. The extra bits are denoted with an "X" for don't care. Even though these extra bits have no effect on their respective controls, they still must be clocked into the LMC1992/3 for proper operation. Otherwise erroneous results will occur.

DATA COMMUNICATION

The following routines apply to operation of the LMC1992/3 with COPS™ microcontrollers. The routines arbitrarily select register 0 as the I/O register. It is assumed that chip select is high, SK (clock) is low, and SO (data) is low on entry to the routines. The routines exit with chip select high, SK low and SO low. Output port G0 is arbitrarily chosen as the chip select for the external device.

The 11 data bits intended to control the LMC1992/3 are assumed to be in the 4 bit registers 13–15 with the 4 MSB bits in register 13. This provides an extra bit (which works fine also) resulting in a data stream 12 bits long.



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Note 1: Negative transition on $\overline{\text{ENABLE}}$ clears previous address. Clock must be low during transition.

Note 2: Additional don't care states may be inserted here for ease of programming. (Optional.)

Note 3: Positive transition on $\overline{\text{ENABLE}}$ latches in new data if the LMC1992/3 has been addressed. Clock can either be high or low during transition.

FIGURE 8. Clocking Data into the Standard MICROWIRE Interface (Minimum Number of Bits in Data Stream)

Applications Hints-Digital (Continued)

DESTRUCTIVE DATA OUTPUT

This routine outputs the data under the conditions specified above. The output data is destroyed after it is transmitted. Note that this is a general purpose routine and handles all the overhead except loading the data into the registers. The routine takes a total of 17 ROM words and can be undoubtedly be reduced in specific applications.

```
OUT1:   LBI    0,13     ;point to start of data word
        SC              ;set C to enable SK clock
        OGI    14       ;select external device G0=0
        LEI    8        ;enable shift register output
SEND:   LD
        XAS             ;data transmission loop
        XIS             ;turn on clock
        JP     SEND
        RC
        XAS    15       ;deselect external device
        LEI    0        ;set S0 to 0
        RET
```

NON DESTRUCTIVE DATA OUTPUT

This routine is identical to the destructive data routine except that the transmitted data is preserved in the microcontroller. The nondestructive routine takes 21 ROM words. Four more than the destructive routine. Again this is a general purpose routine which can probably be reduced in specific applications.

```
OUT2:   LBI    0,13     ;point to start of data word
        SC
        OGI    14       ;select external device G0=0
        LEI    8        ;enable shift register output
        JP     SEND2
SEND1:XAS
SEND2:  LD              ;data output loop
        XIS
        JP     SEND 1
        XAS              ;send last data
        RC               ;wait 4 cycles-data going out
        CLRA
        NOP
        XAS              ;turn SK clock off
        OGI    15        ;deselect device
        LEI    0         ;set S0 to 0
        RET
```

Note: These routines are tentative and subject to change.

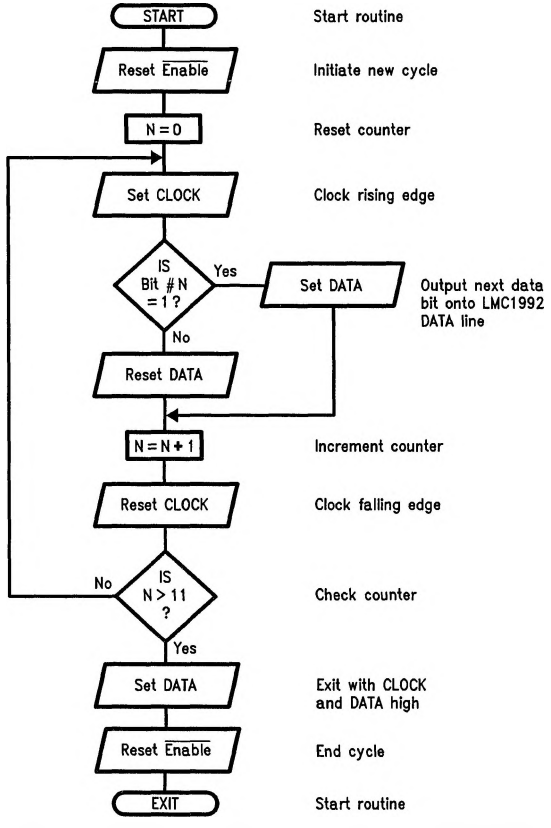

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FIGURE 9. General Flowchart for Controlling LMC1992/3 MICROWIRE Serial Inputs

Application Hints-Digital (Continued)

TABLE I. Programming Codes for LMC1992/3

Address			Function	Data						Values
A2	A1	A0		D5	D4	D3	D2	D1	D0	
1	1	1	Left Rear Fader	X	M	N	N	N	L	−40 dB = X00000 −20 dB = X01010 0 dB = X101XX
1	1	0	Right Rear Fader	X	M	N	N	N	L	−40 dB = X00000 −20 dB = X01010 0 dB = X101XX
1	0	1	Left Front Fader	X	M	N	N	N	L	−40 dB = X00000 − 20 dB = X01010 0 dB = X101XX
1	0	0	Right Front Fader	X	M	N	N	N	L	−40 dB = X00000 −20 dB = X01010 0 dB = X101XX
0	1	1	Volume	M	N	N	N	N	L	−80 dB = 000000 −40 dB = 010100 0 dB = 101XXX
0	1	0	Treble	X	X	M	N	N	L	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	1	Bass	X	X	M	N	N	L	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	0	Input Select & LOUDNESS	X	X	I	M	N	L	OPEN = XXI000 INPUT1 = XXI001 INPUT2 = XXI010 INPUT3 = XXI011 INPUT4 = XXI100 *(see note) LOUDNESS ON: I = 1 *(see note) LOUDNESS OFF: I = 0

***Note 1:** With LMC1993 loudness device, INPUT 4 is not available.

***Note 2:** With LMC1992 4 input device, D3 of input select must be low (0), and INPUT 4 is available.

Note 3: M & L represent most and least significant data bits.

Note 4: All attenuators 2 dB/step.

Note 5: Tone controls 2 dB/step @ 50 Hz and 15 kHz.

Application Hints—Analog

INPUT CHANNEL SELECTION

When operating from a single positive power supply, the LMC1992/3 signal inputs require a DC bias voltage for proper operation of the internal voltage followers and buffers. This usually means that the signal sources, if operated off the same single supply, can be directly coupled to the LMC1992/3 without a coupling capacitor. For example, on an 8 Vdc power supply, all signal inputs to the LMC1992/3 (pins 4–6, 24–26) should have a DC component of approximately 4 Vdc. Maximum signal levels of 2 Vrms (5.6V peak-to-peak) would then swing from 1.2V to 6.8V.

For signal sources lacking in this requirement, such as those derived from external input jacks to the system, the bias voltage needs to be provided. A simple voltage divider with filter for supply rejection as shown in *Figure 10* will suffice.

When the LMC1993 is used, input 4 is not available. That pin becomes the loudness input. Selecting input 4 when using the LMC1993, or turning on the loudness function when the LMC1992 is used can cause undesirable results, thus is not suggested.

For best results, a separate bias circuit for each channel or even one for each signal source lacking a DC component should be used to prevent crosstalk between channels and inputs. Though stereo sources can have bias circuits in common for left and right signal and still maintain reasonable separation.

Depending upon the particular input source that is selected, one of the three stereo inputs will be available at the select output pins 8 and 22 (left and right channels respectively). The DC bias voltage at those pins will be one base-emitter voltage (approximately 0.7 Vdc) below the source due to the internal emitter follower (see *Figure 1*). Thus, if the selected input has a bias of 4.0 Vdc the DC component at pins 8 and 22 will be about 3.3 Vdc.

The use of an emitter follower for input selection allows connection of additional sources to the system. For example, many radio IC's also have emitter follower outputs that allow the user to wire-or multiple outputs together and control their selection by input or supply switching. The signal output pin 8 and 22 of the LMC1992/3 are constructed similarly and may be treated in the same manner, consistent with the same requirements. If another emitter follower output is driving these nodes, the LMC1992/3 input select should be switched to either "XXX000" or "XXX11X" open input codes (see Table I).

The select output pins 8 and 22 may be directly coupled via a capacitor to the select input (pins 9 and 21) as shown in *Figure 1* or connected to external noise reduction and/or equalizer circuits as shown in *Figure 11*. Should both be utilized, it is important that noise reduction (ie: DNR® using the LM1894) be performed before equalization. Otherwise, the equalization control settings could adversely affect or even prevent the noise reduction systems from operating.

The input select switch can also be used as a mute function with volume at −80 dB, the input select can be set to "XXX000" open input to further mute the outputs to provide greater than −100 dB attenuation if desired.

TONE RESPONSE

The tone function (bass and treble) is controlled by capacitors C1 and C2 (see *Figure 1*). The exact amount of boost and cut obtained is determined by the data word as given in Table I.

The typical tone response obtained in the standard application circuit (C2 = C3 = 0.0047 μF) is shown in *Figures 2–5* for each step of boost and cut. When modifying these curves it is important to note that it is ratio of C3 to C2 that determines the mid frequency gain. For example, with C3 = 2(C3) the tone response at "flat" setting would be approximately 0 dB at 20 Hz and 20 kHz while +6 dB at 1 kHz. Thus C2 should equal C3 for a symmetric tone response.

The effect of altering the recommended values of the tone shaping capacitors C2 and C3 is to shift the tone response curve up or down in frequency. By increasing the capacitance of C2 and C3, the frequencies at which 2 dB/step is achieved will decrease from 50 Hz to 35 Hz and from 15 kHz to 10 kHz with a 0.0068 μF capacitor. Likewise with a decrease in capacitance of C2 and C3 the 2 dB/step frequencies will increase from 50 Hz to 70 Hz and from 15 kHz to 20 kHz with a 0.0033 μF capacitor.

From *Figure 1* the turnover frequencies are approximately F_{hb} = 1/sC2(13.8K) and F_{lb} = 1/sC1(116.4K) for treble and bass respectively at maximum boost. While the inflection frequencies (at which maximum boost and cut are within 3 dB of their final values) are F_h = 1/sC2(2.6K) and F_l = 1/sC1(625.6K) for treble and bass respectively at maximum boost.

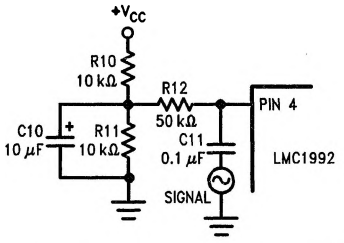

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FIGURE 10. DC Bias Input Circuit

LOUDNESS FUNCTION—LMC1993 ONLY

The loudness compensation as shown in *Figure 1* is controlled by components R1, R2, C4, C5. If selected it will introduce bass and slight treble boost (in addition to any tone shaping requested) that is dependent upon the setting of the volume control. The exact nature of the transfer function at −34 dB is given by:

$$\frac{V_o}{V_i} = \frac{1}{4.67} \frac{(s*C5*R2+1)*(s*C4*(R1+112K)+1)}{(s*C4*R1+1)*(s*C5*(R5+41.34K)+1)}$$

If only bass boost is required the external components R1 and C4 can be deleted, minimizing the external component count.

If this device is selected only three inputs will be available to input select (input 1–input 3). For systems where loudness compensation is not required the user may choose the LMC1992 or simply eliminate the components associated with the loudness pin and being careful when programming to always keep the loudness function off (see Table I).

The data bit used to enable or disable the loudness function is embedded in the input data select data word as D3. Thus care must be taken to send a complete data word (loudness on/off and input select data) in order to prevent erroneous operation.

FADER FUNCTION

Since all four fader outputs LR, LF, RR, RF are all independently adjustable, a balance control would be redundant. The balance function is accomplished via software by simultaneously changing both front and rear faders on the same channel by the desired amount of balance. Since 40 dB of attenuation is available this should satisfy most any balance requirements.

SYSTEM CONNECTION

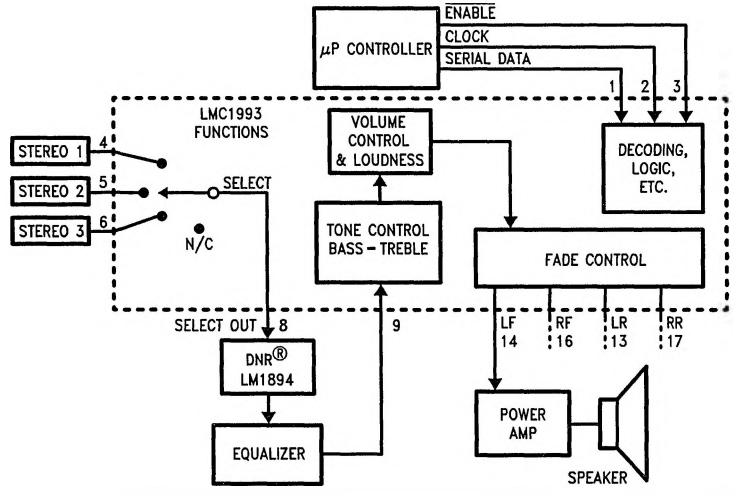

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FIGURE 11. System Block Diagram Showing Inclusion of DNR® Noise Reduction and Equalizer (LMC843, LMC835) (One Channel Only—LMC1993).