August 2000

National Semiconductor

# LMC555
# CMOS Timer

## General Description

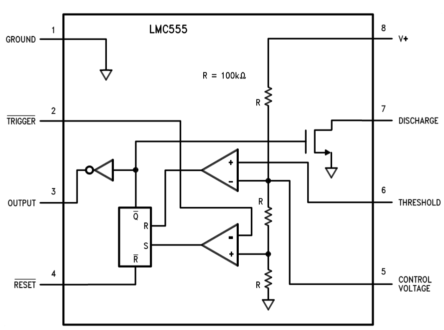
The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. In addition to the standard package (SOIC, MSOP, and MDIP) the LMC555 is also available in a chip sized package (8 Bump micro SMD) using National's micro SMD package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the stable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of National Semiconductor's LMCMOS™ process extends both the frequency range and low supply capability.

## Features

- Less than 1 mW typical power dissipation at 5V supply
- 3 MHz astable frequency capability
- 1.5V supply operating voltage guaranteed
- Output fully compatible with TTL and CMOS logic at 5V supply
- Tested to −10 mA, +50 mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers
- Available in 8 pin MSOP Package and 8-Bump micro SMD package

## Block and Connection Diagrams

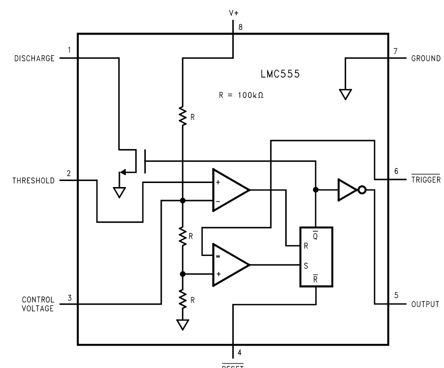
**8-Pin SOIC, MSOP, and MDIP Packages**




DS008669-1

**Top View**

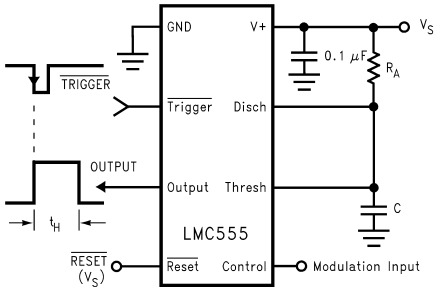
**8-Bump micro SMD**



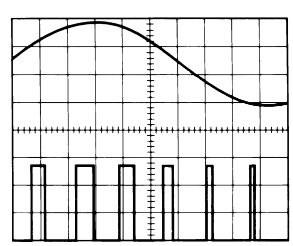

DS008669-9

**Top View (bump side down)**

## Pulse Width Modulator




DS008669-20



DS008669-15

LMCMOS™ is a trademark of National Semiconductor Corp.

## Ordering Information

| Package | Temperature Range<br>Industrial<br>−40˚C to +85˚C | Package Marking | Transport Media | NSC Drawing |
|---|---|---|---|---|
| 8-LeadSmall Outline (SO) | LMC555CM | LMC555CM | Rails | M08A |
| | LMC555CMX | LMC555CM | 2.5k Units Tape and Reel | |
| 8-Lead Mini Small Outline (MSOP) | LMC555CMM | ZC5 | 1k Units Tape and Reel | MUA08A |
| | LMC555CMMX | ZC5 | 3.5k Units Tape and Reel | |
| 8-Lead Molded Dip (MDIP) | LMC555CN | LMC555CN | Rails | N08E |
| 8-Bump micro SMD | LMC555CBP | F1 | 250 Units Tape and Reel | BPA08EFB |
| | LMC555CBPX | F1 | 3k Units Tape and Reel | |
| Metronome Circuit | LMC555CBPEVAL | N/A | N/A | N/A |

## Absolute Maximum Ratings (Notes 2, 3)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, $V^+$ | 15V |
| Input Voltages, $V_{TRIG}$, $V_{RES}$, $V_{CTRL}$, $V_{THRESH}$ | −0.3V to $V_S$ + 0.3V |
| Output Voltages, $V_O$, $V_{DIS}$ | 15V |
| Output Current $I_O$, $I_{DIS}$ | 100 mA |
| Storage Temperature Range | −65˚C to +150˚C |
| Soldering Information | |
| MDIP Soldering (10 seconds) | 260˚C |
| SOIC, MSOP Vapor Phase (60 sec) | 215˚C |
| SOIC, MSOP Infrared (15 sec) | 220˚C |

**Note:** See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Operating Ratings (Notes 2, 3)

| | |
|---|---|
| Termperature Range | −40˚C to +85˚C |
| Thermal Resistance ($\theta_{JA}$) (Note 2) | |
| SO, 8-lead Small Outline | 169˚C/W |
| MSOP, 8-lead Mini Small Outline | 225˚C/W |
| MDIP, 8-lead Molded Dip | 111˚C/W |
| 8-Bump micro SMD | 220˚C/W |
| Maximum Allowable Power Dissipation @25˚C | |
| MDIP-8 | 1126mW |
| SO-8 | 740mW |
| MSOP-8 | 555mW |
| 8 Bump micro SMD | 568mW |

## Electrical Characteristics (Notes 1, 2)

Test Circuit, T = 25˚C, all switches open, $\overline{\text{RESET}}$ to $V_S$ unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units (Limits) |
|---|---|---|---|---|---|---|
| $I_S$ | Supply Current | $V_S$ = 1.5V<br>$V_S$ = 5V<br>$V_S$ = 12V | | 50<br>100<br>150 | 150<br>250<br>400 | µA |
| $V_{CTRL}$ | Control Voltage | $V_S$ = 1.5V<br>$V_S$ = 5V<br>$V_S$ = 12V | 0.8<br>2.9<br>7.4 | 1.0<br>3.3<br>8.0 | 1.2<br>3.8<br>8.6 | V |
| $V_{DIS}$ | Discharge Saturation Voltage | $V_S$ = 1.5V, $I_{DIS}$ = 1 mA<br>$V_S$ = 5V, $I_{DIS}$ = 10 mA | | 75<br>150 | 150<br>300 | mV |
| $V_{OL}$ | Output Voltage (Low) | $V_S$ = 1.5V, $I_O$ = 1 mA<br>$V_S$ = 5V, $I_O$ = 8 mA<br>$V_S$ = 12V, $I_O$ = 50 mA | | 0.2<br>0.3<br>1.0 | 0.4<br>0.6<br>2.0 | V |
| $V_{OH}$ | Output Voltage (High) | $V_S$ = 1.5V, $I_O$ = −0.25 mA<br>$V_S$ = 5V, $I_O$ = −2 mA<br>$V_S$ = 12V, $I_O$ = −10 mA | 1.0<br>4.4<br>10.5 | 1.25<br>4.7<br>11.3 | | V |
| $V_{TRIG}$ | Trigger Voltage | $V_S$ = 1.5V<br>$V_S$ = 12V | 0.4<br>3.7 | 0.5<br>4.0 | 0.6<br>4.3 | V |
| $I_{TRIG}$ | Trigger Current | $V_S$ = 5V | | 10 | | pA |
| $V_{RES}$ | Reset Voltage | $V_S$ = 1.5V (Note 4)<br>$V_S$ = 12V | 0.4<br>0.4 | 0.7<br>0.75 | 1.0<br>1.1 | V |
| $I_{RES}$ | Reset Current | $V_S$ = 5V | | 10 | | pA |
| $I_{THRESH}$ | Threshold Current | $V_S$ = 5V | | 10 | | pA |
| $I_{DIS}$ | Discharge Leakage | $V_S$ = 12V | | 1.0 | 100 | nA |
| t | Timing Accuracy | SW 2, 4 Closed<br>$V_S$ = 1.5V<br>$V_S$ = 5V<br>$V_S$ = 12V | <br>0.9<br>1.0<br>1.0 | <br>1.1<br>1.1<br>1.1 | <br>1.25<br>1.20<br>1.25 | ms |
| $\Delta t/\Delta V_S$ | Timing Shift with Supply | $V_S$ = 5V ± 1V | | 0.3 | | %/V |
| $\Delta t/\Delta T$ | Timing Shift with Temperature | $V_S$ = 5V<br>−40˚C ≤ T ≤ +85˚C | | 75 | | ppm/˚C |
| $f_A$ | Astable Frequency | SW 1, 3 Closed, $V_S$ = 12V | 4.0 | 4.8 | 5.6 | kHz |
| $f_{MAX}$ | Maximum Frequency | Max. Freq. Test Circuit, $V_S$ = 5V | | 3.0 | | MHz |
| $t_R$, $t_F$ | Output Rise and Fall Times | Max. Freq. Test Circuit<br>$V_S$ = 5V, $C_L$ = 10 pF | | 15 | | ns |

## Electrical Characteristics (Notes 1, 2)

Test Circuit, T = 25˚C, all switches open, $\overline{\text{RESET}}$ to $V_S$ unless otherwise noted (Continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units (Limits) |
|---|---|---|---|---|---|---|
| $t_{PD}$ | Trigger Propagation Delay | $V_S$ = 5V, Measure Delay from Trigger to Output | | 100 | | ns |

**Note 1:** All voltages are measured with respect to the ground pin, unless otherwise specified.

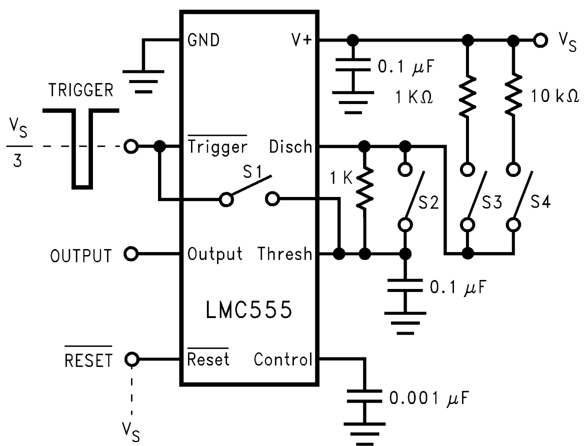
**Note 2:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

**Note 3:** See AN-450 for other methods of soldering surface mount devices, and also AN-1112 for micro SMD considerations.

**Note 4:** If the $\overline{\text{RESET}}$ pin is to be used at temperatures of −20˚C and below $V_S$ is required to be 2.0V or greater.

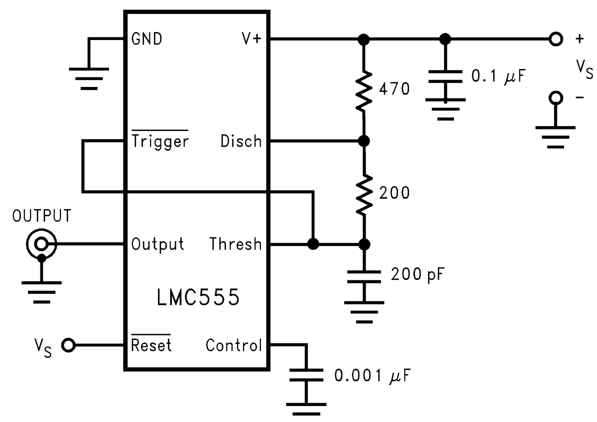
**Note 5:** For device pinout please refer to table 1

**Test Circuit** (Note 5)




DS008669-2

**Maximum Frequency Test Circuit** (Note 5)




DS008669-3

**TABLE 1. Package Pinout Names vs. Pin Function**

| Pin Function | Package Pin numbers | |
|---|---|---|
| | 8-Pin SO,MSOP, and MDIP | 8-Bump micro SMD |
| GND | 1 | 7 |
| $\overline{\text{Trigger}}$ | 2 | 6 |
| Output | 3 | 5 |
| $\overline{\text{Reset}}$ | 4 | 4 |
| Control Voltage | 5 | 3 |
| Threshold | 6 | 2 |
| Discharge | 7 | 1 |
| $V^+$ | 8 | 8 |

# Application Info

### MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by internal circuitry. Upon application of a negative trigger pulse of less than 1/3 $V_S$ to the $\overline{\text{Trigger}}$ terminal, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

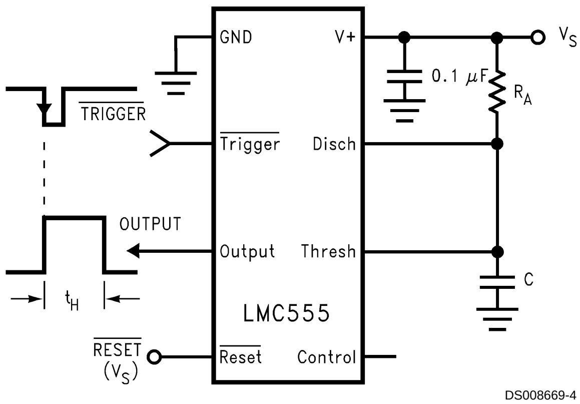
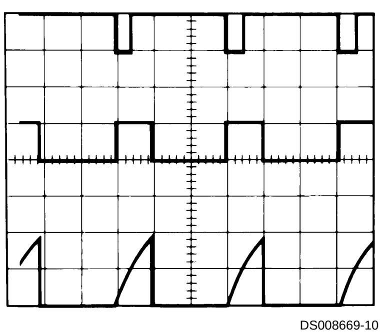



**FIGURE 1. Monostable (One-Shot)**

The voltage across the capacitor then increases exponentially for a period of $t_H$ = 1.1 $R_AC$, which is also the time that the output stays high, at the end of which time the voltage equals 2/3 $V_S$. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.




$V_{CC}$ = 5V  Top Trace: Input 5V/Div.
TIME = 0.1 ms/Div.  Middle Trace: Output 5V/Div.
$R_A$ = 9.1kΩ  Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01µF

**FIGURE 2. Monostable Waveforms**

Reset overrides Trigger, which can override threshold. Therefore the trigger pulse must be shorter than the desired $t_H$. The minimum pulse width for the Trigger is 20ns, and it is 400ns for the Reset. During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal. The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not use, it is recommended that it be connected to $V_+$ to avoid any possibility of false triggering. *Figure 3* is a nomograph for easy determination of RC values for various time delays.

**Note:** In monstable operation, the trigger should be driven high before the end of timing cycle.

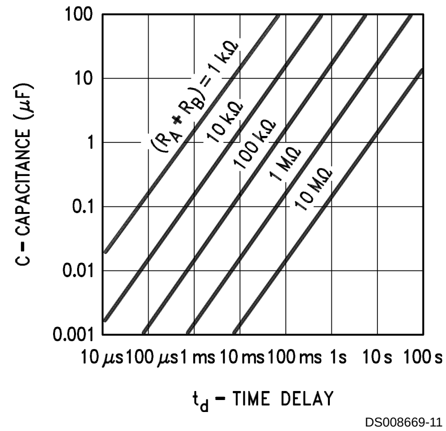



**FIGURE 3. Time Delay**

### ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* ($\overline{\text{Trigger}}$ and Threshold terminals connected together) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A$ + $R_B$ and discharges through $R_B$. Thus the duty cycle may be precisely set by the ratio of these two resistors.

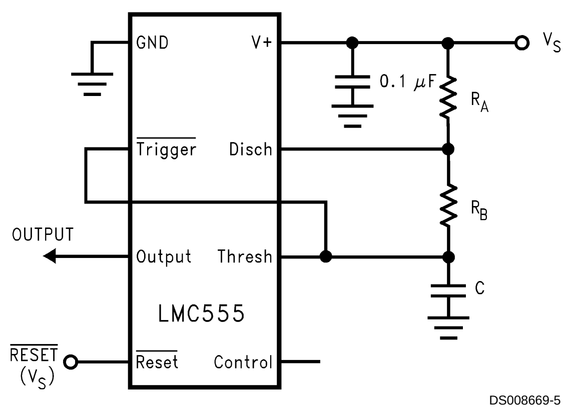
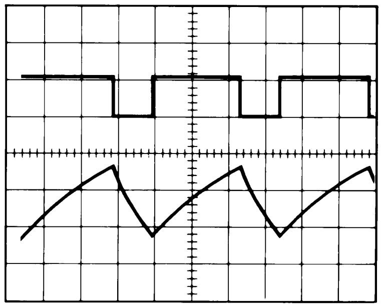



**FIGURE 4. Astable (Variable Duty Cycle Oscillator)**

In this mode of operation, the capacitor charges and discharges between 1/3 $V_S$ and 2/3 $V_S$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

*Figure 5* shows the waveform generated in this mode of operation.

## Application Info (Continued)



DS008669-12

$V_{CC}$ = 5V Top Trace: Output 5V/Div.
TIME = 20 µs/Div. Bottom Trace: Capacitor Voltage 1V/Div.
$R_A$ = 3.9kΩ
$R_B$ = 9kΩ
C = 0.01µF

**FIGURE 5. Astable Waveforms**

The charge time (output high) is given by

$$t_1 = \text{Ln2 } (R_A + R_B)C$$

And the discharge time (output low) by:

$$t_2 = \text{Ln2 } (R_B)C$$

Thus the total period is:

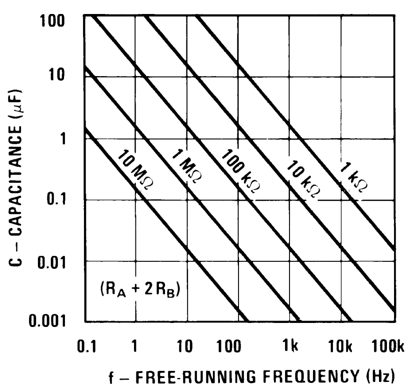
$$T = t_1 + t_2 = \text{Ln2 } (R_A + R_B)C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C}$$

*Figure 6* may be used for quick determination of these RC Values. The duty cycle, as a fraction of total period that the output is low, is:

$$D = \frac{R_B}{R_A + 2R_B}$$

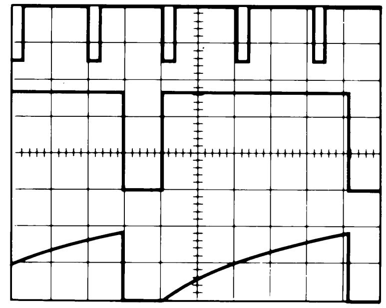



DS008669-13

**FIGURE 6. Free Running Frequency**

### FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



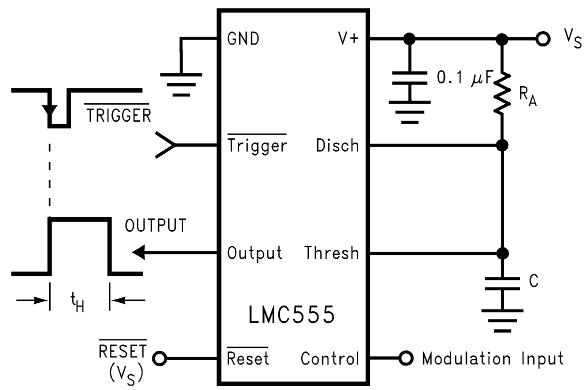
DS008669-14

$V_{CC}$ = 5V Top Trace: Input 4V/Div.
TIME = 20 µs/Div. Middle Trace: Output 2V/Div.
$R_A$ = 9.1 kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01µF

**FIGURE 7. Frequency Divider Waveforms**

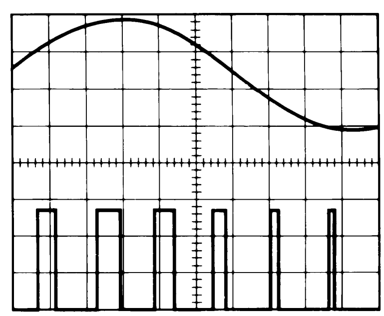
### PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to the Control Voltage Terminal. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.




DS008669-20

**FIGURE 8. Pulse Width Modulator**



DS008669-15

$V_{CC}$ = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/Div. Bottom Trace: Output Voltage 2V/Div.
$R_A$ = 9.1 kΩ
C = 0.01µF

**FIGURE 9. Pulse Width Modulator Waveforms**

### PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with

## Application Info (Continued)

the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

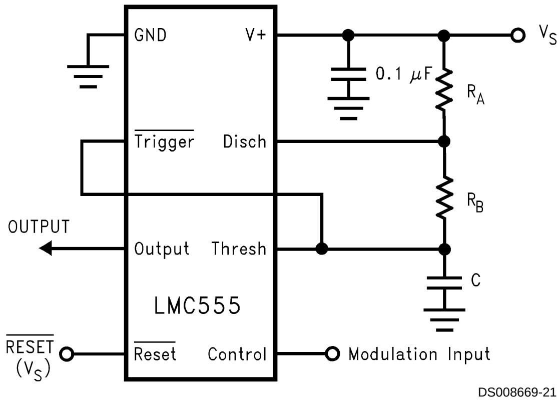
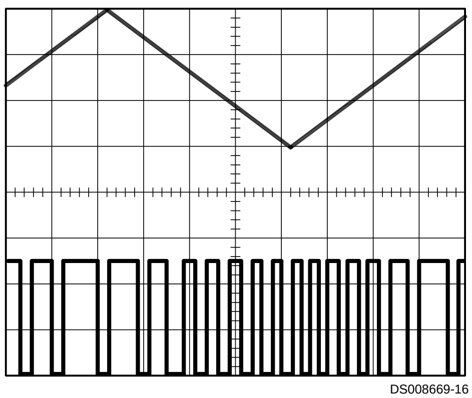



**FIGURE 10. Pulse Position Modulator**




$V_{CC}$ = 5V
TIME = 0.1 ms/Div.
$R_A$ = 3.9 kΩ
$R_B$ = 3 kΩ
C = 0.01µF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

**FIGURE 11. Pulse Position Modulator Waveforms**

**50% DUTY CYCLE OSCILLATOR**

The frequency of oscillation is

$f = 1/(1.4\ R_C C)$

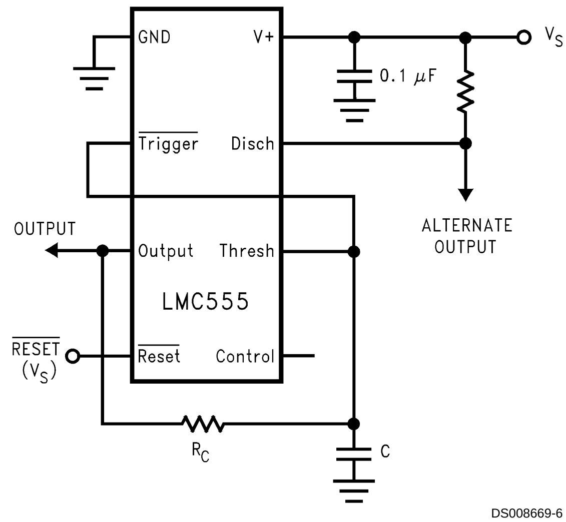
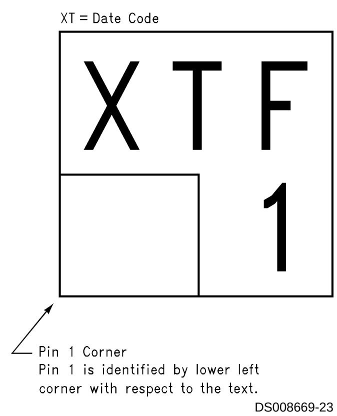


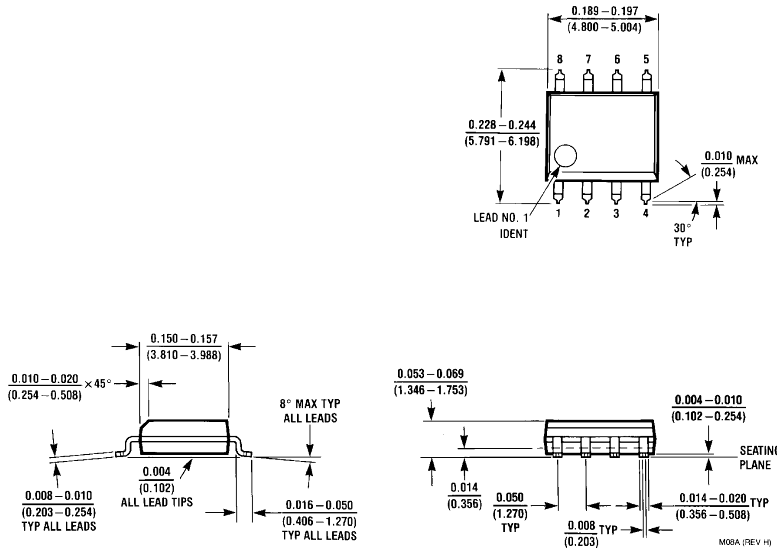

**FIGURE 12. 50% Duty Cycle Oscillator**

**micro SMD Marking Orientation**
**Top View**

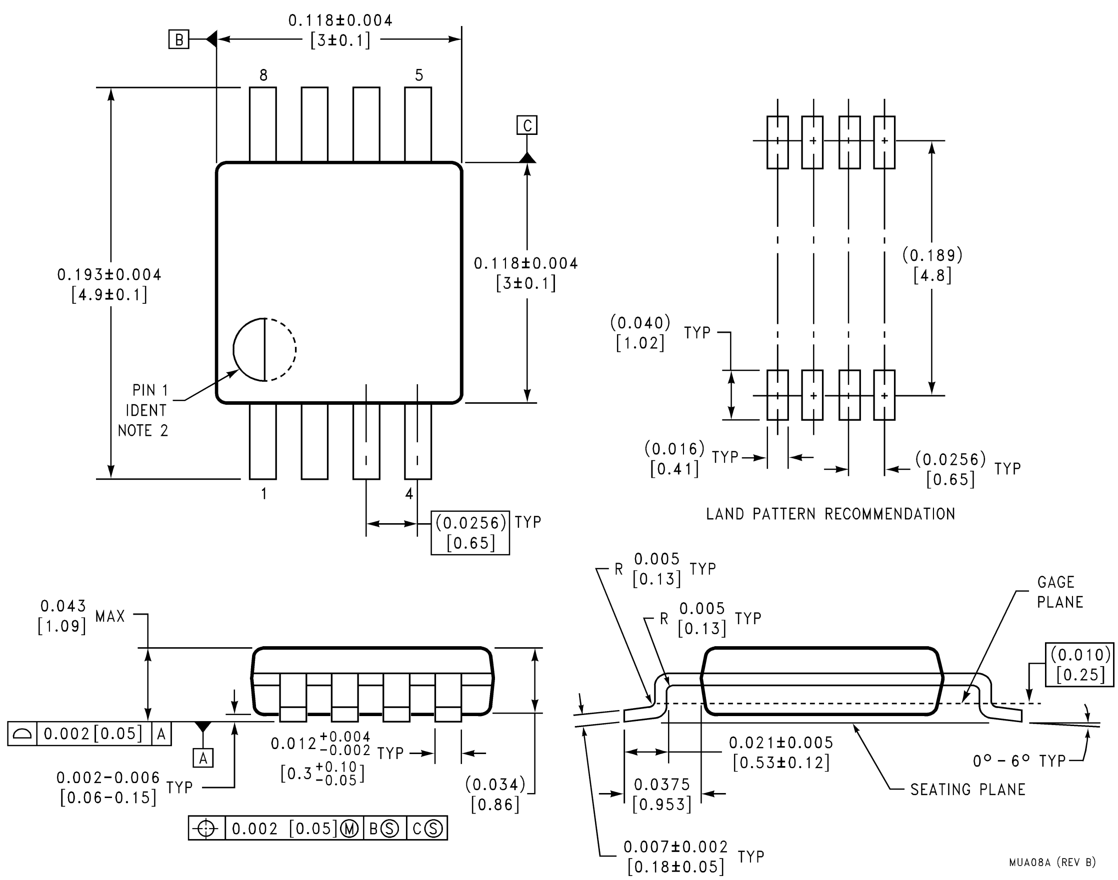



Bumps are numbered counter-clockwise

## Physical Dimensions inches (millimeters) unless otherwise noted

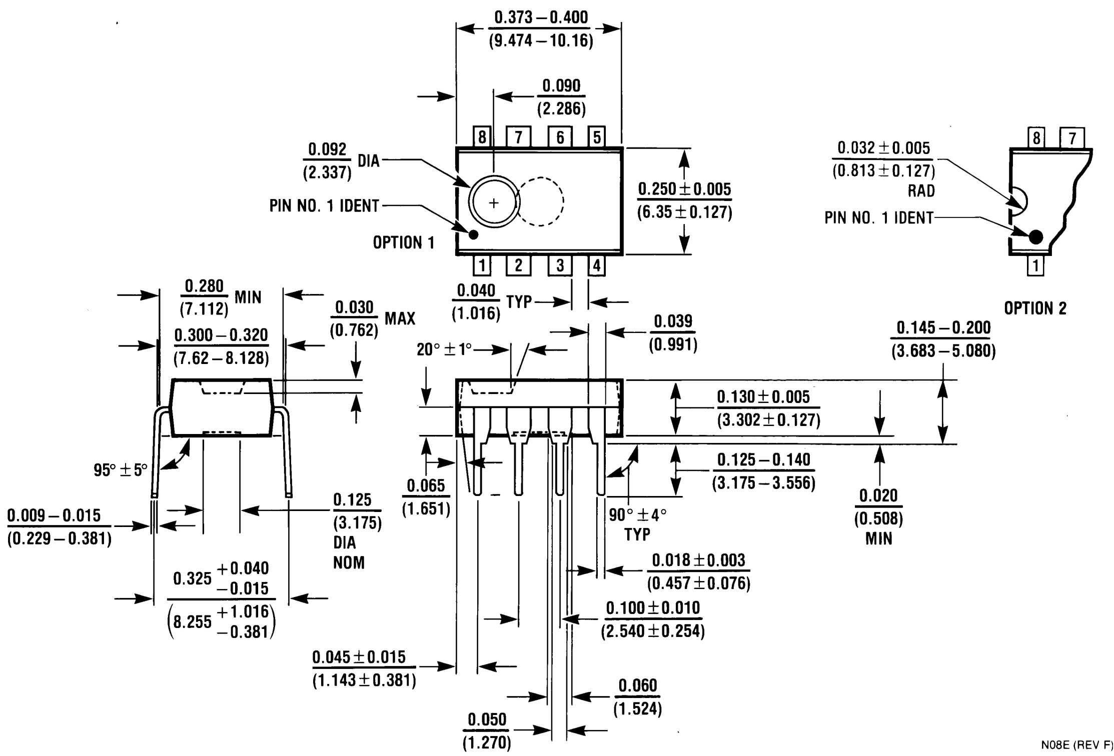



**Molded Small Outline (SO) Package (M)**
**NS Package Number M08A**



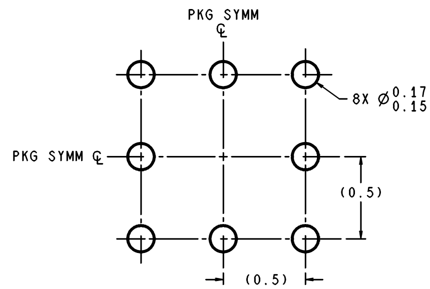

**8-Lead (0.118” Wide) Molded Mini Small Outline Package**
**NS Package Number MUA08A**

## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

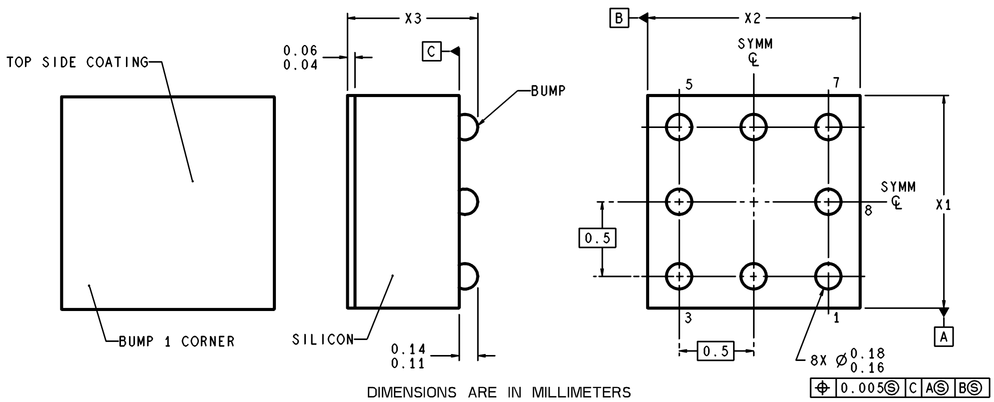



**Molded Dual-in-line Package (N)**
**NS Package Number N08E**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




LAND PATTERN RECOMMENDATION




DIMENSIONS ARE IN MILLIMETERS

BPA08XXX (Rev A)

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTERCLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

**micro SMD Package**
**NS Package Number BPA08EFB**
**$X_1 = 1.387$ $X_2 = 1.412$ $X_3 = 0.850$**

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**National Semiconductor Corporation**
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

**National Semiconductor Europe**
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia Pacific Customer Response Group**
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

**National Semiconductor Japan Ltd.**
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507