

LMC6084 Precision CMOS Quad Operational Amplifier

Check for Samples: [LMC6084](#)

FEATURES

(Typical Unless Otherwise Stated)

- **Low Offset Voltage: 150 μ V**
- **Operates from 4.5V to 15V Single Supply**
- **Ultra Low Input Bias Current: 10 fA**
- **Output Swing to within 20 mV of Supply Rail, 100k Load**
- **Input Common-Mode Range Includes V^-**
- **High Voltage Gain: 130 dB**
- **Improved Latchup Immunity**

APPLICATIONS

- **Instrumentation Amplifier**
- **Photodiode and Infrared Detector Preamplifier**
- **Transducer Amplifiers**
- **Medical Instrumentation**
- **D/A Converter**
- **Charge Amplifier for Piezoelectric Transducers**

DESCRIPTION

The LMC6084 is a precision quad low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6084 ideally suited for precision circuit applications.

Other applications using the LMC6084 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

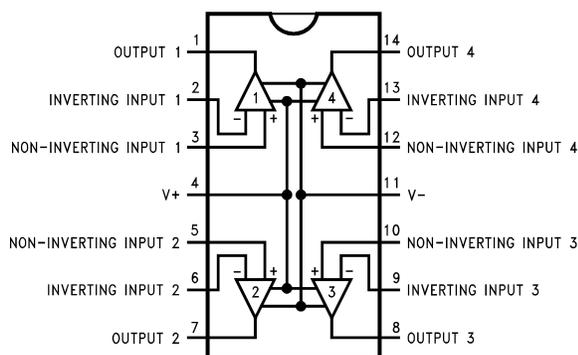
This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6064 precision quad micropower operational amplifier.

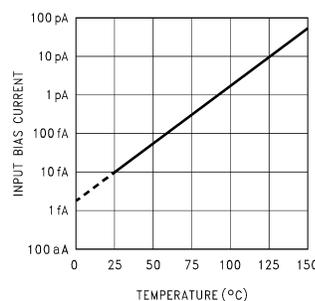
For a single or dual operational amplifier with similar features, see the LMC6081 or LMC6082 respectively.

PATENT PENDING

Connection Diagram



**Figure 1. 14-Pin PDIP/SOIC
Top View**



**Figure 2. Input Bias Current
vs Temperature**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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Absolute Maximum Ratings⁽¹⁾⁽²⁾

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V ⁺) +0.3V, (V ⁻) -0.3V
Supply Voltage (V ⁺ - V ⁻)	16V
Output Short Circuit to V ⁺	See ⁽³⁾
Output Short Circuit to V ⁻	See ⁽⁴⁾
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temp. Range	-65°C to +150°C
Junction Temperature	150°C
ESD Tolerance ⁽⁵⁾	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	See ⁽⁶⁾

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) Do not connect output to V⁺, when V⁺ is greater than 13V or reliability will be adversely affected.
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
- (5) Human body model, 1.5 kΩ in series with 100 pF.
- (6) The maximum power dissipation is a function of T_{J(Max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(Max)} - T_A) / θ_{JA}.

Operating Ratings⁽¹⁾

Temperature Range	LMC6084AM	-55°C ≤ T _J ≤ +125°C
	LMC6084AI, LMC6084I	-40°C ≤ T _J ≤ +85°C
Supply Voltage		4.5V ≤ V ⁺ ≤ 15.5V
Thermal Resistance (θ _{JA}) ⁽²⁾	14-Pin PDIP	81°C/W
	14-Pin SOIC	126°C/W
Power Dissipation		See ⁽³⁾

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
- (2) All numbers apply for packages soldered directly into a PC board.
- (3) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with P_D = (T_J - T_A) / θ_{JA}. All numbers apply for packages soldered directly into a PC board.

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V⁺ = 5V, V⁻ = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	LMC6084AM Limit ⁽²⁾	LMC6084AI Limit ⁽²⁾	LMC6084I Limit ⁽²⁾	Units
V _{OS}	Input Offset Voltage		150	350 1000	350 800	800 1300	μV Max
TCV _{OS}	Input Offset Voltage Average Drift		1.0				μV/°C
I _B	Input Bias Current		0.010	100	4	4	pA Max
I _{OS}	Input Offset Current		0.005	100	2	2	pA Max

- (1) Typical values represent the most likely parametric norm.
- (2) All limits are guaranteed by testing or statistical analysis.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	LMC6084AM Limit ⁽²⁾	LMC6084AI Limit ⁽²⁾	LMC6084I Limit ⁽²⁾	Units		
R_{IN}	Input Resistance		>10				Tera Ω		
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 12.0\text{V}$ $V^+ = 15\text{V}$	85	75 72	75 72	66 63	dB Min		
+PSRR	Positive Power Supply Rejection Ratio	$5\text{V} \leq V^+ \leq 15\text{V}$ $V_O = 2.5\text{V}$	85	75 72	75 72	66 63	dB Min		
-PSRR	Negative Power Supply Rejection Ratio	$0\text{V} \leq V^- \leq -10\text{V}$	94	84 81	84 81	74 71	dB Min		
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5\text{V}$ and 15V for $\text{CMRR} \geq 60\text{ dB}$	-0.4	-0.1 0	-0.1 0	-0.1 0	V Max		
			$V^+ - 1.9$	$V^+ - 2.3$ $V^+ - 2.6$	$V^+ - 2.3$ $V^+ - 2.5$	$V^+ - 2.3$ $V^+ - 2.5$	V Min		
A_V	Large Signal Voltage Gain	$R_L = 2\text{ k}\Omega$ ⁽³⁾	Sourcing	1400 300	400 300	400 200	300 200	V/mV Min	
			Sinking	350 70	180 100	180 60	90 60	V/mV Min	
		$R_L = 600\Omega$ ⁽³⁾	Sourcing	1200 150	400 150	400 150	200 80	V/mV Min	
			Sinking	150 35	100 50	100 35	70 35	V/mV Min	
V_O	Output Swing	$V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to 2.5V	4.87	4.80 4.70	4.80 4.73	4.75 4.67	V Min		
			0.10	0.13 0.19	0.13 0.17	0.20 0.24	V Max		
		$V^+ = 5\text{V}$ $R_L = 600\Omega$ to 2.5V	4.61	4.50 4.24	4.50 4.31	4.40 4.21	V Min		
			0.30	0.40 0.63	0.40 0.50	0.50 0.63	V Max		
		$V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to 7.5V	14.63	14.50 14.30	14.50 14.34	14.37 14.25	V Min		
			0.26	0.35 0.48	0.35 0.45	0.44 0.56	V Max		
		$V^+ = 15\text{V}$ $R_L = 600\Omega$ to 7.5V	13.90	13.35 12.80	13.35 12.86	12.92 12.44	V Min		
			0.79	1.16 1.42	1.16 1.32	1.33 1.58	V Max		
		I_O	Output Current $V^+ = 5\text{V}$	Sourcing, $V_O = 0\text{V}$	22	16 8	16 10	13 8	mA Min
				Sinking, $V_O = 5\text{V}$	21	16 11	16 13	13 10	mA Min
		I_O	Output Current $V^+ = 15\text{V}$	Sourcing, $V_O = 0\text{V}$	30	28 18	28 22	23 18	mA Min
				Sinking, $V_O = 13\text{V}$ ⁽⁴⁾	34	28 19	28 22	23 18	mA Min

(3) $V^+ = 15\text{V}$, $V_{\text{CM}} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

(4) Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	LMC6084AM Limit ⁽²⁾	LMC6084AI Limit ⁽²⁾	LMC6084I Limit ⁽²⁾	Units
I_S	Supply Current	All Four Amplifiers	1.8	3.0	3.0	3.0	mA
		$V^+ = +5\text{V}$, $V_O = 1.5\text{V}$		3.6	3.6	3.6	Max
		All Four Amplifiers	2.2	3.4	3.4	3.4	mA
		$V^+ = +15\text{V}$, $V_O = 7.5\text{V}$		4.0	4.0	4.0	Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	LMC6084AM Limit ⁽²⁾	LMC6084AI Limit ⁽²⁾	LMC6084I Limit ⁽²⁾	Units
SR	Slew Rate	See ⁽³⁾	1.5	0.8 0.5	0.8 0.6	0.8 0.6	V/ μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	See ⁽⁴⁾	140				dB
e_n	Input-Referred Voltage Noise	$F = 1\text{ kHz}$	22				nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$F = 1\text{ kHz}$	0.0002				pA/ $\sqrt{\text{Hz}}$
T.H.D.	Total Harmonic Distortion	$F = 10\text{ kHz}$, $A_V = -10$ $R_L = 2\text{ k}\Omega$, $V_O = 8\text{ V}_{\text{PP}}$ $\pm 5\text{V}$ Supply	0.01				%

(1) Typical values represent the most likely parametric norm.

(2) All limits are guaranteed by testing or statistical analysis.

(3) $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

(4) Input referred $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\text{ V}_{\text{PP}}$.

Typical Performance Characteristics

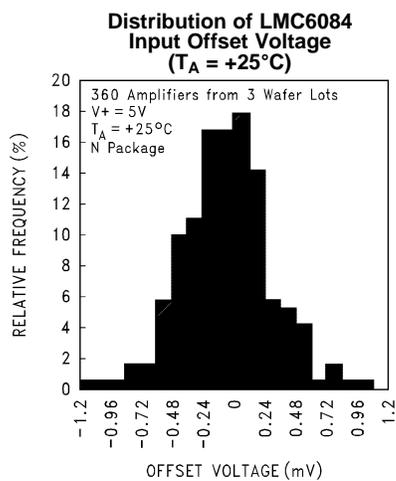


Figure 3.

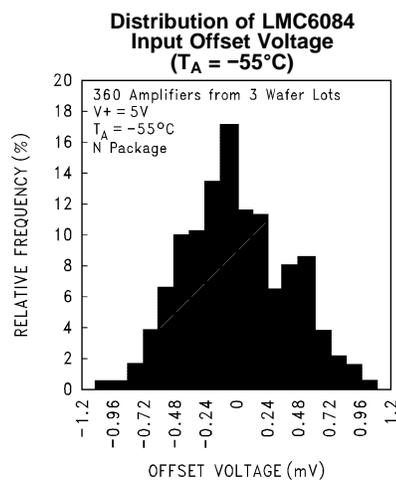


Figure 4.

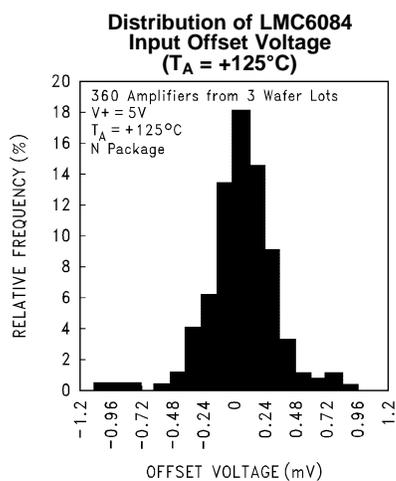


Figure 5.

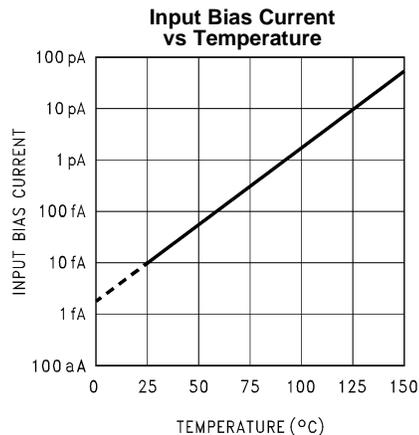


Figure 6.

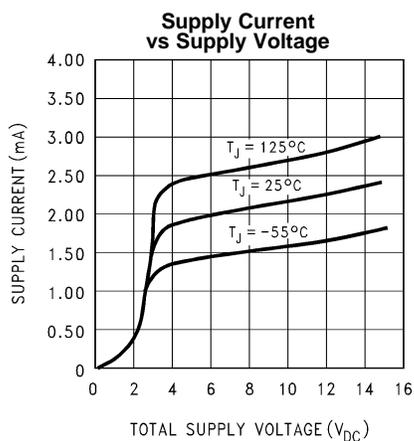


Figure 7.

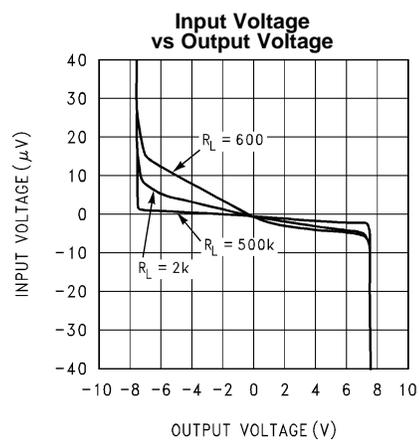


Figure 8.

Typical Performance Characteristics (continued)

Common Mode Rejection Ratio vs Frequency

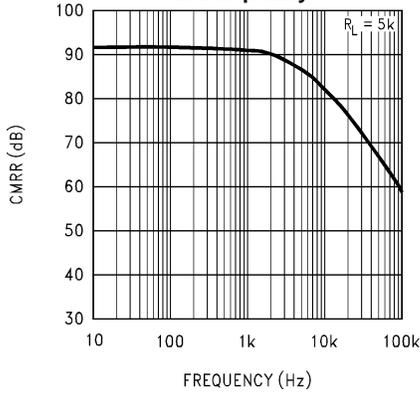


Figure 9.

Power Supply Rejection Ratio vs Frequency

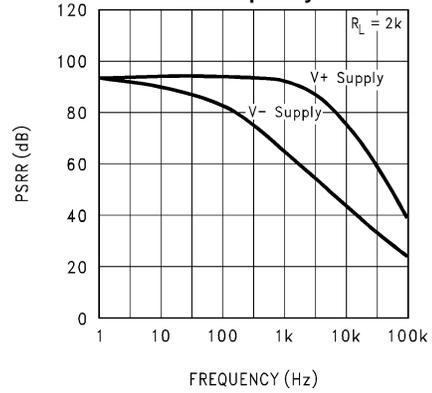


Figure 10.

Input Voltage Noise vs Frequency

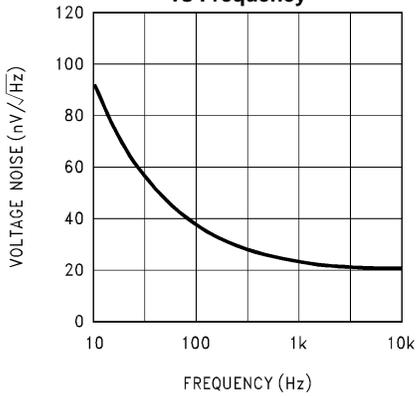


Figure 11.

Output Characteristics Sourcing Current

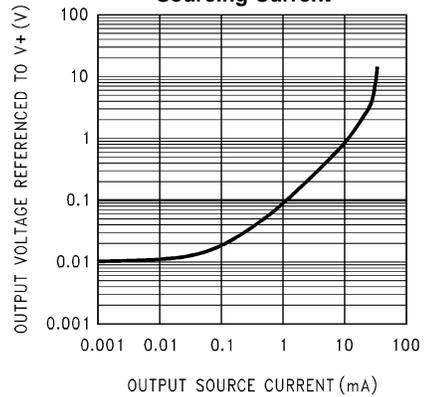


Figure 12.

Output Characteristics Sinking Current

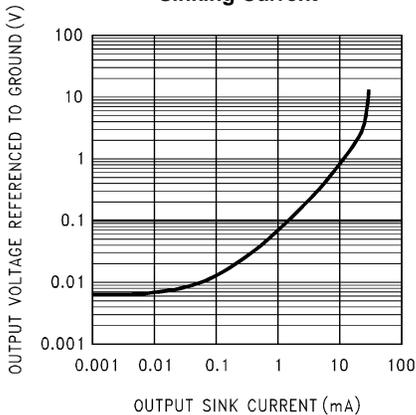


Figure 13.

Gain and Phase Response vs Temperature (-55°C to +125°C)

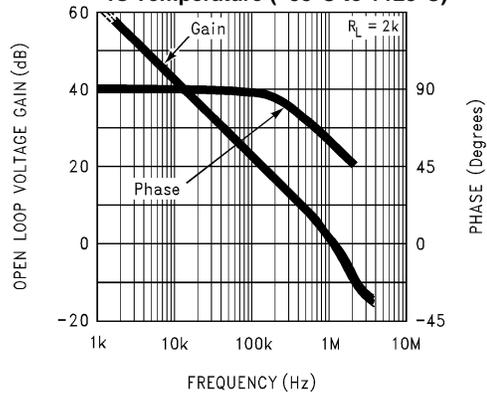


Figure 14.

Typical Performance Characteristics (continued)

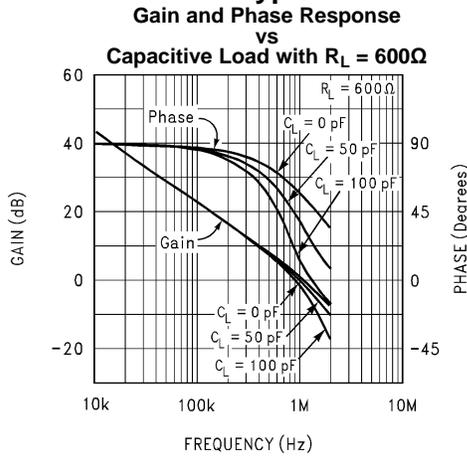


Figure 15.

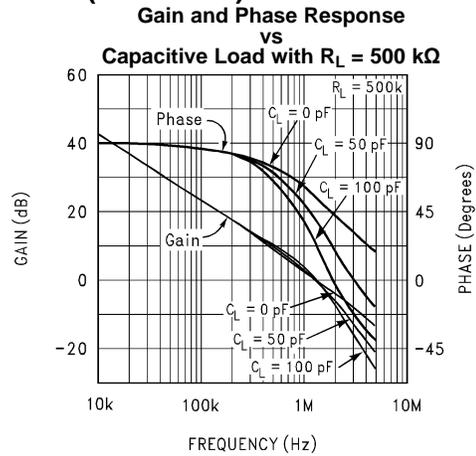


Figure 16.

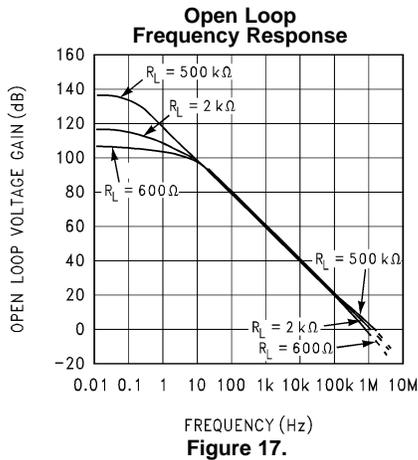


Figure 17.

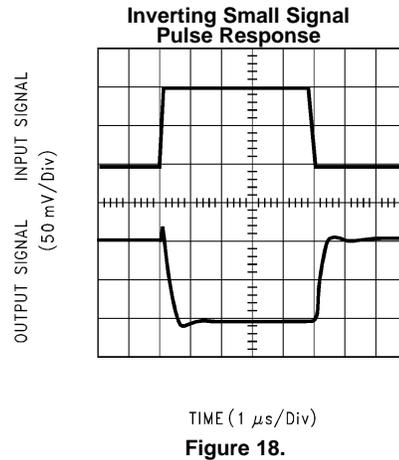


Figure 18.

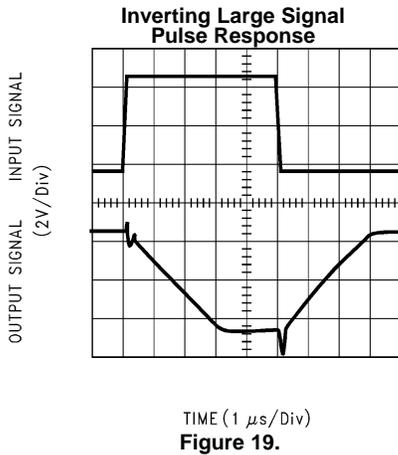


Figure 19.

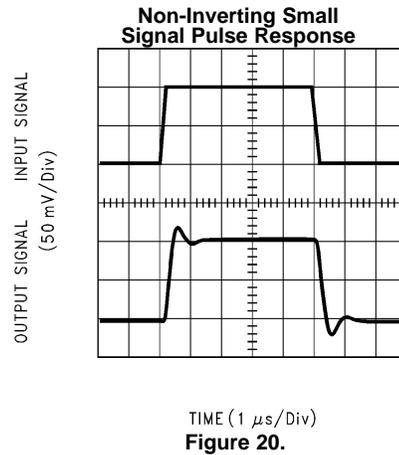


Figure 20.

Typical Performance Characteristics (continued)

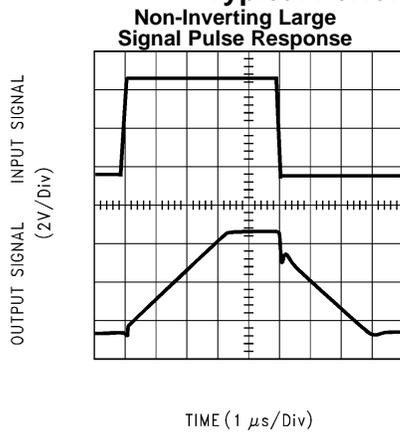


Figure 21.

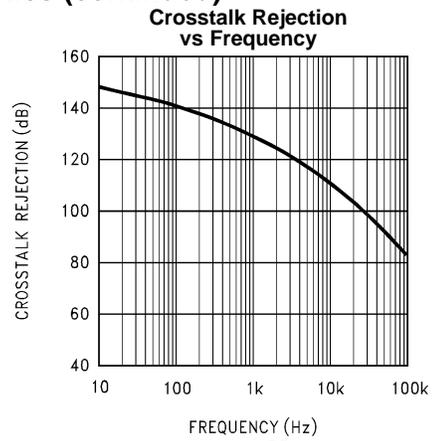


Figure 22.

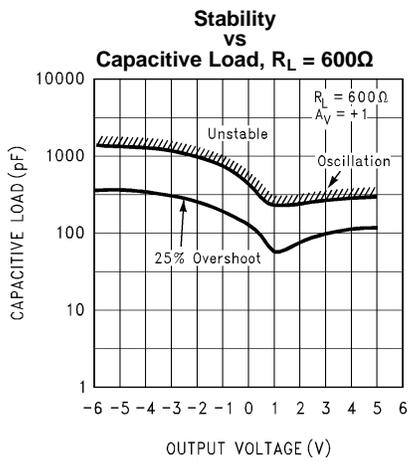


Figure 23.

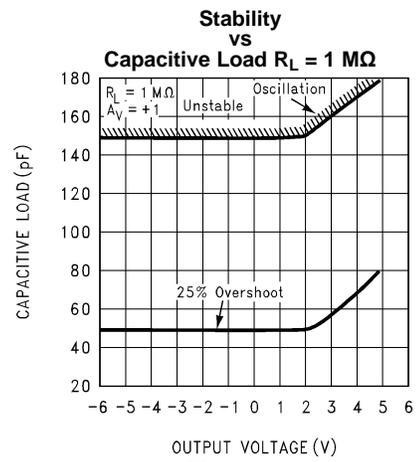


Figure 24.

APPLICATIONS HINTS

AMPLIFIER TOPOLOGY

The LMC6084 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6084 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6084.

Although the LMC6084 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6084 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See [Printed-Circuit-Board Layout for High Impedance Work](#))

The effect of input capacitance can be compensated for by adding a capacitor, C_f , around the feedback resistors (as in [Figure 25](#)) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or (2)

$$R_1 C_{IN} \leq R_2 C_f \quad (3)$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

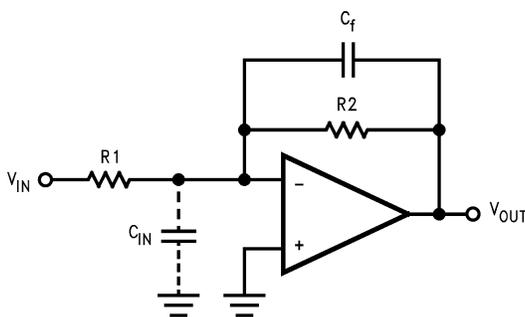


Figure 25. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see [typical curves](#)).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in [Figure 26](#).

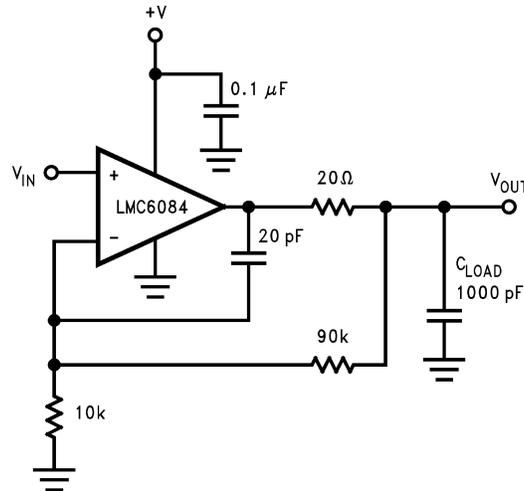


Figure 26. LMC6084 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of [Figure 26](#), R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V⁺ [Figure 27](#). Typically a pull up resistor conducting 500 μ A or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see [Electrical Characteristics](#)).

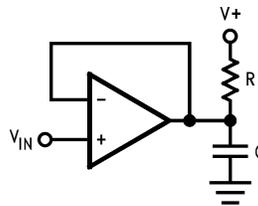


Figure 27. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6084, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6084's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in [Figure 28](#). To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6084's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See [Figure 29](#) for typical connections of guard rings for standard op-amp configurations.

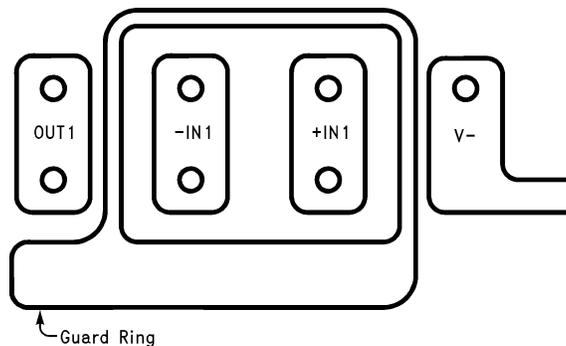


Figure 28. Example of Guard Ring in P.C. Board Layout

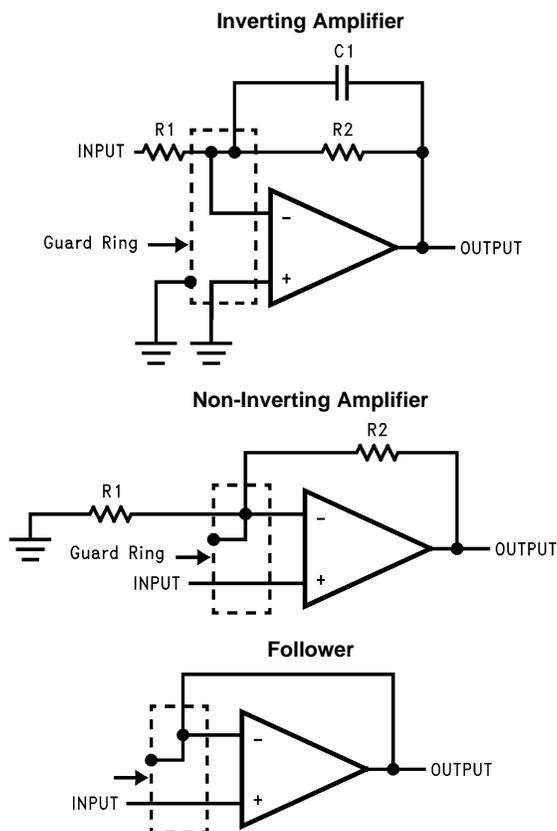
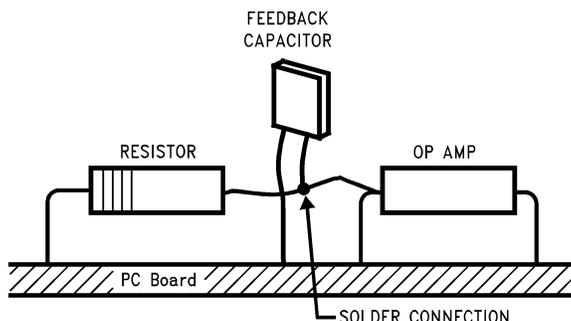


Figure 29. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See [Figure 30](#).

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6084 is designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

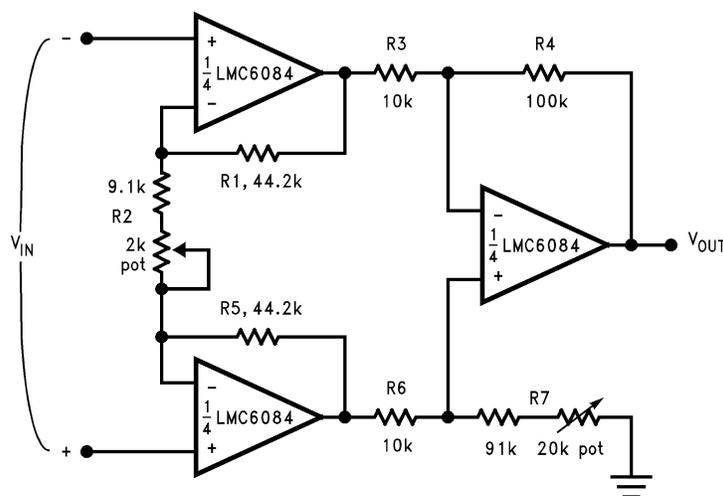
Figure 30. Air Wiring

Typical Single-Supply Applications

$(V^+ = 5.0 V_{DC})$

The extremely high input impedance, and low power consumption, of the LMC6084 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 31 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 $\mu V/^\circ C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

∴ $A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

Figure 31. Instrumentation Amplifier

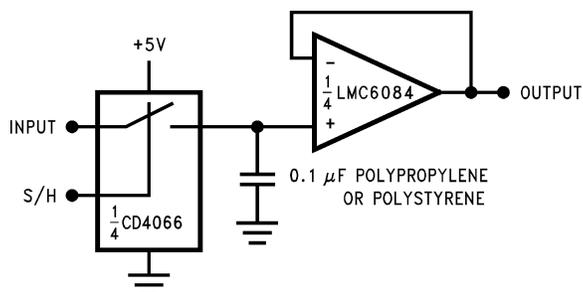


Figure 32. Low-Leakage Sample and Hold

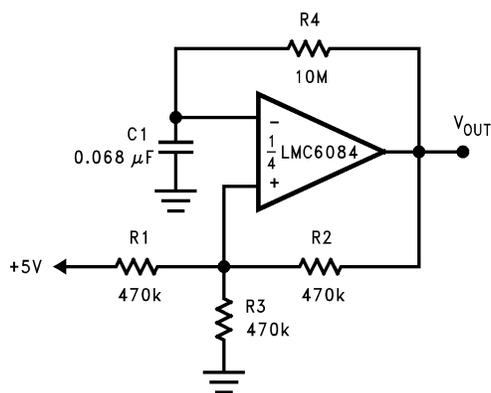


Figure 33. 1 Hz Square Wave Oscillator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMC6084AIM	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMC6084 AIM	Samples
LMC6084AIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6084 AIM	Samples
LMC6084AIMX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMC6084 AIM	Samples
LMC6084AIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6084 AIM	Samples
LMC6084IM	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMC6084IM	Samples
LMC6084IM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6084IM	Samples
LMC6084IMX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMC6084IM	Samples
LMC6084IMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6084IM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

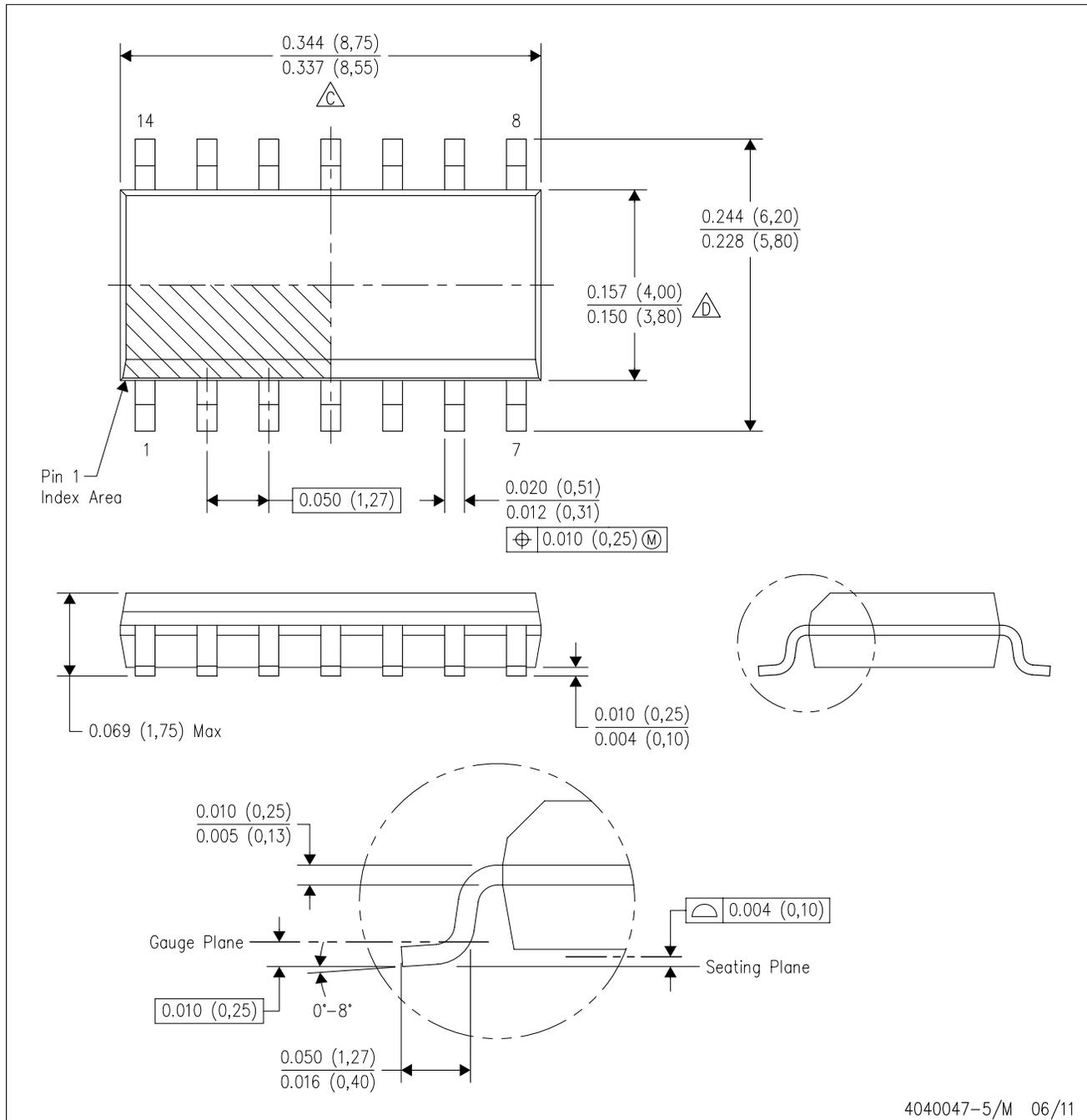
(4) Only one of markings shown within the brackets will appear on the physical device.

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D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

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