National Semiconductor Corporation

PRELIMINARY

LMC660AM /LMC660AI /LMC660C CMOS Quad Operational Amplifier

General Description

The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It is fully specified for operation from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

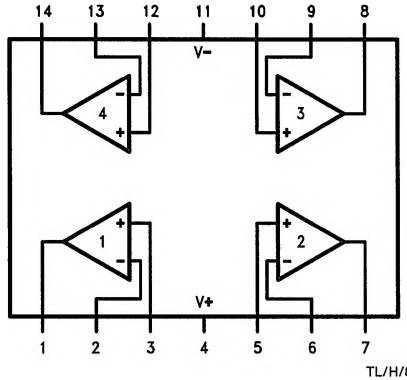
This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

Features

- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low input offset voltage 3 mV max
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode includes GND
- Operation guaranteed from +5V to +15V
- I_{SS} = 375 μA/amplifier; independent of V^+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Insensitive to latch-up

Connection Diagram

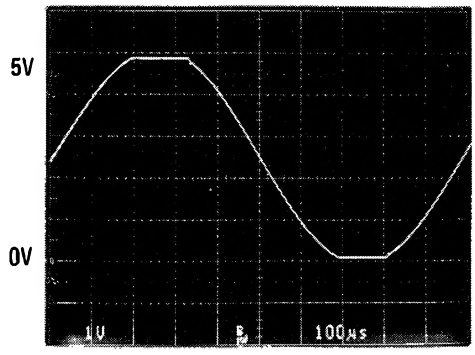
14 Pin DIP



TL/H/8767–1

Order Number LMC660AMD or LMC660AID
Order Number LMC660AIN or LMC660CN
See NS Package Number D14E or N14A

Output Swing



V^+ = 5V R_L = 2 kΩ

TL/H/8767–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Either Input beyond V^+ or V^-	0.7V
Supply Voltage	16V
Output Short Circuit to GND (Note 1)	Continuous
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Operating Temperature Range	
LMC660AM	−55°C to +125°C
LMC660AI	−40°C to +85°C
LMC660C	0°C to +70°C
Operating Supply Range	4.75V to 15.5V
Junction Temperature (Note 2)	150°C

ESD rating is to be determined.

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LMC660AM		LMC660AI		LMC660C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		1	3		3	**3.3**	6	**6.3**	mV max
			3.5						
Input Offset Voltage Average Drift		1.3							µV/°C
Input Bias Current	(Note 9)	0.04	20		20	**4**		**2**	pA max
			30						
Input Offset Current	(Note 9)	0.01	20		20	**2**		**1**	pA max
			30						
Input Resistance		>1							TerraΩ
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70		72	**68**	63	**62**	dB min
			68						
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70		70	**68**	68	**62**	dB min
			68						
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84		84	**83**	74	**73**	dB min
			82						
Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1		−0.1	**0**	−0.1	**0**	V max
			0						
		$V^+ - 1.9$	$V^+ - 2.3$		$V^+ - 2.3$	$\mathbf{V^+ - 2.5}$	$V^+ - 2.3$	$\mathbf{V^+ - 2.4}$	V min
			$\mathbf{V^+ - 2.6}$						
Large Signal Voltage Gain	$R_L = 2 k\Omega$ (Note 6)								
	Sourcing	2000	400		400	**440**	200	**300**	V/mV min
			300						
	Sinking	500	180		180	**120**	90	**80**	V/mV min
			70						
	$R_L = 600\Omega$ (Note 6)								
	Sourcing	1000	200		200	**220**	100	**150**	V/mV min
			150						
	Sinking	250	100		100	**60**	50	**40**	V/mV min
			35						

DC Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	Typ	LMC660AM		LMC660AI		LMC660C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Swing	$V^+ = 5V$ $R_L = 2\,k\Omega$ to $V^+/2$	4.87	4.82		4.82	**4.79**	4.78	**4.76**	V min
			4.77						
		0.10	0.15		0.15	**0.17**	0.19	**0.21**	V max
			0.19						
	$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$	4.61	4.41		4.41	**4.31**	4.27	**4.21**	V min
			4.24						
		0.30	0.50		0.50	**0.56**	0.63	**0.69**	V max
			0.63						
	$V^+ = 15V$ $R_L = 2\,k\Omega$ to $V^+/2$	14.63	14.50		14.50	**14.44**	14.37	**14.32**	V min
			14.40						
		0.26	0.35		0.35	**0.40**	0.44	**0.48**	V max
			0.43						
	$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$	13.90	13.35		13.35	**13.15**	12.92	**12.76**	V min
			13.02						
		0.79	1.16		1.16	**1.32**	1.45	**1.58**	V max
			1.42						
Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16		16	**14**	13	**11**	mA min
			12						
	Sinking, $V_O = 5V$	21	16		16	**14**	13	**11**	mA min
			12						
Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19		28	**25**	23	**21**	mA min
			19						
	Sinking, $V_O = 13V$	39	19		28	**24**	23	**20**	mA min
			19						
Supply Current	All Four Amplifiers	1.5	2.2		2.2	**2.6**	2.7	**2.9**	mA min
			2.9						

AC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LMC660AM		LMC660AI		LMC660C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Slew Rate	(Note 7)	1.1	0.8		0.8	**0.6**		**0.7**	V/μs min
			0.5						
Gain-Bandwidth Product		1.4							MHz min
Phase Margin		50							Deg
Gain Margin		17							dB
Amp-to-Amp Isolation	(Note 8)	130							dB
Input Referred Voltage Noise	F = 1 kHz	22							nV/√Hz
Input Referred Current Noise	F = 1 kHz	0.0002							pA/√Hz
Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP}	0.01							%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The junction-to-ambient thermal resistance of the molded plastic DIP (N) is 75°C/W., the molded plastic SO (M) package is 105°C/W., and the cavity DIP (D) package is 92°C/W. All numbers apply for packages soldered directly into a PC board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1\ M\Omega$ unless otherwise specified.

Note 4: These limits are guaranteed and are used in calculating outgoing AQL.

Note 5: These limits are guaranteed, but are not used in calculating outgoing AQL.

Note 6: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 7: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 8: Input referred. $V^+ = 15V$ and $R_L = 10\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

Note 9: The specifications in the Design Limit column reflect the true performance of the part, while those in the Tested Limit column are degraded to allow for the unavoidable inaccuracies involved in cost-effective high-speed automatic testing.