National Semiconductor Corporation

PRELIMINARY

LMC668A/LMC668 Chopper Stabilized Operational Amplifier

General Description

The LMC668 is a high performance versatile chopper-stabilized amplifier with low input offset voltage. This low offset is achieved through a nulling scheme that provides continuous error correction. A nulling amplifier alternately nulls itself and the main amplifier. Two external capacitors are used to store the correcting voltages on the amplifier nulling inputs. The LMC668 has exceptionally low offset drift over time and temperature. The nulling circuit also provides for very high open loop gain, CMRR, and PSRR at low frequencies.

The clock oscillator and all the other control circuitry are completely self contained. The 14-pin version has an Internal/External Clock select pin and an External Clock In pin for use in applications requiring synchronized or special chopping frequencies. The 8-pin version does not allow for an external clock or the output clamp. Both versions are pin compatible replacements for the ICL7650 series of parts.

Features

- Low input offset voltage
- High gain, CMRR and PSRR
- Low offset voltage drift with time and temperature
- Low DC input bias current
- Low intermodulation effects

Key Specifications

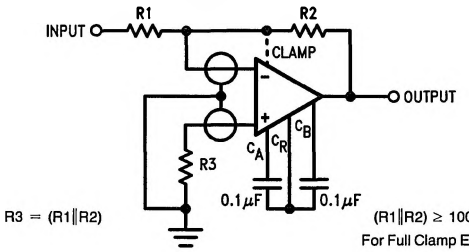
■ Input offset voltage	$< \pm 5\ \mu V$
■ DC input bias current	<60 pA
■ Large signal voltage gain	$> 10^6$ V/V
■ Common mode rejection ratio	>120 dB
■ Power supply rejection ratio	>120 dB
■ Internal chopping frequency	Typ 200 Hz

Ordering Information

Part	Temp Range	Package
LMC668ACJ	0°C to 70°C	14 pin CERDIP
LMC668CJ	0°C to 70°C	14 pin CERDIP
LMC668ACJ-8	0°C to 70°C	8 pin CERDIP
LMC668CJ-8	0°C to 70°C	8 pin CERDIP
LMC668ACN	0°C to 70°C	14 pin Plastic
LMC668CN	0°C to 70°C	14 pin Plastic
LMC668ACN-8	0°C to 70°C	8 pin Plastic
LMC668CN-8	0°C to 70°C	8 pin Plastic

Typical Applications

Inverting Amplifier with Optional Clamp



R3 = (R1‖R2)

(R1‖R2) ≥ 100 KΩ
For Full Clamp Effect

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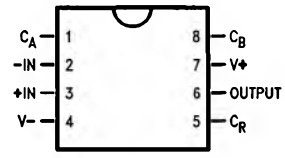
Connection Diagram

LMC668-8



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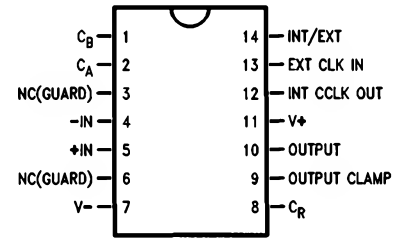
Top View

LMC668



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V^+ to V^-)	18V
Input Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Voltage on Oscillator Control Pins	V^+ to V^-
Except EXT CLOCK IN:	(V^+ + 0.3V) to (V^+ − 6.0V)
Duration of Output Short Circuit	Indefinite
Current into any pin	10 mA
—while operating (Note 2)	100 μA
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Susceptibility (Note 4)	1500V
Power Dissipation (Note 3)	
CERDIP J Package	500 mW
Plastic N Package	375 mW
Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC668ACJ/CJ	0°C to 70°C
LMC668ACN/CN	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	125°C

Electrical Characteristics: Vsupply = ±5V unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all others limits T_A = 25°C.

Symbol	Parameter	Conditions	LMC668A			LMC668			Limit Units
			Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
V_{OS}	Input Offset Voltage	0V Common Mode	±1	±5	**±15**	±1	±10	**±20**	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Temperature Coefficient of Input Offset Voltage	CJ Suffix Parts CN Suffix Parts	±0.05 ±0.05			±0.05 ±0.05			μV/°C μV/°C
I_{Bias}	Input Bias Current	0V Common Mode	±20	±60		±20	±60		pA
R_{IN}	Input Resistance		10^{12}			10^{12}			Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 10 KΩ	5x10⁶	1x10⁶	**0.5x10⁶**	5x10⁶	1x10⁶	**0.5x10⁶**	V/V
V_{OUT}	Output Voltage Swing	Clamp not Connected } R_L = 10 KΩ R_L = 100 KΩ	±4.85 ±4.95	±4.7	**±4.7**	±4.85 ±4.95	±4.7	**±4.7**	V V
CMVR	Common Mode Voltage Range		−5.2 to +2.0	−5.0 to +1.6	**−5.0 to +1.6**	−5.2 to +2.0	−5.0 to +1.6	**−5.0 to +1.6**	V V
CMRR	Common Mode Rejection Ratio	CMVR = −5V to +1.6V	125	120	**107**	125	110	**107**	dB
PSRR	Power Supply Rejection Ratio	±3V to ±8V	130	120	**108**	130	120	**108**	dB
V+ to V−	Operating Supply Range (Note 1)			4.5 to 16	**4.5 to 16**		4.5 to 16	**4.5 to 16**	V V
I_{SUPP}	Supply Current	No Load	1.8	3.5	**3.5**	1.8	3.5	**3.5**	mA
f_{CLK}	Internal Chopping Frequency	pins 13 and 14 open (14 pin DIP)	200	120 to 375	**70 to 375**	200	120 to 375	**70 to 375**	Hz Hz
	Clamp ON Current (Note 8)	R_L = 100 KΩ	70	25 to 200	**25 to 200**	70	25 to 200	**25 to 200**	μA μA
	Clamp Off Current (Note 8)	−4.0V < Vout < +4.0V	1			1			pA
e_n	Input Noise Voltage	Rs = 100Ω, 0 to 10 Hz	2			2			μVp-p
I_n	Input Noise Current	f = 10 Hz	0.01			0.01			pA/√HZ
GBW	Unity Gain Bandwidth		1.0			1.0			MHz
SR	Slew Rate	C_L = 50 pF, R_L = 10 KΩ	2.5			2.5			V/μs
t_r	Rise Time		0.2			0.2			μs
	Overshoot		20			20			%
	Offset Voltage vs Time		100			100			nV/mth

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: To avoid possible destructive latchup, currents greater than 100 μA should not be forced into the input pins.

Note 3: The maximum allowable power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, Θ_{JA}, and ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is less. Θ_{JA} is typically 120°C/W for the J package and 140°C/W for the N package.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Specifications in the "Typical" column are at 25°C and represent the most likely parametric norm.

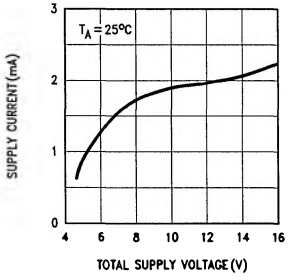
Note 6: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Guaranteed and not 100% production tested. These limits are not used to calculate outgoing quality levels.

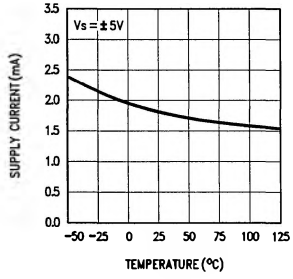
Note 8: See Output Clamp discussion in Application Hints.

Typical Performance Characteristics

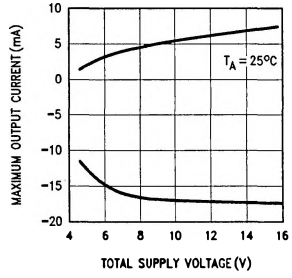
Supply Current vs Supply Voltage



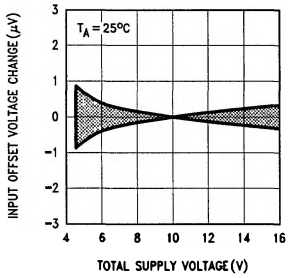
Supply Current vs Ambient Temperature



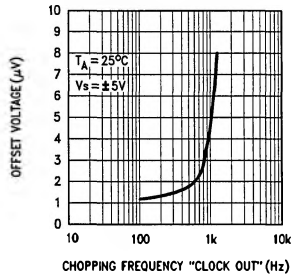
Max Output Current vs Supply Voltage



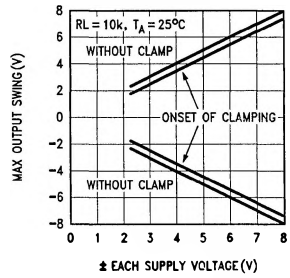
Input Offset Voltage Change vs Supply Voltage



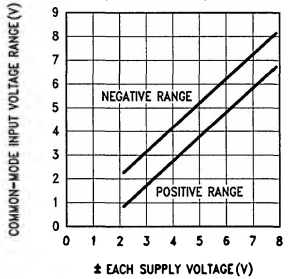
Input Offset Voltage vs Chopping Frequency



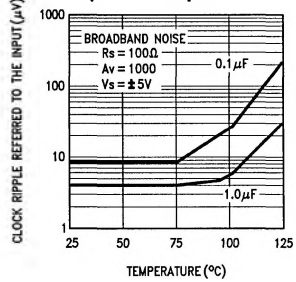
Max Output Swing vs Supply Voltage



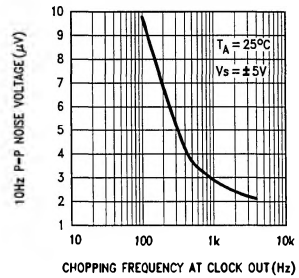
Common-Mode Input Voltage Range vs Supply Voltage



Clock Ripple Referred to the Input vs Temperature



10 Hz P-P Noise Voltage vs Chopping Frequency



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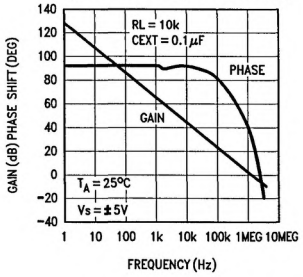
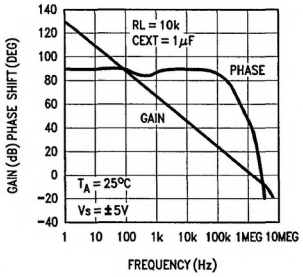
Typical Performance Characteristics (Continued)

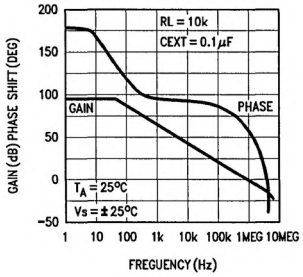
Open Loop Gain and Phase Shift vs Frequency (Autozeroing Main Amp.)



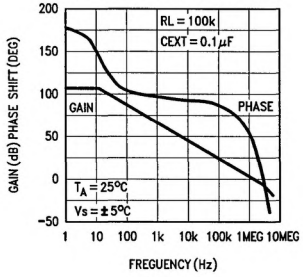
Open Loop Gain and Phase Shift vs Frequency (Autozeroing Main Amp.)



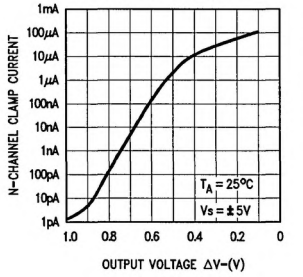
Open Loop Gain and Phase Shift vs Frequency (Autozeroing Null Amp.)



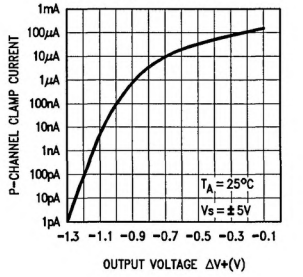
Open Loop Gain and Phase Shift vs Frequency (Autozeroing Null Amp.)



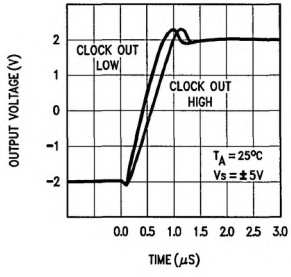
N-Channel Clamp Current vs Output Voltage



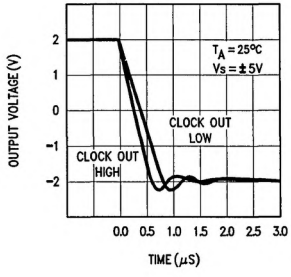
P-Channel Clamp Current vs Output Voltage



Voltage Follower Large Signal Pulse Response



Voltage Follower Large Signal Pulse Response



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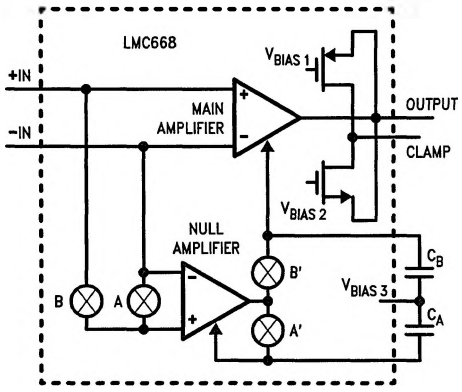
Application Hints

THEORY OF OPERATION

Figure 1 shows a simplified block diagram of the LMC668's analog signal path. The circuit effectively consists of two amplifiers, some MOS switches, and a pair of external capacitors. The "main amplifier" is a conventional MOS operational amplifier and is connected to the external feedback components. This amplifier is always active. The "null amplifier" has its inverting input connected to the main amplifier's inverting input. The null amplifier's non-inverting input is switched between the main amplifier's two inputs. Each amplifier also has an additional input pin that can be use to adjust V_{OS}.

In operation, the null amplifier's inputs are first shorted together, and its output is connected to its V_{OS} input. This creates a negative feedback loop that adjusts the input V_{OS} to zero. When switches A' and B' are opened, the correction voltage at the V_{OS} input is stored by capacitor C_A, holding the null amplifier offset voltage at zero. Switch B is then closed, shorting the main amplifier's non-inverting input to the null amplifier's non-inverting input. Since the main amplifier is enclosed in the external feedback loop, its two inputs should ideally be at the same voltage. Any voltage difference between the main amplifier's inputs will be amplified by the nullling amplifier and applied to the main amp's V_{OS} adjust pin. The closed loop system reaches equilibrium when the main amplifier's input V_{OS} equals zero. The correction voltage for the main amplifier is stored on C_B, and the entire process repeats at the chopping frequency (around 200 Hz).



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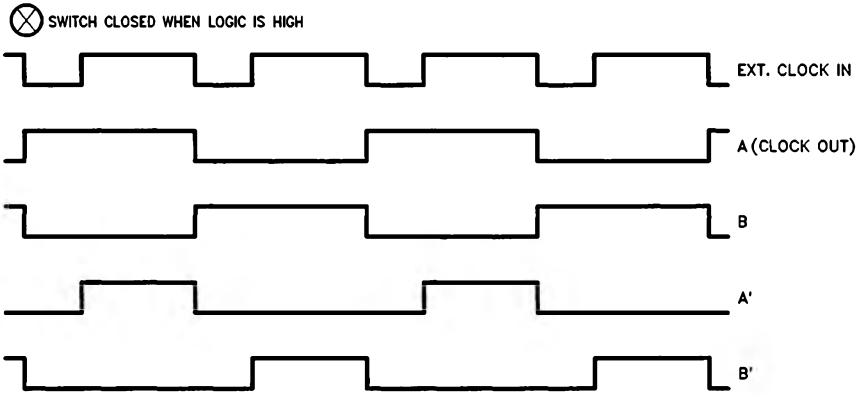

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FIGURE 1. Block Diagram of LMC668 Analog Signal Path

Application Hints (Continued)

Figure 2 shows a simplified schematic of the block diagram in *Figure 1*. Note that transistor P1 serves as the inverting input for both the main amplifier and the null amplifier. Note also that the "back gate" substrate connections on transistors N1 and N2 are the V_{OS} adjust inputs. Increasing the back gate voltage on these transistors increases the channel conductivity, but to a lesser degree than would be caused by an equivalent voltage change at the "normal" gate.

INTERMODULATION

An ideal operational amplifier has infinite gain at all frequencies, so that when feedback is applied, the voltage differential between the two inputs will be zero. A real amplifier has finite gain that decreases with increasing frequency, resulting in a small voltage across the inputs that increases with signal frequency. In a typical chopper-stabilized amplifier, the ac voltage is modulated by the chopping frequency, creating spurious output signals at sum and difference frequencies of the input frequency, the chopping frequency, and their harmonics. The LMC668 combats this problem by injecting a compensation signal into the nulling amplifier. This compensation substantially reduces the levels of intermodulation components at the amplifier output.

OUTPUT CLAMP

When an operational amplifier is overdriven and clips, the feedback loop opens, and the input differential voltage can become quite large. This voltage is equivalent to a large input offset voltage, so the LMC668's offset correction circuitry attempts to compensate for it, and the external capacitors are eventually charged to rather high voltages before the correction circuit saturates. When the overdrive is removed the capacitors can't be immediately discharged so the circuit takes a long time to recover from the saturated condition.

The 14-pin version of the LMC668 includes a circuit whose purpose is to prevent excessive overdrive recovery time by introducing a current path from the amplifier output to the inverting input. This current path is inactive until the output voltage approaches the supply voltage. Just before the onset of clipping, the current path becomes active and clamps the output voltage before it saturates. Since the clamping action occurs within the feedback loop, the input differential voltage will remain near zero volts and long recovery times are eliminated. The clamp circuit is brought into operation by connecting the clamp pin (9) to the inverting input (pin 4). For best performance, the parallel combination of the feedback resistors should be 100 kΩ or higher. A small feedback capacitor (≈10 pF) may be needed to reduce clamp oscillations.

The only disadvantage to the use of the clamp is a slight reduction in output voltage swing (see Typical Performance curves).

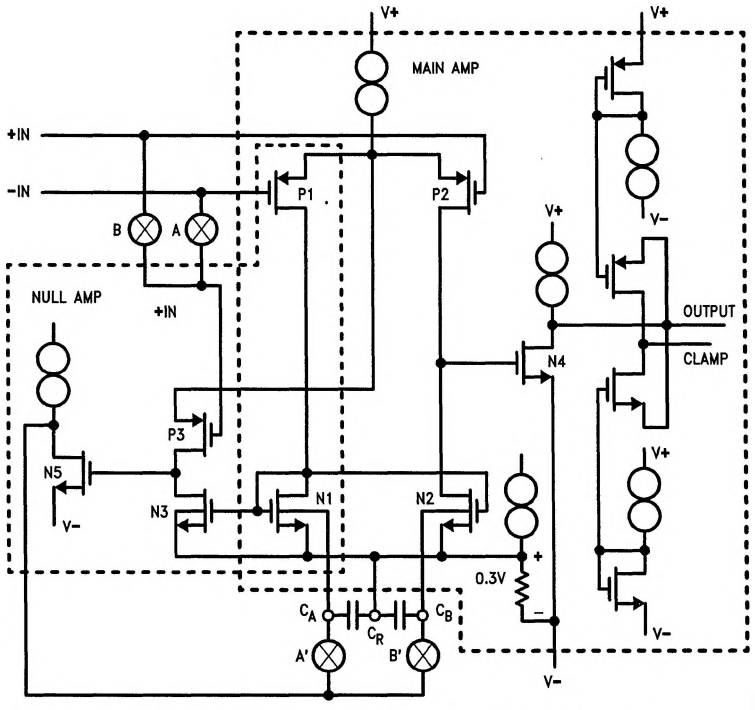

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FIGURE 2. Simplified Schematic of the LMC668 Analog Signal Path

Application Hints (Continued)

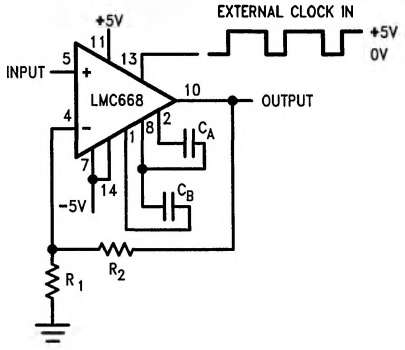

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FIGURE 3. Using External Clock (14-pin LMC668 only). For operation with internal clock, leave pins 13 and 14 open.

THERMOELECTRIC EFFECTS

When dissimilar metals come into contact with one another, thermocouples are created that generate dc error voltages. To reduce the effects of thermocouples, temperatures throughout the sensitive parts of the system should be as similar as possible. Circuitry should be enclosed to limit air movement, junctions with high thermoelectric coefficients should be avoided, and power dissipation should be minimized as much as possible to avoid thermal gradients.

CLOCK CONSIDERATIONS

The internal clock in the LMC668 is set to oscillate around 400 Hz. This signal is available at pin 12 of the 14-pin LMC668. The actual chopping rate is half of the clock frequency. The 14-pin version of the device provides the option of using a different clock frequency from an external source. To do this the INT/EXT pin must be tied to V^- to disable the internal clock *(Figure 3)*. This pin has an internal pull-up, so it may be left open when the internal clock is used. At frequencies below 500 Hz, the external clock's duty cycle is not critical, but above this frequency, a 60% to 80% positive duty cycle will give better results since the null storage capacitors (C_A and C_B) are charged only on the positive half of the clock waveform. A positive duty cycle ensures that the capacitors will be fully charged and any transients will have settled before they are disconnected from the charging circuitry. The maximum recommended clock frequency is approximately 1 kHz. Higher frequencies should be avoided because the offset voltage is degraded at fast chopping rates. The external clock signal should swing between ground and V^+ for supply voltages up to $\pm 6V$, and between V^+ and $V^+ - 6V$ for higher supplies. Voltages outside of this range may cause damage to the IC.

EXTERNAL CAPACITORS

C_A and C_B should be connected from the C_A and C_B pins to the C_R pin. Where possible, the outside foil leads should be connected to C_R. If the internal 200 Hz clock is used, the capacitors should be 0.1 μF. The optimum capacitance varies inversely with chopping frequency. Good quality film capacitors (mylar, polypropylene, polystyrene, polycarbonate, etc.) will give best results. Capacitors with low dielectric absorption (polypropylene and polystyrene) yield the fastest initial settling and turn-on performance. Ceramic capacitors may be adequate in some applications, but these may require several seconds to settle to very low offset values.

LOAD IMPEDANCE

The LMC668 output stage has a relatively high (18 kΩ) output impedance, so the load impedance will have a strong influence on amplifier performance. This is illustrated in the Typical Performance Curves showing open-loop gain for two different load resistors. It is recommended that the load impedance be kept above 10 kΩ to avoid drastic loss of gain, especially at high frequencies. This load resistance will result in a smooth first-order rolloff in the open-loop gain from 0.1 Hz to 2 MHz, with phase errors under 10° in the transition region where the main amplifier takes over from the null amplifier.

LEAKAGE CURRENTS AND INPUT GUARDING

When the low input bias currents of the LMC668 are essential to an application, it is important to take special steps to reduce external sources of leakage currents. Circuit boards must be thoroughly cleaned with appropriate solvents and blown dry with compressed air, and the cleaned traces should be coated with epoxy or silicone rubber to prevent contamination.

Leakage currents due to circuit board traces at supply potentials near the input pins can be excessive for some applications, and these can be minimized by using a guard ring around the input pins. This ring should be tied to a voltage that is near the voltage on the input pins. It will absorb most of the leakage currents from high potential pins and traces.

OUTPUT GLITCHES

The CMOS switches in the LMC668, like all analog switches, produce transients when they are turned on or off. These transients are minimized by careful balancing of the internal switches, but they will still couple to the amplifier output. The transients can be minimized by keeping source impedances low. Input referred glitches on the order of 100 μV are typical with a source impedance of 10 kΩ and Av = 1000. Glitch amplitude increases with higher source resistance and decreases when the clamp circuit is used. At low gains (Av < 10), output glitch amplitude is not as strongly dependent on gain. Typical output glitch amplitudes for $R_1 = R_2 = 100$ kΩ *(Figure 3)*, are 100 mV to 150 mVp-p.