

# LME49721 High Performance, High Fidelity Rail-to-Rail Input/Output Audio Operational Amplifier

Check for Samples: LME49721

#### **FEATURES**

- Rail-to-rail Input and Output
- Easily drives 10kΩ loads to within 10mV of each power supply voltage
- Optimized for superior audio signal fidelity
- Output short circuit protection

#### **APPLICATIONS**

- Ultra high quality portable audio amplification
- High fidelity preamplifiers
- High fidelity multimedia
- State of the art phono pre amps
- High performance professional audio
- High fidelity equalization and crossover networks
- · High performance line drivers
- High performance line receivers
- High fidelity active filters
- DAC I–V converter
- ADC front-end signal conditioning

#### **DESCRIPTION**

The LME49721 is a low distortion, low noise Rail-to-Rail Input/Output operational amplifier optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state-of-the-art circuit design, the LME49721 Rail-to-Rail Input/Output operational amplifier delivers superior signal amplification for outstanding performance. The LME49721 combines a very high slew rate with low THD+N to easily satisfy demanding applications. To ensure that the most challenging loads are driven without compromise, the LME49721 has a high slew rate of  $\pm 8.5 \text{V/µs}$  and an output current capability of  $\pm 9.7 \text{mA}$ . Further, dynamic range is maximized by an output stage that drives  $\pm 10 \text{k}\Omega$  loads to within  $\pm 10 \text{mV}$  of either power supply voltage.

The LME49721 has a wide supply range of 2.2V to 5.5V. Over this supply range the LME49721's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49721 is unity gain stable.

**Table 1. Key Specifications** 

	VALUE	UNIT
Power Supply Voltage Range	2.2V to 5.5	V
Quiescent Current	2.15	mA (typ)
THD+N $(A_V = 2, V_{OUT} = 4V_{p-p}, f_{IN} = 1kHz)$ $R_L = 2k\Omega$ $R_L = 600\Omega$	0.00008 0.0001	% (typ)
Input Noise Density	4nV/√ <del>Hz</del> (typ), @ 1	kHz
Slew Rate	±8.5V/µs (typ)	
Gain Bandwidth Product	20	MHz (typ)
Open Loop Gain ( $R_L = 600\Omega$ )	118	dB (typ)
Input Bias Current	40	fA (typ)
Input Offset Voltage	0.3mV (typ)	
PSRR	103	dB (typ)

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### Typical Connection, Pinout, and Package Marking

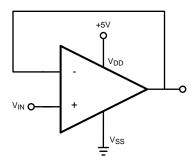


Figure 1. Buffer Amplifier

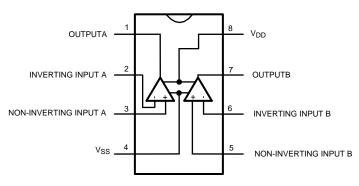
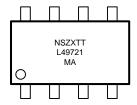


Figure 2.



NS = National Logo, Z = Assembly plant code, X = 1 Digit date code, TT = Lot traceability, L49721 = LME49721, MA = Narrow SOIC package code

Figure 3. Package Marking



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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# Absolute Maximum Ratings (1) (2)

Power Supply Voltage $(V_S = V^+ - V^-)$	6V
Storage Temperature	−65°C to 150°C
Input Voltage	(V-) - 0.7V to (V+) + 0.7V
Output Short Circuit (Note 3)	Continuous
Power Dissipation	Internally Limited
ESD Rating (Note 4)	2000V
ESD Rating (Note 5)	200V
Junction Temperature	150°C
Thermal Resistance, θ <sub>JA</sub> (SO)	165°C/W
Temperature Range, $T_{MIN} \le T_A \le T_{MAX}$	-40°C ≤ T <sub>A</sub> ≤ 85°C
Supply Voltage Range	2.2V ≤ V <sub>S</sub> ≤ 5.5V

 <sup>&</sup>quot;Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified
 The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as

Product Folder Links: LME49721

<sup>(2)</sup> The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.



#### **Electrical Characteristics for the LME49721**

The following specifications apply for the circuit shown in Figure 4.  $V_S = 5V$ ,  $R_L = 10k\Omega$ ,  $R_{SOURCE} = 10\Omega$ ,  $f_{IN} = 1kHz$ , and  $T_A = 10k\Omega$ 25°C, unless otherwise specified.

			LME	49721	Linita	
Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)	
			(1)	(2)	(=	
THD+N	Total Harmonic Distortion + Noise	$A_V = +1, \ V_{OUT} = 2V_{p-p},$ $R_L = 2k\Omega$ $R_L = 600\Omega$	0.0002 0.0002	0.001	% (max)	
IMD	Intermodulation Distortion	$A_V = +1$ , $V_{OUT} = 2V_{p-p}$ , Two-tone, 60Hz & 7kHz 4:1	0.0004		%	
GBWP	Gain Bandwidth Product		20	15	MHz (min)	
SR	Slew Rate	A <sub>V</sub> = +1	8.5		V/µs (min)	
FPBW	Full Power Bandwidth	V <sub>OUT</sub> = 1V <sub>P-P</sub> , –3dB referenced to output magnitude at f = 1kHz	2.2		MHz	
t <sub>s</sub>	Settling time	A <sub>V</sub> = 1, 4V step 0.1% error range	800		ns	
۵	Equivalent Input Noise Voltage	f <sub>BW</sub> = 20Hz to 20kHz, A-weighted	.707	1.13	μV <sub>P-P</sub> (max)	
e <sub>n</sub>	Equivalent Input Noise Density	f = 1kHz A-weighted	4	6	nV <b>/</b> √Hz (max)	
In	Current Noise Density	f = 10kHz	4.0		fA <b>/</b> √Hz	
V <sub>OS</sub>	Offset Voltage		0.3	1.5	mV (max)	
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Voltage Drift vs Temperature	40°C ≤ T <sub>A</sub> ≤ 85°C	1.1		μV/°C	
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage		103	85	dB (min)	
ISO <sub>CH-CH</sub>	Channel-to-Channel Isolation	$f_{IN} = 1kHz$	117		dB	
$I_{B}$	Input Bias Current	$V_{CM} = V_S/2$	40		fA	
$\Delta I_{OS}/\Delta Temp$	Input Bias Current Drift vs Temperature	-40°C ≤ T <sub>A</sub> ≤ 85°C	48		fA/°C	
Ios	Input Offset Current	$V_{CM} = V_S/2$	60		fA	
V <sub>IN-CM</sub>	Common-Mode Input Voltage Range			(V+) - 0.1 (V-) + 0.1	V (min)	
CMRR	Common-Mode Rejection	$V_{SS}$ - 100mV < $V_{CM}$ < $V_{DD}$ + 100mV	93	70	dB (min)	
	1/f Corner Frequency		2000		Hz	
		$V_{SS}$ - 200mV < $V_{OUT}$ < $V_{DD}$ + 200mV				
٨	Open Lean Voltage Gain	$R_L = 600\Omega$	118	100	dB (min)	
A <sub>VOL</sub>	Open Loop Voltage Gain	$R_L = 2k\Omega$	122		dB (min)	
		$R_L = 10k\Omega$	130	115	dB (min)	
		$R_L = 600\Omega$	$V_{DD} - 30 mV$	$V_{DD} - 80 mV$	V (min)	
V	Output Voltage Swing	KL = 00022	$V_{SS}$ + 30mV	V <sub>SS</sub> + 80mV	V (min)	
V <sub>OUTMIN</sub>	Output Voltage Swing	$R_{L} = 10k\Omega, V_{S} = 5.0V$	$V_{DD} - 10 mV$	$V_{DD} - 20 mV$	V (min)	
		$N_L = 10K22$ , $V_S = 5.0V$	V <sub>SS</sub> + 10mV	V <sub>SS</sub> + 20mV	V (min)	
I <sub>OUT</sub>	Output Current	$R_L = 250\Omega, V_S = 5.0V$	9.7	9.3	mA (min)	
I <sub>OUT-SC</sub>	Short Circuit Current		100		mA	
R <sub>OUT</sub>	Output Impedance	f <sub>IN</sub> = 10kHz Closed-Loop Open-Loop	0.01 46		Ω	
I <sub>S</sub>	Quiescent Current per Amplifier	I <sub>OUT</sub> = 0mA	2.15	3.25	mA (max)	

<sup>(1)</sup> Typical values represent most likely parametric norms at  $T_A = +25$ °C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Product Folder Links: LME49721

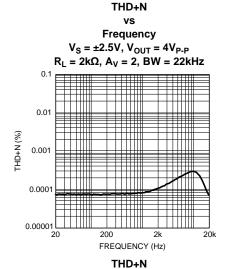
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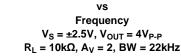
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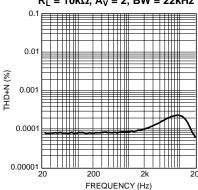


#### **Typical Performance Characteristics**

Graphs were taken in dual supply configuration.





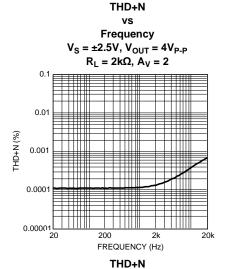


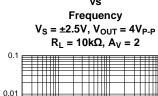
 $\begin{array}{c} \text{Vs} \\ \text{Frequency} \\ \text{V}_{\text{S}} = \pm 2.5 \text{V}, \text{V}_{\text{OUT}} = 4 \text{V}_{\text{P-P}} \\ \text{R}_{\text{L}} = 600 \Omega, \text{A}_{\text{V}} = 2, \text{BW} = 22 \text{kHz} \\ \\ 0.01 \\ \hline \\ 0.0001 \\ \hline \\ 0.00001 \\ \end{array}$ 

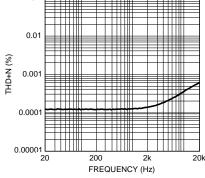
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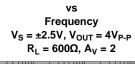
FREQUENCY (Hz)

THD+N

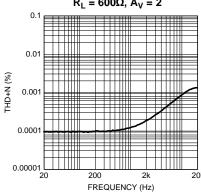






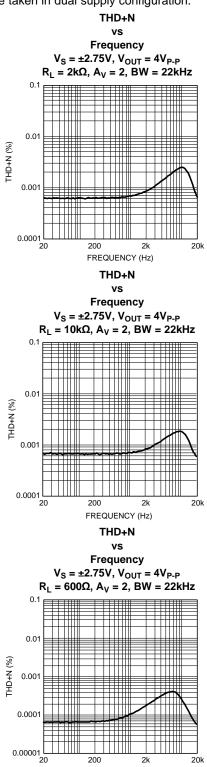


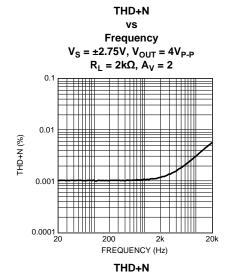
THD+N

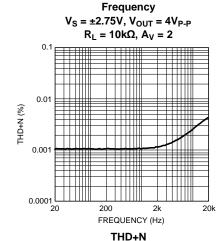




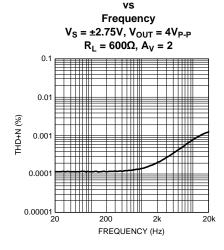
Graphs were taken in dual supply configuration.







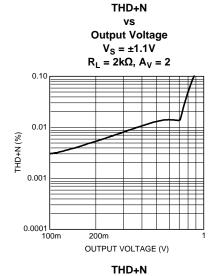
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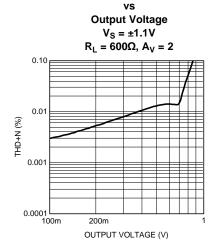


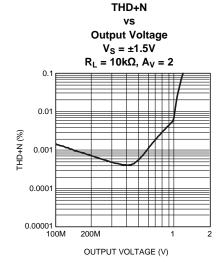
FREQUENCY (Hz)

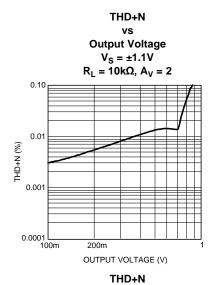


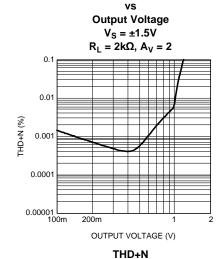
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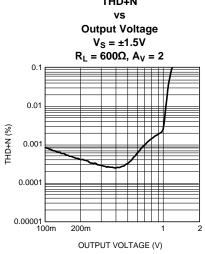






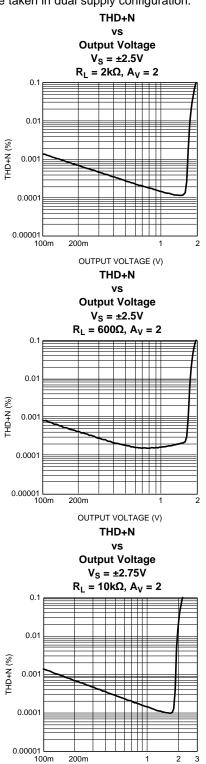


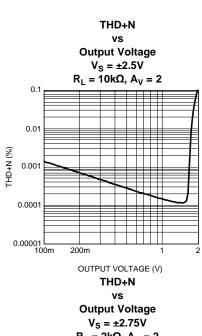


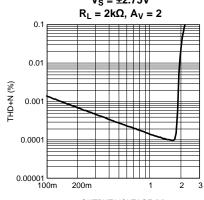


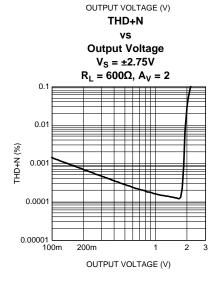


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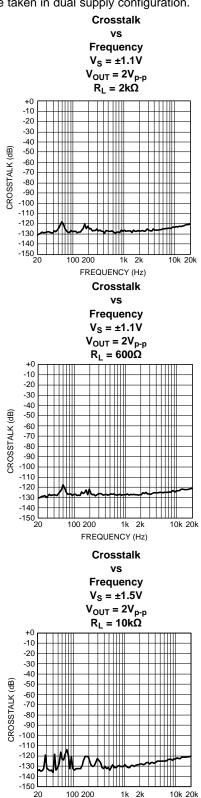


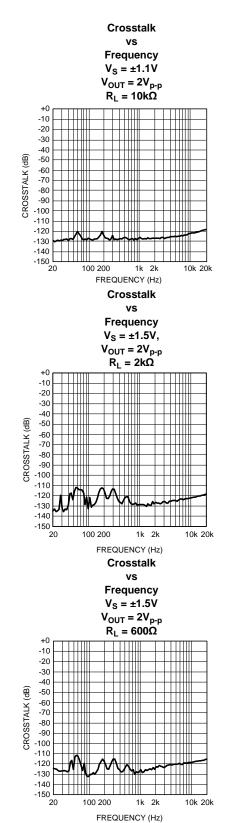
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OUTPUT VOLTAGE (V)



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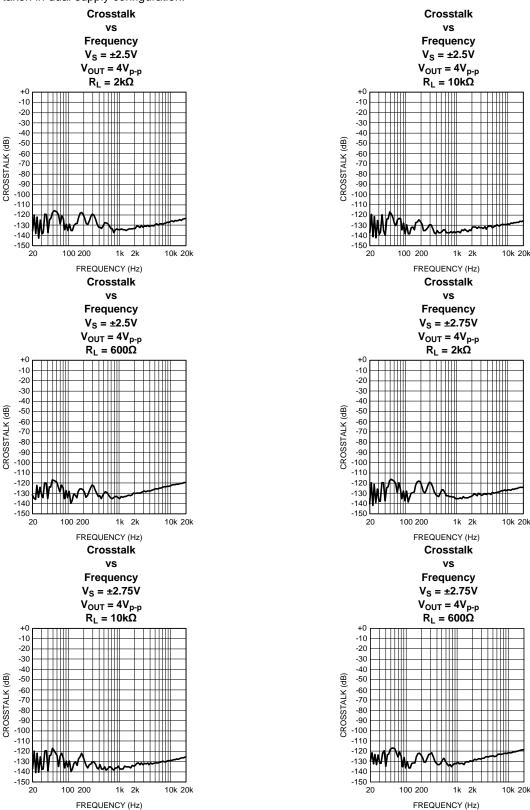




FREQUENCY (Hz)

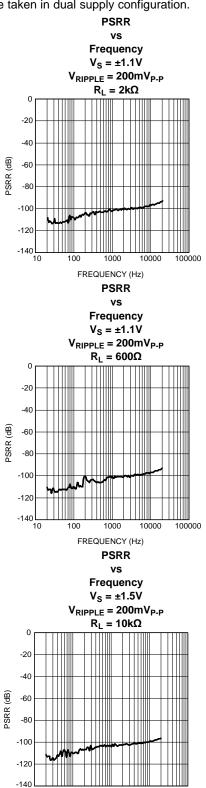


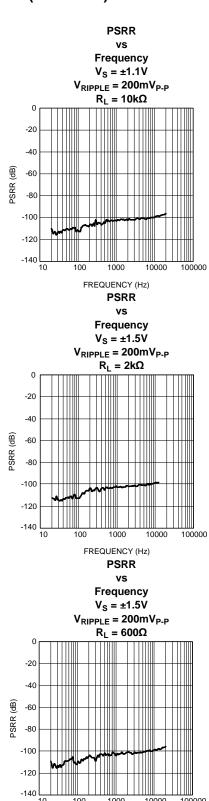
Graphs were taken in dual supply configuration.





Graphs were taken in dual supply configuration.



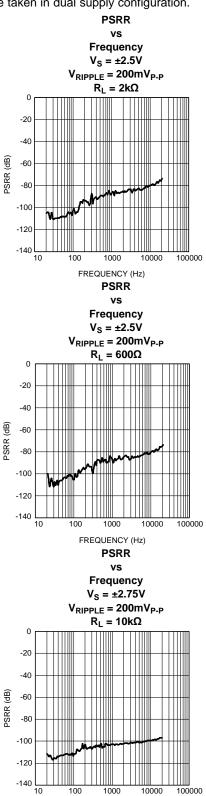


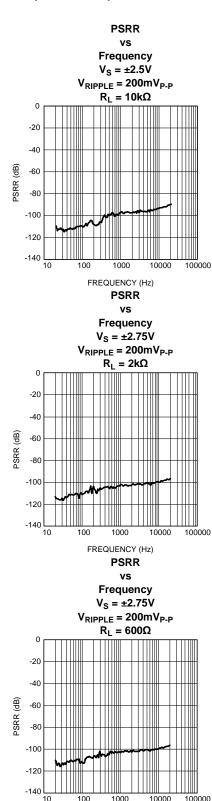
FREQUENCY (Hz)

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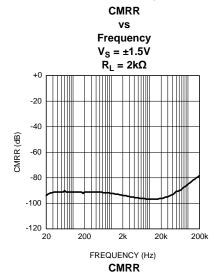


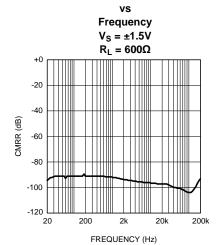
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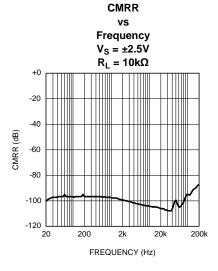
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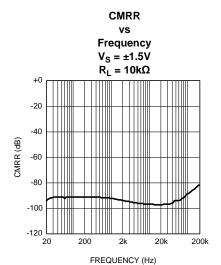


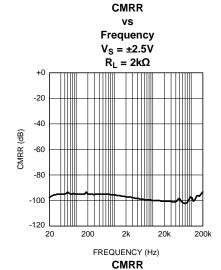
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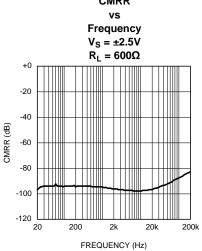






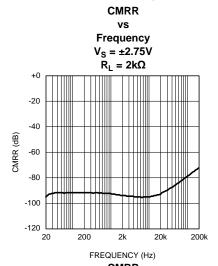


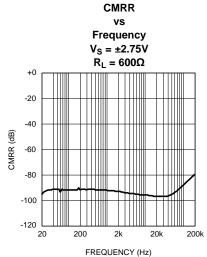


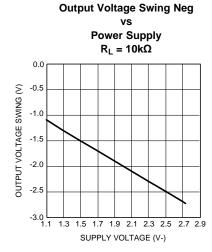


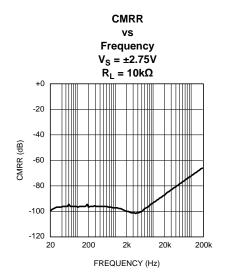


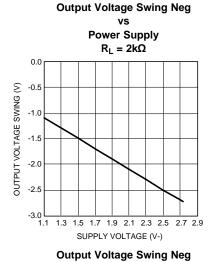
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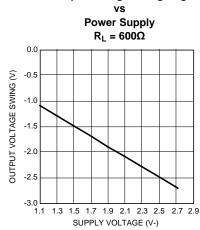






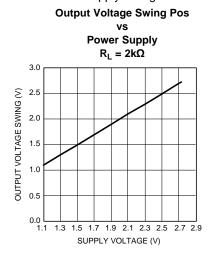




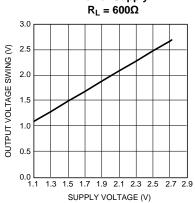




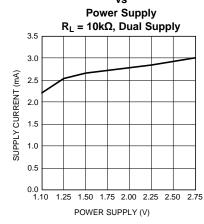
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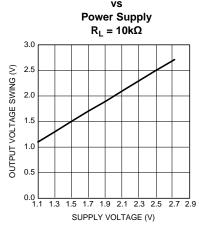
### Output Voltage Swing Pos vs Power Supply



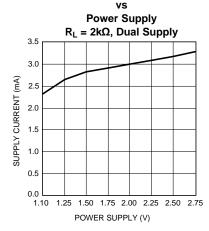
# Supply Current per amplifier vs



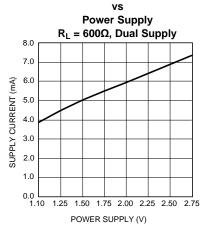




# Supply Current per amplifier



#### Supply Current per amplifier



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#### **Application Information**

#### **DISTORTION MEASUREMENTS**

The vanishingly low residual distortion produced by LME49721 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49721's low residual is an input referred internal error. As shown in Figure 4, adding the  $10\Omega$  resistor connected between a the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 4.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so, produces distortion components that are within equipments capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

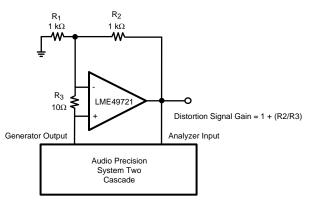


Figure 4. THD+N and IMD Distortion Test Circuit with  $A_V = 2$ 

#### **OPERATING RATINGS AND BASIC DESIGN GUIDELINES**

The LME49721 has a supply voltage range from +2.2V to +5.5V single supply or ±1.1 to ±2.75V dual supply.

Bypassed capacitors for the supplies should be placed as close to the amplifier as possible. This will help minimize any inductance between the power supply and the supply pins. In addition to a 10µF capacitor, a 0.1µF capacitor is also recommended in CMOS amplifiers.

The amplifier's inputs lead lengths should also be as short as possible. If the op amp does not have a bypass capacitor, it may oscillate.

#### **BASIC AMPLIFIER CONFIGURATIONS**

The LME49721 may be operated with either a single supply or dual supplies. Figure 5 shows the typical connection for a single supply inverting amplifier. The output voltage for a single supply amplifier will be centered around the common-mode voltage Vcm. Note, the voltage applied to the Vcm insures the output stays above ground. Typically, the Vcm should be equal to  $V_{DD}/2$ . This is done by putting a resistor divider ckt at this node, see Figure 5.

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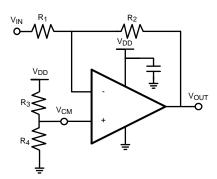


Figure 5. Single Supply Inverting Op Amp

Figure 6 shows the typical connection for a dual supply inverting amplifier. The output voltage is centered on zero.

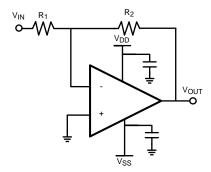


Figure 6. Dual Supply Inverting Op Amp

Figure 7 shows the typical connection for the Buffer Amplifier or also called a Voltage Follower. A Buffer Amplifier can be used to solve impedance matching problems, to reduce power consumption in the source, or to drive heavy loads. The input impedance of the op amp is very high. Therefore, the input of the op amp does not load down the source. The output impedance on the other hand is very low. It allows the load to either supply or absorb energy to a circuit while a secondary voltage source dissipates energy from a circuit. The Buffer is a unity stable amplifier, 1V/V. Although the feedback loop is tied from the output of the amplifier to the inverting input, the gain is still positive. Note, if a positive feedback is used, the amplifier will most likely drive to either rail at the output.

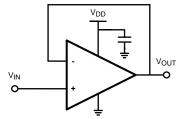


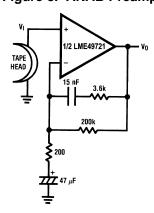
Figure 7. Buffer

Product Folder Links: LME49721



# **Typical Applications**

Figure 8. ANAB Preamp



 $A_V = 34.5$  F = 1 kHz  $E_n = 0.38 \text{ }\mu\text{V}$  A Weighted

Figure 9. NAB Preamp Voltage Gain vs Frequency

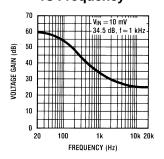
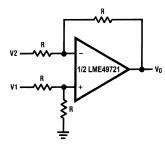
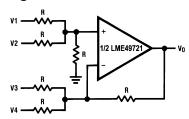


Figure 10. Balanced to Single Ended Converter



 $V_O = V1-V2$ 

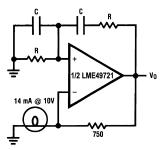
Figure 11. Adder/Subtracter



 $V_0 = V1 + V2 - V3 - V4$ 

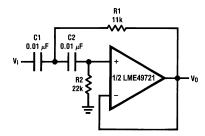


Figure 12. Sine Wave Oscillator



$$f_0 = \frac{1}{2\pi RC}$$

Figure 13. Second Order High Pass Filter (Butterworth)

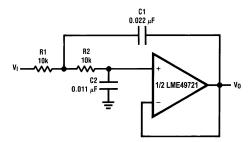


if C1 = C2 = C 
$$R1 = \frac{\sqrt{2}}{2\omega_0 C}$$

R2 = 2•R1

Illustration is  $f_0 = 1 \text{ kHz}$ 

Figure 14. Second Order Low Pass Filter (Butterworth)



if R1 = R2 = R

$$C1 = \frac{\sqrt{2}}{\omega_0 R}$$

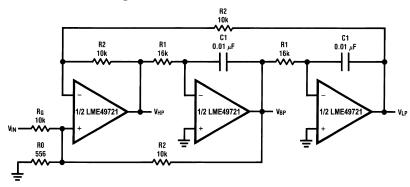
 $C2 = \frac{C1}{2}$ 

Illustration is  $f_0 = 1 \text{ kHz}$ 

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Figure 15. State Variable Filter



$$\begin{split} f_0 &= \frac{1}{2\pi C 1R1}, Q = \frac{1}{2} \left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG} \end{split}$$
 Illustration is  $f_0 = 1$  kHz,  $Q = 10$ ,  $A_{BP} = 1$ 

Figure 16. AC/DC Converter

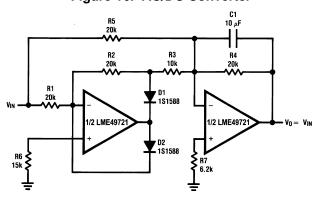


Figure 17. 2 Channel Panning Circuit (Pan Pot)

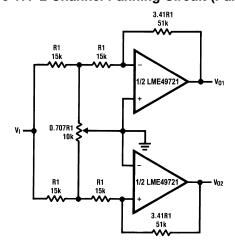




Figure 18. Line Driver

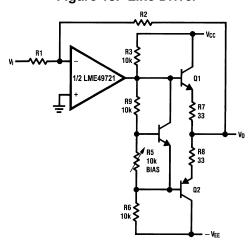
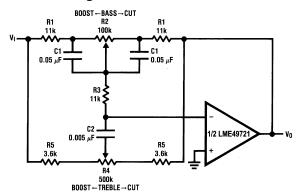


Figure 19. Tone Control



$$\begin{split} f_L &= \frac{1}{2\pi R 2C1}, f_{LB} = \frac{1}{2\pi R 1C1} \\ f_H &= \frac{1}{2\pi R SC2}, f_{HB} = \frac{1}{2\pi (R1 + R5 + 2R3)C2} \\ Illustration is: \\ f_L &= 32 \ Hz, \ f_{LB} = 320 \ Hz \\ f_H &= 11 \ kHz, \ f_{HB} = 1.1 \ kHz \end{split}$$

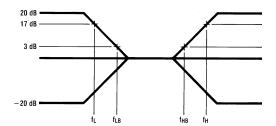
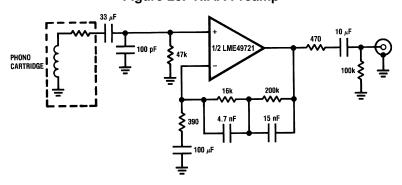


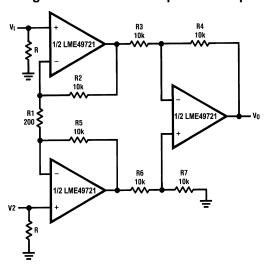


Figure 20. RIAA Preamp



 $\begin{array}{l} A_{\nu}=35~\text{dB} \\ E_{n}=0.33~\mu\text{V} \\ \text{S/N}=90~\text{dB} \\ f=1~\text{kHz} \\ \text{A Weighted}, \text{V}_{\text{IN}}=10~\text{mV} \\ @f=1~\text{kHz} \end{array}$ 

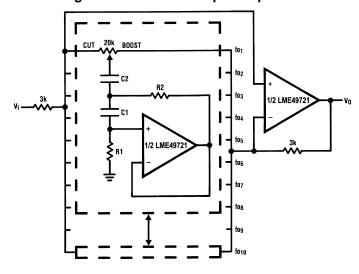
Figure 21. Balanced Input Mic Amp



If R2 = R5, R3 = R6, R4 = R7  $V0 = \left(1 + \frac{2R2}{R1}\right) \frac{R4}{R3} (V2 - V1)$  Illustration is: V0 = 101 (V2 - V1)



Figure 22. 10 Band Graphic Equalizer



fo (Hz)	C <sub>1</sub>	C <sub>2</sub>	R <sub>1</sub>	R <sub>2</sub>
32	0.12μF	4.7µF	75kΩ	500Ω
64	0.056µF	3.3µF	68kΩ	510Ω
125	0.033µF	1.5µF	62kΩ	510Ω
250	0.015µF	0.82µF	68kΩ	470Ω
500	8200pF	0.39µF	62kΩ	470Ω
1k	3900pF	0.22µF	68kΩ	470Ω
2k	2000pF	0.1µF	68kΩ	470Ω
4k	1100pF	0.056µF	62kΩ	470Ω
8k	510pF	0.022µF	68kΩ	510Ω
16k	330pF	0.012µF	51kΩ	510Ω

# **Revision History**

Rev	Date	Description
1.0	09/26/07	Initial release.
1.1	10/01/07	Input more info under the Buffer Amplifier.
1.2	04/21/10	Added the Ordering Information table.

Product Folder Links: *LME49721* 





17-Nov-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type		Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Samples
	(1)		Drawing			(2)		(3)	(Requires Login)
LME49721MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LME49721MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49721MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

# **PACKAGE MATERIALS INFORMATION**

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49721MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

# D (R-PDSO-G8)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



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