LMH6628EP Enhanced Plastic Dual Wideband, Low Noise, Voltage Feedback Op Amp

Check for Samples: LMH6628EP

FEATURES

- **Wide unity gain bandwidth: 300MHz**
- **Low noise: 2nV/ $\sqrt{Hz}$**
- **Low Distortion: −65/−74dBc (10MHz)**
- **Settling time: 12ns to 0.1%**
- **Wide supply voltage range: ±2.5V to ±6V**
- **High output current: ±85mA**
- **Improved replacement for CLC428**

APPLICATIONS

- **High speed dual op amp**
- **Low noise integrators**
- **Selected Military Applications**
- **Selected Avionics Applications**

DESCRIPTION

The National LMH6628EP is a high speed dual op amp that offers a traditional voltage feedback topology featuring unity gain stability and slew enhanced circuitry. The LMH6628EP's low noise and very low harmonic distortion combine to form a wide dynamic range op amp that operates from a single (5V to 12V) or dual (±5V) power supply.

Each of the LMH6628EP's closely matched channels provides a 300MHz unity gain bandwidth and low input voltage noise density (2nV/ $\sqrt{Hz}$). Low 2nd/3rd harmonic distortion (−65/−74dBc at 10MHz) make the LMH6628EP a perfect wide dynamic range amplifier for matched I/Q channels.

With its fast and accurate settling (12ns to 0.1%), the LMH6628EP is also an excellent choice for wide dynamic range, anti-aliasing filters to buffer the inputs of hi resolution analog-to-digital converters. Combining the LMH6628EP's two tightly matched amplifiers in a single 8-pin SOIC package reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

The LMH6628EP is fabricated using National's VIP10™ complimentary bipolar process.

To reduce design times and assist in board layout, the LMH6628EP is supported by an evaluation board (CLC730036).

ENHANCED PLASTIC

- Extended Temperature Performance of −40°C to +85°C
- Baseline Control - Single Fab & Assembly Site
- Process Change Notification (PCN)
- Qualification & Reliability Data
- Solder (PbSn) Lead Finish is standard
- Enhanced Diminishing Manufacturing Sources (DMS) Support

Connection Diagram

8-Pin SOIC

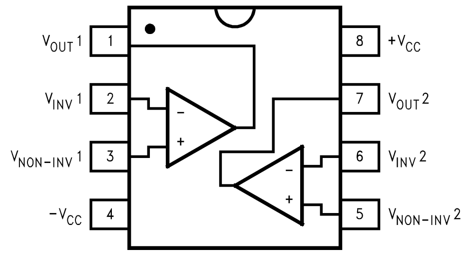


Figure 1. Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Human Body Model	2kV
Machine Model	200V
Supply Voltage	13.5
Short Circuit Current	(3)
Common-Mode Input Voltage	$V^+ - V^-$
Differential Input Voltage	$V^+ - V^-$
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering 10 sec)	+300°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.
(2) Human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω In series with 200pF.
(3) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

Operating Ratings (1)

Thermal Resistance (2)			
Package	(θ_{JC})	(θ_{JA})	
SOIC	65°C/W	145°C/W	
Temperature Range			−40°C to +85°C
Nominal Supply Voltage			±2.5V to ±6V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Electrical Characteristics (1)

V_{CC} = ±5V, A_V = +2V/V, R_F = 100Ω, R_G = 100Ω, R_L = 100Ω; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GB	Gain Bandwidth Product	V_O < 0.5V_{PP}		200		MHz
SSBW	-3dB Bandwidth, A_V = +1	V_O < 0.5V_{PP}	180	300		MHz
SSBW	-3dB Bandwidth, A_V = +2	V_O < 0.5V_{PP}		100		MHz
GFL	Gain Flatness	V_O< 0.5V_{PP}				
GFP	Peaking	DC to 200MHz		0.0		dB
GFR	Rolloff	DC to 20MHz		.1		dB
LPD	Linear Phase Deviation	DC to 20MHz		.1		deg
Time Domain Response						
TR	Rise and Fall Time	1V Step		4		ns
TS	Settling Time	2V Step to 0.1%		12		ns
OS	Overshoot	1V Step		1		%
SR	Slew Rate	4V Step	300	550		V/µs
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	1V_{PP}, 10MHz		−65		dBc
HD3	3rd Harmonic Distortion	1V_{PP}, 10MHz		−74		dBc
	Equivalent Input Noise					
V_N	Voltage	1MHz to 100MHz		2		nV/ $\sqrt{Hz}$
I_N	Current	1MHz to 100MHz		2		pA/ $\sqrt{Hz}$
XTLKA	Crosstalk	Input Referred, 10MHz		−62		dB
Static, DC Performance						
G_{OL}	Open-Loop Gain		56 **53**	63		dB
V_{IO}	Input Offset Voltage			±.5	±2 **±2.6**	mV
DV_{IO}	Average Drift			5		µV/°C
I_{BN}	Input Bias Current			±.7	±20 **±30**	µA
DI_{BN}	Average Drift			150		nA/°C
I_{OS}	Input Offset Current			0.3	±6	µA
I_{OSD}	Average Drift			5		nA/°C
PSRR	Power Supply Rejection Ratio		60 **46**	70		dB
CMRR	Common-Mode Rejection Ratio		57 **54**	62		dB
I_{CC}	Supply Current	Per Channel, R_L = ∞	7.5 **7.0**	9	12 **12.5**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Common-Mode		500		kΩ
		Differential-Mode		200		kΩ
C_{IN}	Input Capacitance	Common-Mode		1.5		pF
		Differential-Mode		1.5		pF
R_{OUT}	Output Resistance	Closed-Loop		.1		Ω

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Note 6 for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

Electrical Characteristics [1] (continued)

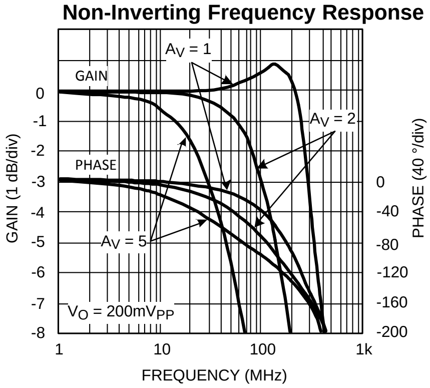
V_{CC} = ±5V, A_V = +2V/V, R_F = 100Ω, R_G = 100Ω, R_L = 100Ω; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage Range	R_L = ∞		±3.8		V
V_{OL}		R_L = 100Ω	±3.2 **±3.1**	±3.5		V
CMIR	Input Voltage Range	Common- Mode		±3.7		V
I_O	Output Current		±50	±85		mA

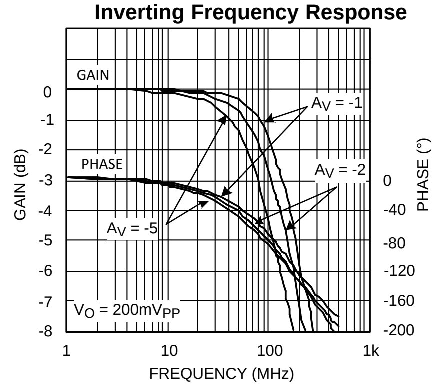
Typical Performance Characteristics

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_f =100Ω, R_L = 100Ω, unless specified)

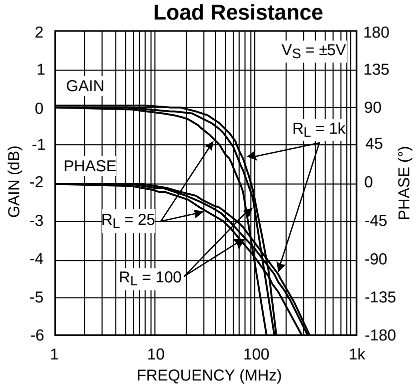
Non-Inverting Frequency Response



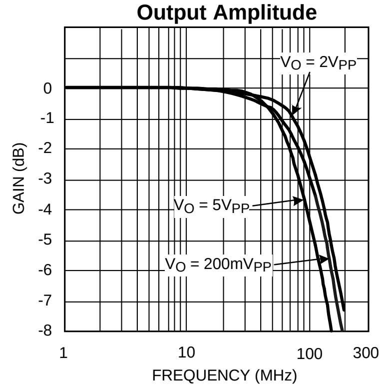
Inverting Frequency Response



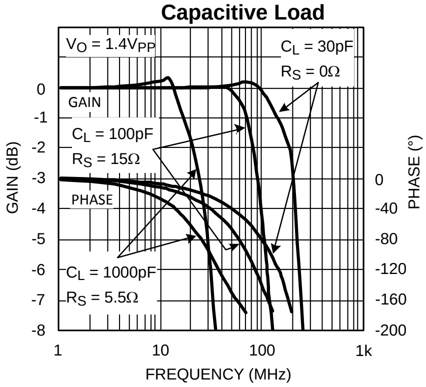
Frequency Response vs. Load Resistance



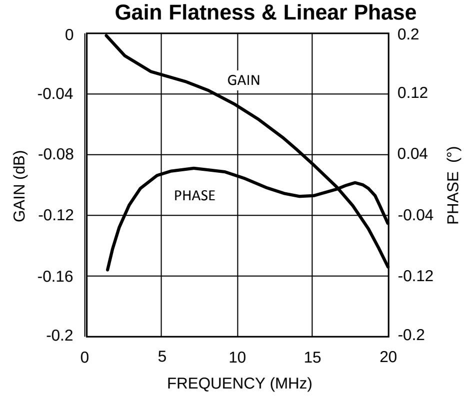
Frequency Response vs. Output Amplitude



Frequency Response vs. Capacitive Load



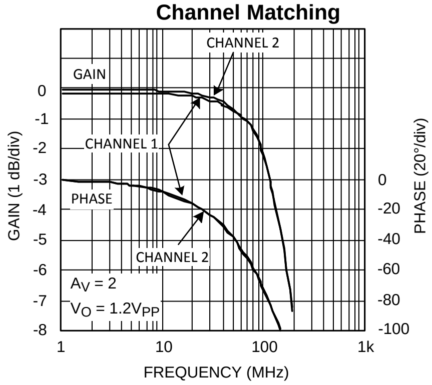
Gain Flatness & Linear Phase



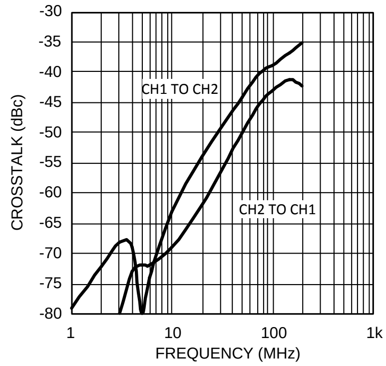
Typical Performance Characteristics (continued)

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_f =100Ω, R_L = 100Ω, unless specified)

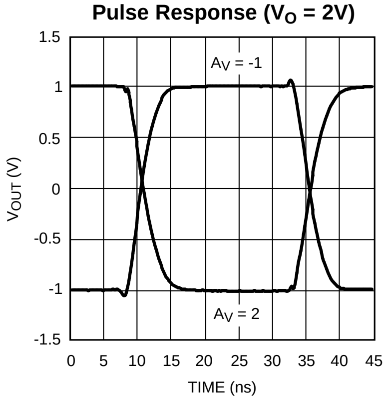
Channel Matching



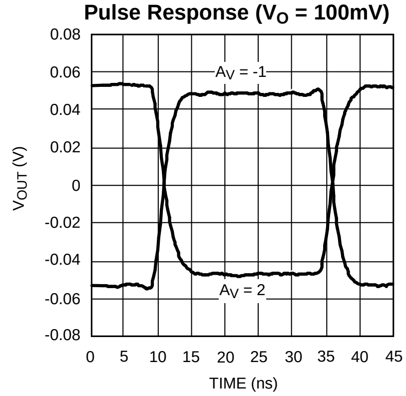
Channel to Channel Crosstalk



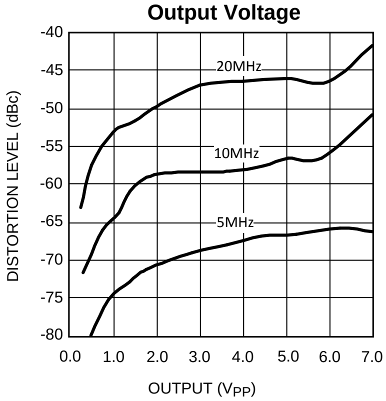
Pulse Response (V_O = 2V)



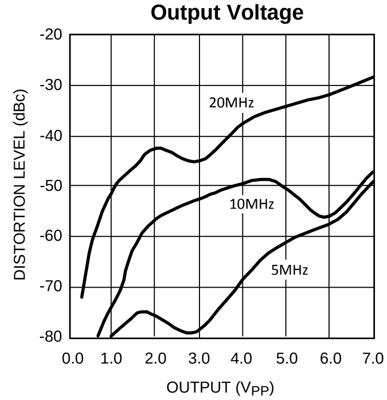
Pulse Response (V_O = 100mV)



2nd Harmonic Distortion vs. Output Voltage



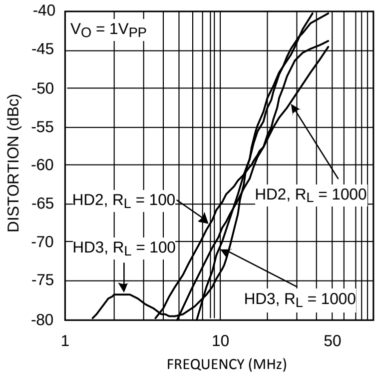
3rd Harmonic Distortion vs. Output Voltage



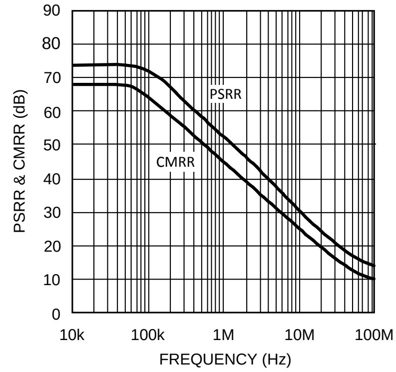
Typical Performance Characteristics (continued)

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_f =100Ω, R_L = 100Ω, unless specified)

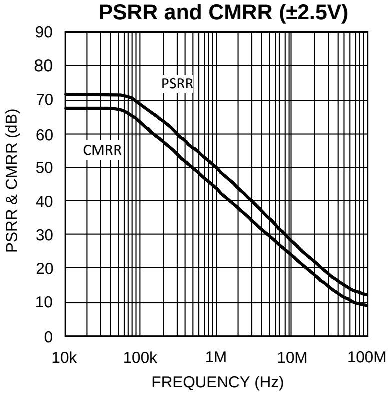
2nd & 3rd Harmonic Distortion vs. Frequency



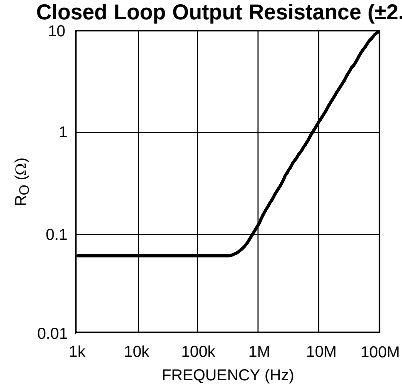
PSRR and CMRR (±5V)



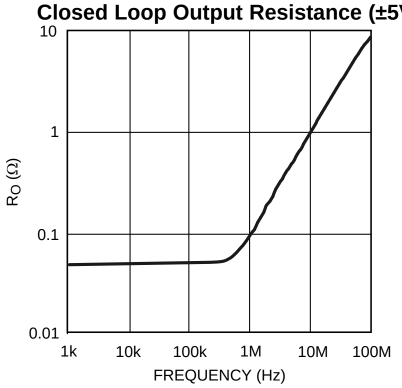
PSRR and CMRR (±2.5V)



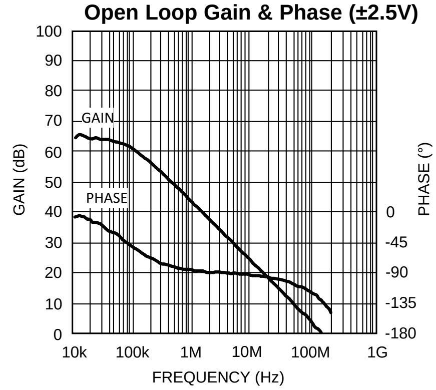
Closed Loop Output Resistance (±2.5V)



Closed Loop Output Resistance (±5V)



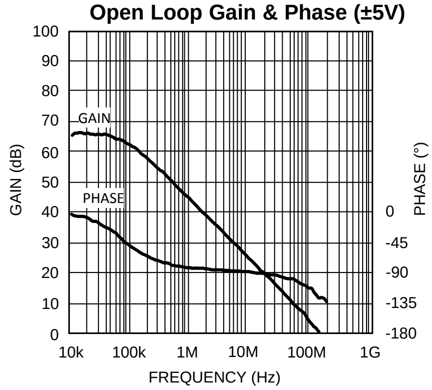
Open Loop Gain & Phase (±2.5V)



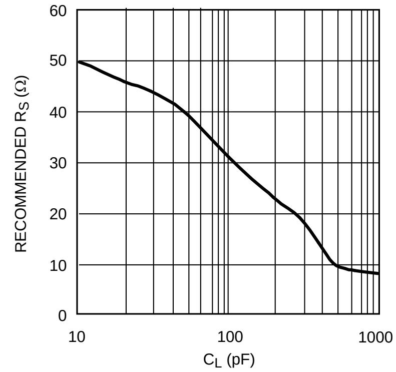
Typical Performance Characteristics (continued)

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_f =100Ω, R_L = 100Ω, unless specified)

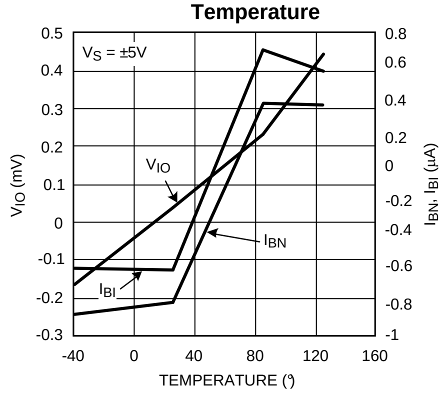
Open Loop Gain & Phase (±5V)



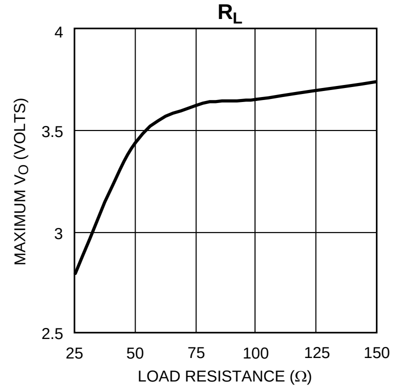
Recommended R_S vs. C_L



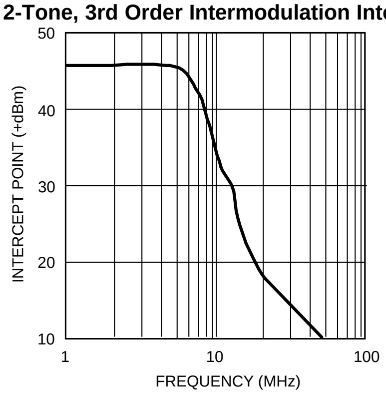
DC Errors vs. Temperature



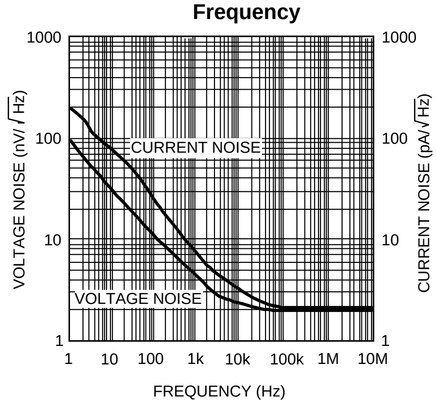
Maximum V_O vs. R_L



2-Tone, 3rd Order Intermodulation Intercept



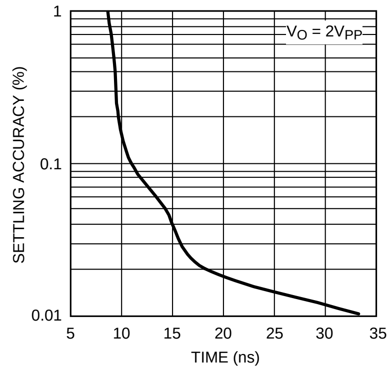
Voltage & Current Noise vs. Frequency



Typical Performance Characteristics (continued)

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_f =100Ω, R_L = 100Ω, unless specified)

Settling Time vs. Accuracy



Application Section

LOW NOISE DESIGN

Ultimate low noise performance from circuit designs using the LMH6628EP requires the proper selection of external resistors. By selecting appropriate low valued resistors for R_F and R_G, amplifier circuits using the LMH6628EP can achieve output noise that is approximately the equivalent voltage input noise of 2nV/ $\sqrt{Hz}$ multiplied by the desired gain (A_V).

DC BIAS CURRENTS AND OFFSET VOLTAGES

Cancellation of the output offset voltage due to input bias currents is possible with the LMH6628EP. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage (V_{OS}) multiplied by the desired gain (A_V). National Application Note OA-7 offers several solutions to further reduce the output offset.

OUTPUT AND SUPPLY CONSIDERATIONS

With ±5V supplies, the LMH6628EP is capable of a typical output swing of ±3.8V under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than 50Ω, the output swing will be limited by the LMH6628EP's output current capability, typically 85mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See the plot labeled "R_S vs. C_L" in the Typical Performance section.

LAYOUT

Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of 0.1μF should be placed as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 for more information. National suggests the 730036 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

ANALOG DELAY CIRCUIT (ALL-PASS NETWORK)

The circuit in Figure 2 implements an all-pass network using the LMH6628EP. A wide bandwidth buffer (LM7121) drives the circuit and provides a high input impedance for the source. As shown in Figure 3, the circuit provides a 13.1ns delay (with R = 40.2Ω, C = 47pF). R_F and R_G should be of equal and low value for parasitic insensitive operation.

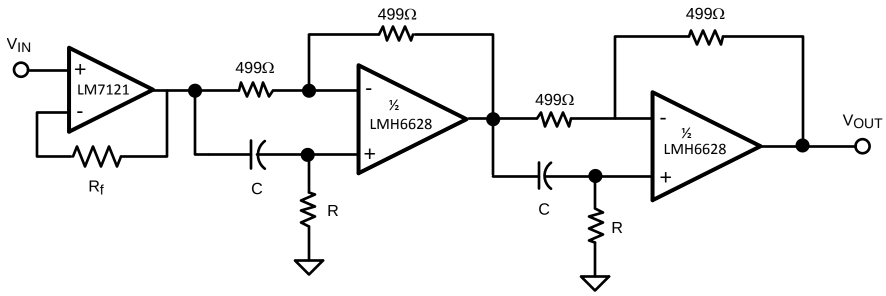


Figure 2.

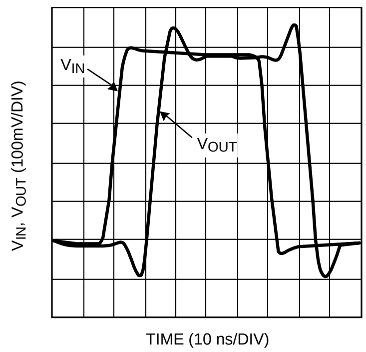


Figure 3. Delay Circuit Response to 0.5V Pulse

The circuit gain is +1 and the delay is determined by the following equations.

$$\tau_{delay} = 2(2RC + T_d) \quad (1)$$

$$T_d = \frac{1}{360}\frac{d\phi}{df}; \quad (2)$$

where T_d is the delay of the op amp at $A_V = +1$.

The LMH6628EP provides a typical delay of 2.8ns at its −3dB point.

FULL DUPLEX DIGITAL OR ANALOG TRANSMISSION

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The LMH6628EP's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in Figure 4, one of the LMH6628EP's amps is used as a "driver" and the other as a difference "receiver" amplifier. The output impedance of the "driver" is essentially zero. The two R's are chosen to match the characteristic impedance of the transmission line. The "driver" op amp gain can be selected for unity or greater.

Receiver amplifier A_2 (B_2) is connected across R and forms differential amplifier for the signals transmitted by driver A_2 (B_2). If R_F equals R_G, receiver A_2 (B_1) will then reject the signals from driver A_1 (B_1) and pass the signals from driver B_1 (A_1).

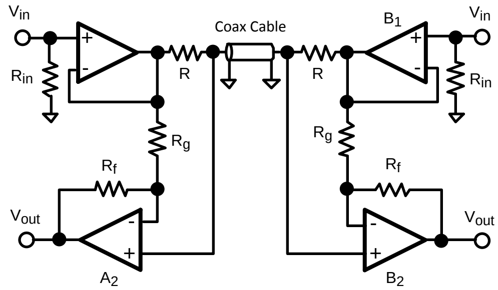


Figure 4. Example Circuit

The output of the receiver amplifier will be:

$$V_{out_{A(B)}} = \frac{1}{2} V_{in_{A(B)}} \left[1 - \frac{R_f}{R_g}\right] + \frac{1}{2} V_{in_{B(A)}} \left[1 + \frac{R_f}{R_g}\right] \tag{3}$$

Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of Figure 5 shows the simultaneous reception of signals transmitted at 1MHz and 10MHz.

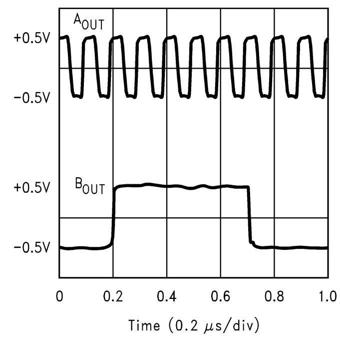


Figure 5. Simultaneous 1- and 10-MHz Signal Reception

POSITIVE PEAK DETECTOR

The LMH6628EP's dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in Figure 6.

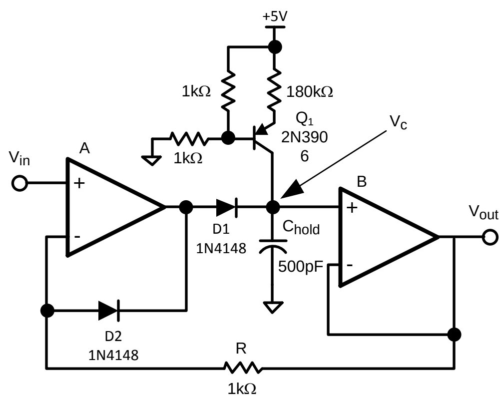


Figure 6. Unity-Gain Peak Detector Circuit

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging C_{hold}. A plot of the circuit's performance is shown in Figure 7 with a 1MHz sinusoidal input.

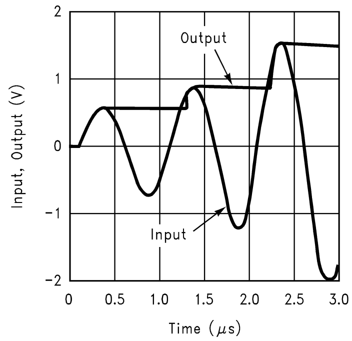


Figure 7. Circuit Performance with 1-MHz Sinusoidal Input

A current source, built around Q1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D2 prevents negative saturation when V_{IN} is less than V_C. A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

ADJUSTABLE OR BANDPASS EQUALIZER

A "boost" equalizer can be made with the LMH6628EP by summing a bandpass response with the input signal, as shown in Figure 8.

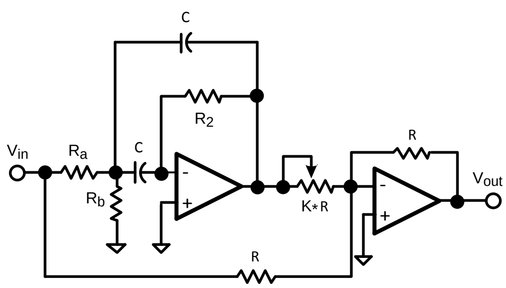


Figure 8. Boost Equalizer Sum

The overall transfer function is shown in Eq. 5.

$$\frac{V_{out}}{V_{in}} = \left[\frac{R_b}{K(R_a + R_b)}\right] \frac{s2Q\omega_o}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} - 1 \quad (4)$$

To build a boost circuit, use the design equations Eq. 6 and Eq. 7.

$$\frac{R_2C}{2} = \frac{Q}{\omega_o} \quad (5)$$

$$2C\,(R_a \| R_b) = \frac{1}{Q\omega_o} \quad (6)$$

Select R_2 and C using Eq. 6. Use reasonable values for high frequency circuits - R_2 between 10Ω and 5kΩ, C between 10pF and 2000pF. Use Eq. 7 to determine the parallel combination of R_a and R_b. Select R_a and R_b by either the 10Ω to 5kΩ criteria or by other requirements based on the impedance V_{in} is capable of driving. Finish the design by determining the value of K from Eq. 8.

$$\text{Peak Gain} = \frac{V_{out}}{V_{in}}(\omega_o) = \frac{R_2}{2KR_a} - 1 \quad (7)$$

Figure 9 shows an example of the response of the circuit of Figure 9, where f_o is 2.3MHz. The component values are as follows: R_a=2.1kΩ, R_b = 68.5Ω, R_2 = 4.22kΩ, R = 500Ω, KR = 50Ω, C = 120pF.

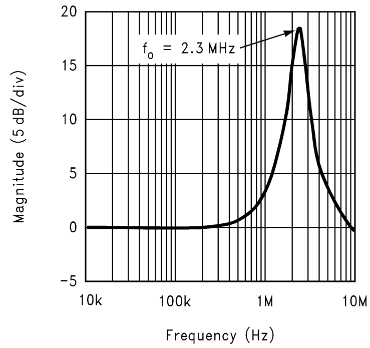


Figure 9. Example Response

IMPORTANT NOTICE

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