LMH6640 TFT-LCD Single, 16V Rail-to-Rail High Output Operational Amplifier

Check for Samples: LMH6640

FEATURES

- (V_S = 16V, R_L= 2 kΩ to $V^+/2$, 25°C, Typical Values Unless Specified)
- Supply current (no load) 4 mA
- Output resistance (closed loop 1 MHz) 0.35Ω
- −3 dB BW (A_V = 1) 190 MHz
- Settling time (±0.1%, 2 V_{PP}) 35 ns
- Input common mode voltage −0.3V to 15.1V
- Output voltage swing 100 mV from rails
- Linear output current ±100 mA
- Total harmonic distortion (2 V_{PP}, 5 MHz) −64 dBc
- Fully characterized for: 5V & 16V
- No output phase reversal with CMVR exceeded
- Differential gain (R_L = 150Ω) 0.12%
- Differential phase (R_L = 150Ω) 0.12°

APPLICATIONS

- TFT panel V_{COM} buffer amplifier
- Active filters
- CD/DVD ROM
- ADC buffer amplifier
- Portable video
- Current sense buffer

DESCRIPTION

The LMH™6640 is a voltage feedback operational amplifier with a rail-to-rail output drive capability of 100 mA. Employing National's patented VIP10 process, the LMH6640 delivers a bandwidth of 190 MHz at a current consumption of only 4mA. An input common mode voltage range extending to 0.3V below the V− and to within 0.9V of V^+, makes the LMH6640 a true single supply op-amp. The output voltage range extends to within 100 mV of either supply rail providing the user with a dynamic range that is especially desirable in low voltage applications.

The LMH6640 offers a slew rate of 170 V/µs resulting in a full power bandwidth of approximately 28 MHz with 5V single supply (2 V_{PP}, −1 dB). Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic for any gain setting including +1, and excellent specifications for driving video cables including total harmonic distortion of −64 dBc @ 5 MHz, differential gain of 0.12% and differential phase of 0.12°.

Typical Application

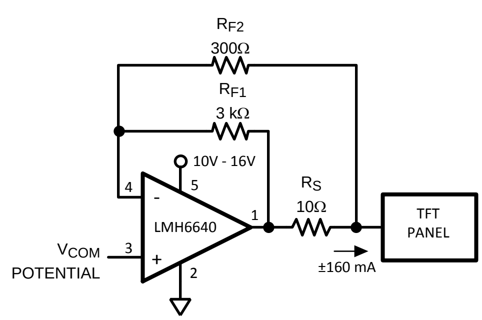


Figure 1. Typical Application as a TFT Panel V_{COM} Driver

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

ESD Tolerance [2]	
Human Body Model	2 KV
Machine Model	200V
V_{IN} Differential	±2.5V
Input Current	±10 mA
Supply Voltages ($V^+ – V^−$)	18V
Voltage at Input/Output Pins	V^+ +0.8V, $V^−$ −0.8V
Storage Temperature Range	−65°C to +150°C
Junction Temperature [3]	+150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

(1) Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Human body model, 1.5 kΩ in series with 100 pF. Machine Model, 0Ω in series with 200 pF.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}-T_A) / θ_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings [1]

Supply Voltage ($V^+ – V^−$)	4.5V to 16V
Operating Temperature Range [2]	−40°C to +85°C
Package Thermal Resistance [2]	
5-Pin SOT23	265°C/W

(1) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 °C Short circuit test is a momentary test. Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}-T_A) / θ_{JA}$. All numbers apply for packages soldered directly onto a PC board.

5V Electrical Characteristics

Unless otherwise specified, All limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_O = V_{CM} = $V^+/2$ and R_L = 2 kΩ to $V^+/2$. **Boldface** limits apply at temperature extremes. (1)

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
BW	−3 dB Bandwidth	A_V = +1 (R_L = 100Ω)		150		MHz
		A_V = −1 (R_L = 100Ω)		58		
$BW_{0.1\ dB}$	0.1 dB Gain Flatness	A_V = −3		18		MHz
FPBW	Full Power Bandwidth	A_V = +1, V_{OUT} = 2 V_{PP}, −1 dB		28		MHz
LSBW	-3 dB Bandwidth	A_V = +1, V_O = 2 V_{PP} (R_L = 100Ω)		32		MHz
GBW	Gain Bandwidth Product	A_V = +1, (R_L = 100Ω)		59		MHz
SR	Slew Rate (4)	A_V = −1		170		V/μs
e_n	Input Referred Voltage Noise	f = 10 kHz		23		$nV/\sqrt{Hz}$
		f = 1 MHz		15		
i_n	Input Referred Current Noise	f = 10 kHz		1.1		$pA/\sqrt{Hz}$
		f = 1 MHz		0.7		
THD	Total Harmonic Distortion	f = 5 MHz, V_O = 2 V_{PP}, A_V = +2 R_L = 1 kΩ to $V^+/2$		–65		dBc
t_s	Settling Time	V_O = 2 V_{PP}, ±0.1%, A_V = −1		35		ns
V_{OS}	Input Offset Voltage			1	5 **7**	mV
I_B	Input Bias Current (5)			−1.2	−2.6 **−3.25**	μA
I_{OS}	Input Offset Current			34	800 **1400**	nA
CMVR	Common Mode Input Voltage Range	CMRR ≥ 50 dB		–0.3	–0.2 **–0.1**	V
			4.0 **3.6**	4.1		
CMRR	Common Mode Rejection Ratio	V^- ≤ V_{CM} ≤ V^+ −1.5V	72	90		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 4 V_{PP}, R_L = 2 kΩ to $V^+/2$	86 **82**	95		dB
		V_O = 3.75 V_{PP}, R_L = 150Ω to $V^+/2$	74 **70**	78		
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$	4.90	4.94		V
		R_L = 150Ω to $V^+/2$	4.75	4.80		
	Output Swing Low	R_L = 2 kΩ to $V^+/2$		0.06	0.10	
		R_L = 150Ω to $V^+/2$		0.20	0.25	
I_{SC}	Output Short Circuit Current (6)	Sourcing to $V^+/2$	100 **75**	130		mA
		Sinking from $V^+/2$	100 **70**	130		
I_{OUT}	Output Current	V_O = 0.5V from either Supply		+75/−90		mA
PSRR	Power Supply Rejection Ratio	4V ≤ V^+ ≤ 6V	72	80		dB
I_S	Supply Current	No Load		3.7	5.5 **8.0**	mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.
(4) Slew rate is the average of the rising and falling slew rates
(5) Positive current corresponds to current flowing into the device.
(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 °C Short circuit test is a momentary test. Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.

5V Electrical Characteristics (continued)

Unless otherwise specified, All limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_O = V_{CM} = V^+/2 and R_L = 2 kΩ to V^+/2. **Boldface** limits apply at temperature extremes. (1)

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
R_{IN}	Common Mode Input Resistance	A_V = +1, f = 1 kHz, R_S = 1 MΩ		15		MΩ
C_{IN}	Common Mode Input Capacitance	A_V = +1, R_S = 100 kΩ		1.7		pF
R_{OUT}	Output Resistance Closed Loop	R_F = 10 kΩ, f = 1 kHz, A_V = −1		0.1		Ω
		R_F = 10 kΩ, f = 1 MHz, A_V = −1		0.4		
DG	Differential Gain	NTSC, A_V = +2 R_L = 150Ω to V^+/2		0.13		%
DP	Differential Phase	NTSC, A_V = +2 R_L = 150Ω to V^+/2		0.10		deg

16V Electrical Characteristics

Unless otherwise specified, All limits guaranteed for T_J = 25°C, V^+ = 16V, V^- = 0V, V_O = V_{CM} = $V^+/2$ and R_L = 2 kΩ to $V^+/2$. **Boldface** limits apply at temperature extremes. (1)

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
BW	−3 dB Bandwidth	A_V = +1 (R_L = 100Ω)			190		MHz
		A_V = −1 (R_L = 100Ω)			60		
$BW_{0.1\ dB}$	0.1 dB Gain Flatness	A_V = −2.7			20		MHz
LSBW	-3 dB Bandwidth	A_V = +1, V_O = 2 V_{PP} (R_L = 100Ω)			35		MHz
GBW	Gain Bandwidth Product	A_V = +1, (R_L = 100Ω)			62		MHz
SR	Slew Rate (4)	A_V = −1			170		V/µs
e_n	Input Referred Voltage Noise		f = 10 kHz		23		$nV/\sqrt{Hz}$
			f = 1 MHz		15		
i_n	Input Referred Current Noise		f = 10 kHz		1.1		$pA/\sqrt{Hz}$
			f = 1 MHz		0.7		
THD	Total Harmonic Distortion	f = 5 MHz, V_O = 2 V_{PP}, A_V = +2 R_L = 1 kΩ to $V^+/2$			–64		dBc
t_s	Settling Time	V_O = 2 V_{PP}, ±0.1%, A_V = −1			35		ns
V_{OS}	Input Offset Voltage				1	5 **7**	mV
I_B	Input Bias Current (5)				−1	−2.6 **−3.5**	µA
I_{OS}	Input Offset Current				34	800 **1800**	nA
CMVR	Common Mode Input Voltage Range	CMRR ≥ 50 dB			–0.3	−0.2 **−0.1**	V
				15.0 **14.6**	15.1		
CMRR	Common Mode Rejection Ratio	V^- ≤ V_{CM} ≤ V^+ −1.5V		72	90		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 15 V_{PP}, R_L = 2 kΩ to $V^+/2$		86 **82**	95		dB
		V_O = 14 V_{PP}, R_L = 150Ω to $V^+/2$		74 **70**	78		
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$		15.85	15.90		V
		R_L = 150Ω to $V^+/2$		15.45	15.78		
	Output Swing Low	R_L = 2 kΩ to $V^+/2$			0.10	0.15	
		R_L = 150Ω to $V^+/2$			0.21	0.55	
I_{SC}	Output Short Circuit Current (6)	Sourcing to $V^+/2$		60 **30**	95		mA
		Sinking from $V^+/2$		50 **15**	75		
I_{OUT}	Output Current	V_O = 0.5V from either Supply			±100		mA
PSRR	Power Supply Rejection Ratio	15V ≤ V^+ ≤ 17V		72	80		dB
I_S	Supply Current	No Load			4	6.5 **7.8**	mA
R_{IN}	Common Mode Input Resistance	A_V = +1, f = 1 kHz, R_S = 1 MΩ			32		MΩ

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.
(4) Slew rate is the average of the rising and falling slew rates
(5) Positive current corresponds to current flowing into the device.
(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 °C Short circuit test is a momentary test. Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.

16V Electrical Characteristics (continued)

Unless otherwise specified, All limits guaranteed for T_J = 25°C, V^+ = 16V, V^- = 0V, V_O = V_{CM} = $V^+/2$ and R_L = 2 kΩ to $V^+/2$. **Boldface** limits apply at temperature extremes. [(1)]

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
C_{IN}	Common Mode Input Capacitance	A_V = +1, R_S = 100 kΩ		1.7		pF
R_{OUT}	Output Resistance Closed Loop	R_F = 10 kΩ, f = 1 kHz, A_V = −1		0.1		Ω
		R_F = 10 kΩ, f = 1 MHz, A_V = −1		0.3		
DG	Differential Gain	NTSC, A_V = +2 R_L = 150Ω to $V^+/2$		0.12		%
DP	Differential Phase	NTSC, A_V = +2 R_L = 150Ω to $V^+/2$		0.12		deg

Connection Diagram

5-Pin SOT23

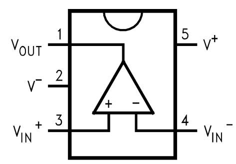
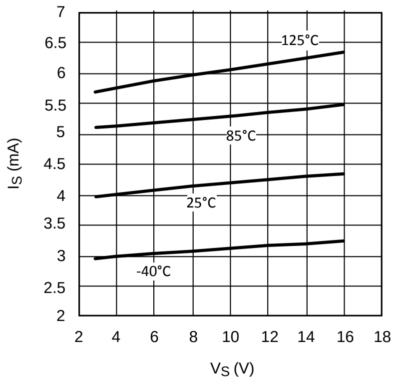


Figure 2. Top View

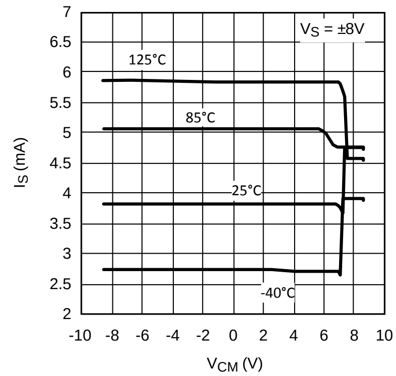
Typical Performance Characteristics

At T_J = 25°C, V^+ = 16 V, V^- = 0V, R_F = 330Ω for A_V= +2, R_F = 1 kΩ for A_V = −1. R_L tied to V^+/2. Unless otherwise specified.

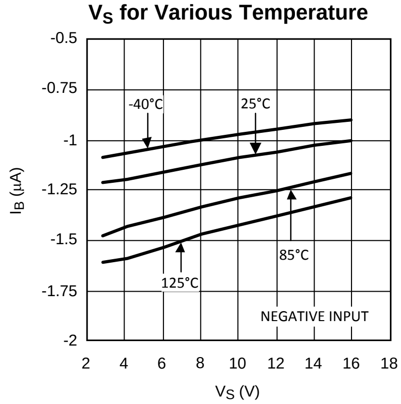
I_S vs. V_S for Various Temperature



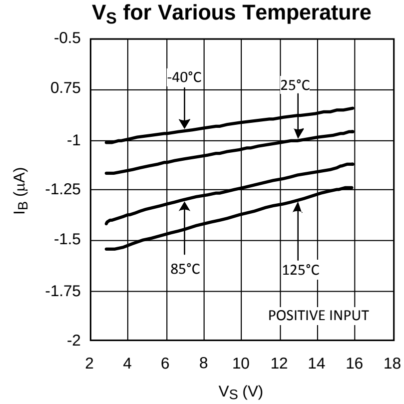
I_S vs. V_{CM} for Various Temperature



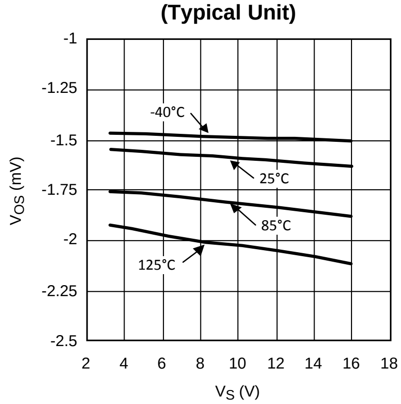
I_B vs. V_S for Various Temperature



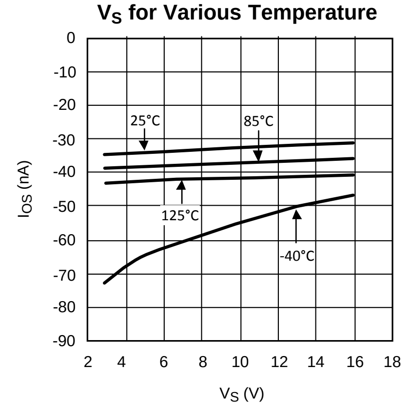
I_B vs. V_S for Various Temperature



V_{OS} vs. V_S for Various Temperature (Typical Unit)



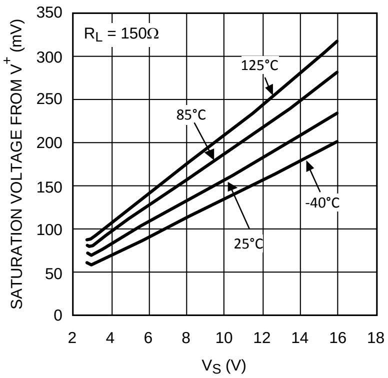
I_{OS} vs. V_S for Various Temperature



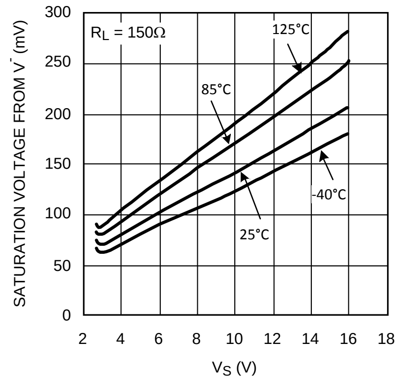
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = 16 V, V^- = 0V, R_F = 330Ω for A_V= +2, R_F = 1 kΩ for A_V = −1. R_L tied to V^+/2. Unless otherwise specified.

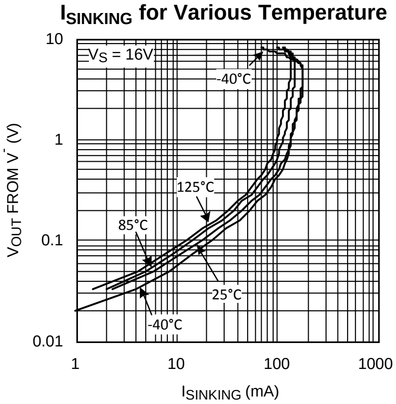
Positive Output Saturation Voltage vs. V_S for Various Temperature



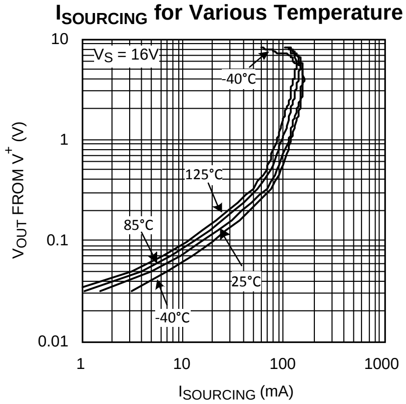
Negative Output Saturation Voltage vs. V_S for Various Temperature



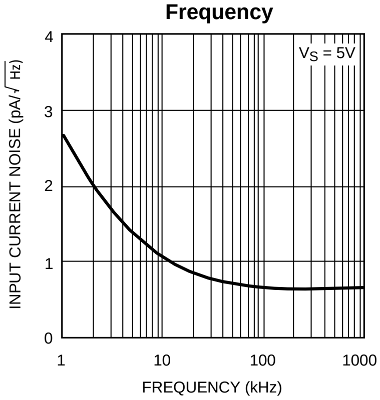
Output Sinking Saturation Voltage vs. $I_{SINKING}$ for Various Temperature



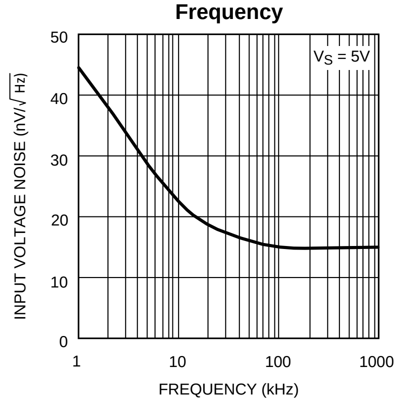
Output Sourcing Saturation Voltage vs. $I_{SOURCING}$ for Various Temperature



Input Current Noise vs. Frequency



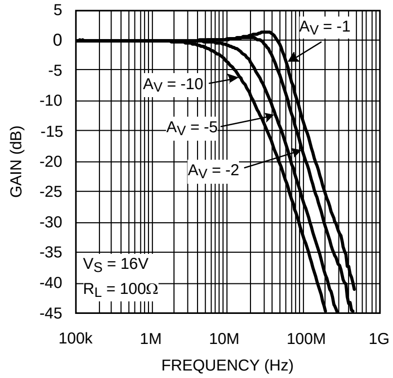
Input Voltage Noise vs. Frequency



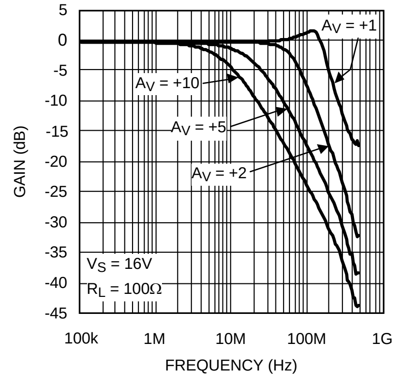
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = 16 V, V^- = 0V, R_F = 330Ω for A_V= +2, R_F = 1 kΩ for A_V = −1. R_L tied to V^+/2. Unless otherwise specified.

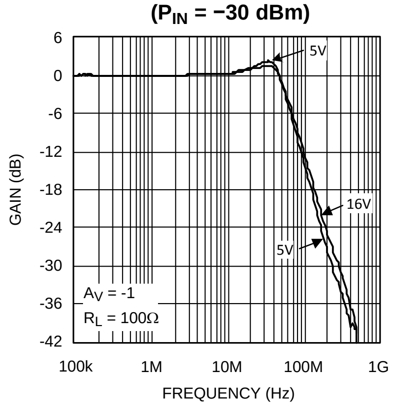
Gain vs. Frequency Normalized (P_{IN}= −30 dBm)



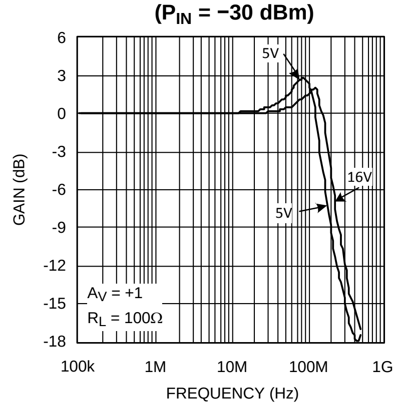
Gain vs. Frequency Normalized (P_{IN}=−30dBm)



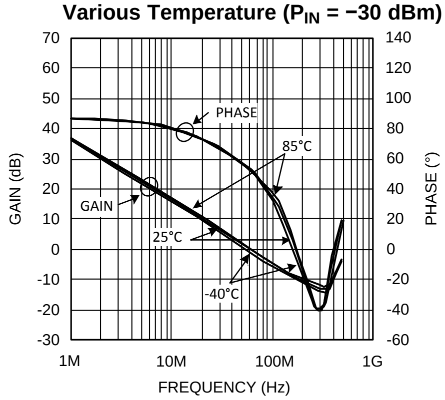
Gain vs. Frequency for Various V_S (P_{IN} = −30 dBm)



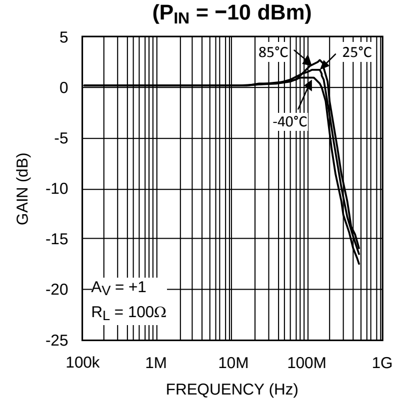
Gain vs. Frequency for Various V_S (P_{IN} = −30 dBm)



Open Loop Gain & Phase vs. Frequency for Various Temperature (P_{IN} = −30 dBm)



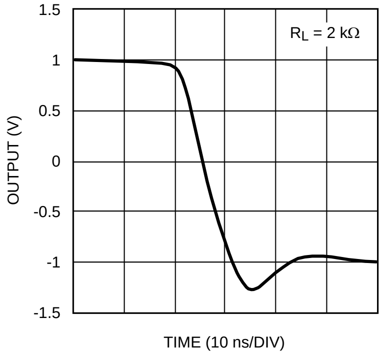
Relative Gain vs. Frequency for Various Temperature (P_{IN} = −10 dBm)



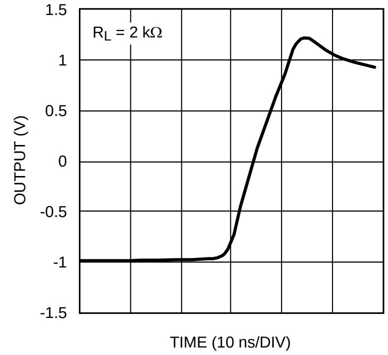
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = 16 V, V^- = 0V, R_F = 330Ω for A_V= +2, R_F = 1 kΩ for A_V = −1. R_L tied to V^+/2. Unless otherwise specified.

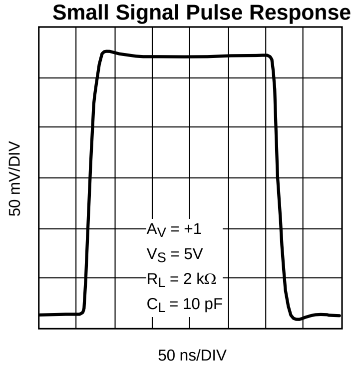
Large Signal Transition



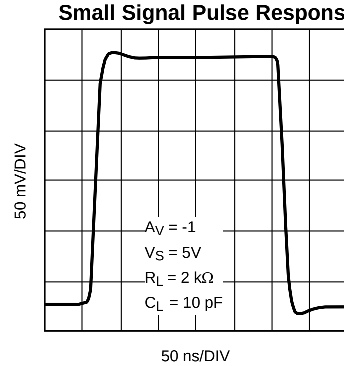
Large Signal Transition



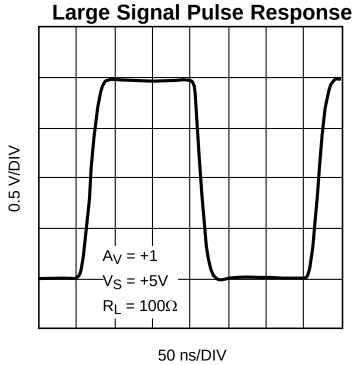
Small Signal Pulse Response



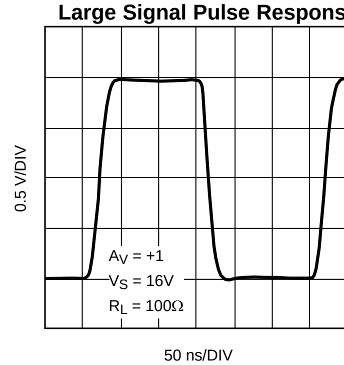
Small Signal Pulse Response



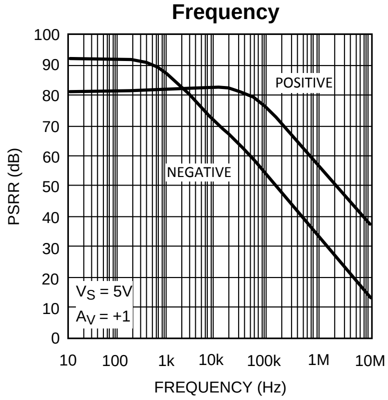
Large Signal Pulse Response



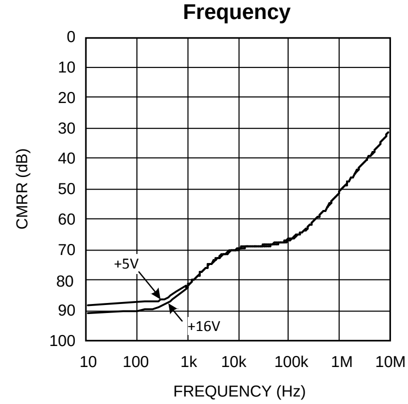
Large Signal Pulse Response



PSRR vs. Frequency



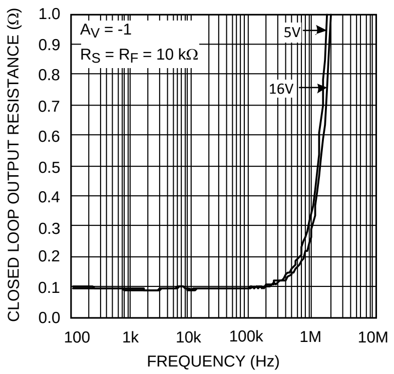
CMRR vs. Frequency



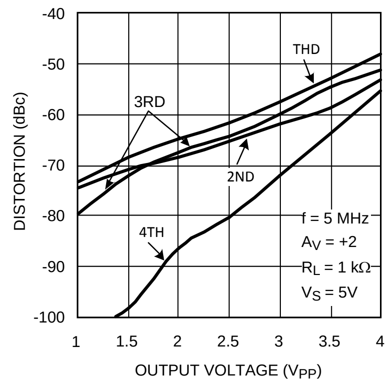
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = 16 V, V^- = 0V, R_F = 330Ω for A_V= +2, R_F = 1 kΩ for A_V = −1. R_L tied to V^+/2. Unless otherwise specified.

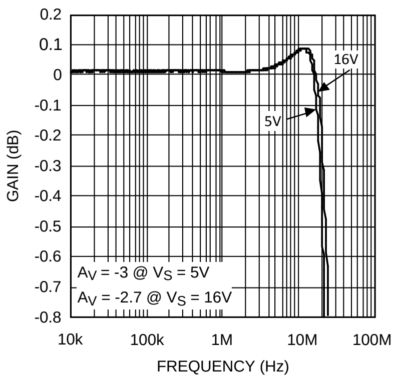
Closed Loop Output Resistance vs. Frequency



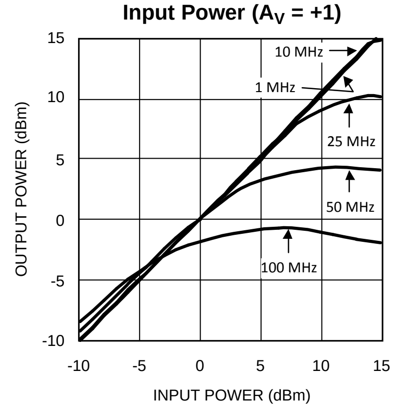
Harmonic Distortion



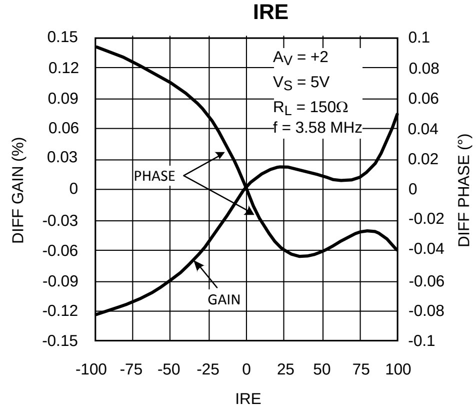
0.1 dB Gain Flatness vs. Frequency Normalized



Output Power vs. Input Power (A_V = +1)



Differential Gain/Phase vs. IRE



Application Notes

With its high output current and speed, one of the major applications for the LMH6640 is the V_{COM} driver in a TFT panel. This application is a specially taxing one because of the demands it places on the operational amplifier's output to drive a large amount of bi-directional current into a heavy capacitive load while operating under unity gain condition, which is a difficult challenge due to loop stability reasons. For a more detailed explanation of what a TFT panel is and what its amplifier requirements are, please see the Application Notes section of the LM6584 found on the web at: http://www.national.com/ds.cgi/LM/LM6584.pdf

Because of the complexity of the TFT V_{COM} waveform and the wide variation in characteristics between different TFT panels, it is difficult to decipher the results of circuit testing in an actual panel. The ability to make simplifying assumptions about the load in order to test the amplifier on the bench allows testing using standard equipment and provides familiar results which could be interpreted using standard loop analysis techniques. This is what has been done in this application note with regard to the LMH6640's performance when subjected to the conditions found in a TFT V_{COM} application.

Figure 3, shows a typical simplified V_{COM} application with the LMH6640 buffering the V_{COM} potential (which is usually around ½ of panel supply voltage) and looking into the simplified model of the load. The load represents the cumulative effect of all stray capacitances between the V_{COM} node and both row and column lines. Associated with the capacitances shown, is the distributed resistance of the lines to each individual transistor switch. The other end of this R-C ladder is driven by the column driver in an actual panel and here is driven with a low impedance MOSFET driver (labeled "High Current Driver") for the purposes of this bench test to simulate the effect that the column driver exerts on the V_{COM} load.

The modeled TFT V_{COM} load, shown in Figure 3, is based on the following simplifying assumptions in order to allow for easy bench testing and yet allow good matching results obtained in the actual application:

- The sum of all the capacitors and resistors in the R-C ladder is the total V_{COM} capacitance and resistance respectively. This total varies from panel to panel; capacitance could range from 50 nF-200 nF and the resistance could be anywhere from 20Ω-100Ω.
- The number of ladder sections has been reduced to a number (4 sections in this case) which can easily be put together in the lab and which behaves reasonably close to the actual load.

In this example, the LMH6640 was tested under the simulated conditions of total 209 nF capacitance and 54Ω as shown in Figure 3.

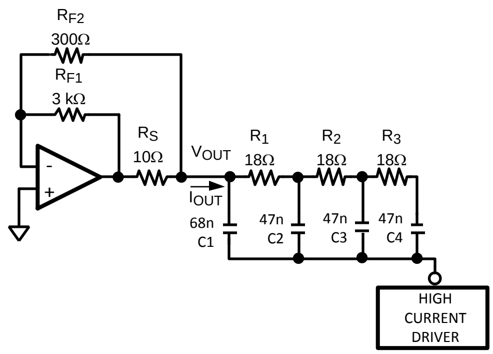


Figure 3. LMH6640 in a V_{COM} Buffer Application with Simulated TFT Load

R_S is sometimes used in the panel to provide additional isolation from the load while R_{F2} provides a more direct feedback from the V_{COM}. R_{F1}, R_{F2}, and R_S are trimmed in the actual circuit with settling time and stability trade-offs considered and evaluated. When tested under simulated load conditions of Figure 3, here are the resultant voltage and current waveforms at the LMH6640 output:

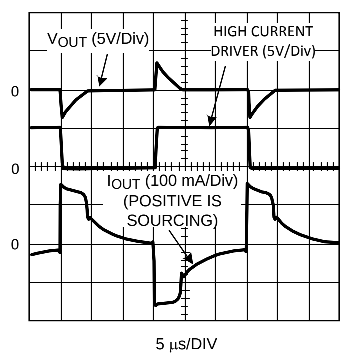


Figure 4. V_{COM} Output, High Current Drive Waveform, & LMH6640 Output Current Waveforms

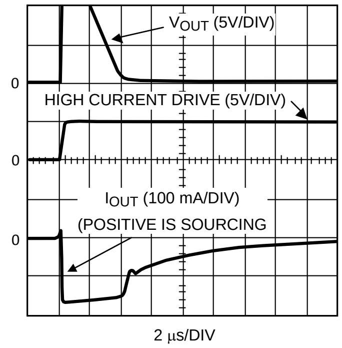


Figure 5. Expanded View of Figure 4 Waveforms showing LMH6640 Current Sinking ½ Cycle

As can be seen, the LMH6640 is capable of supplying up to 160 mA of output current and can settle the output in 4.4 μs.

The LMH6640 is a cost effective amplifier for use in the TFT V_{COM} application and is made even more attractive by its large supply voltage range and high output current. The combination of all these features is not readily available in the market, especially in the space saving SOT23-5 package. All this performance is achieved at the low power consumption of 65 mW which is of utmost importance in today's battery driven TFT panels.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6640MF	ACTIVE	SOT-23	DBV	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	AH1A	Samples
LMH6640MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AH1A	Samples
LMH6640MFX	ACTIVE	SOT-23	DBV	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	AH1A	Samples
LMH6640MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AH1A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

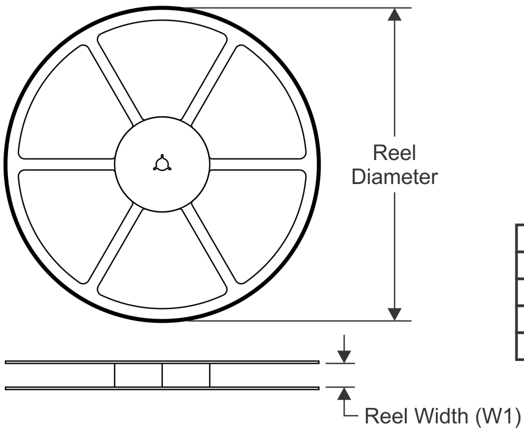
(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

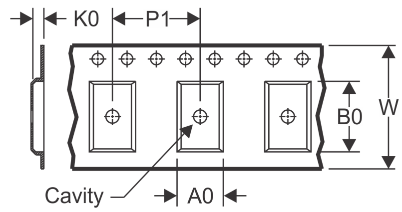
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

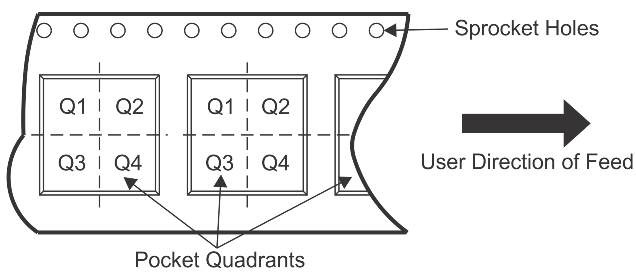


TAPE DIMENSIONS



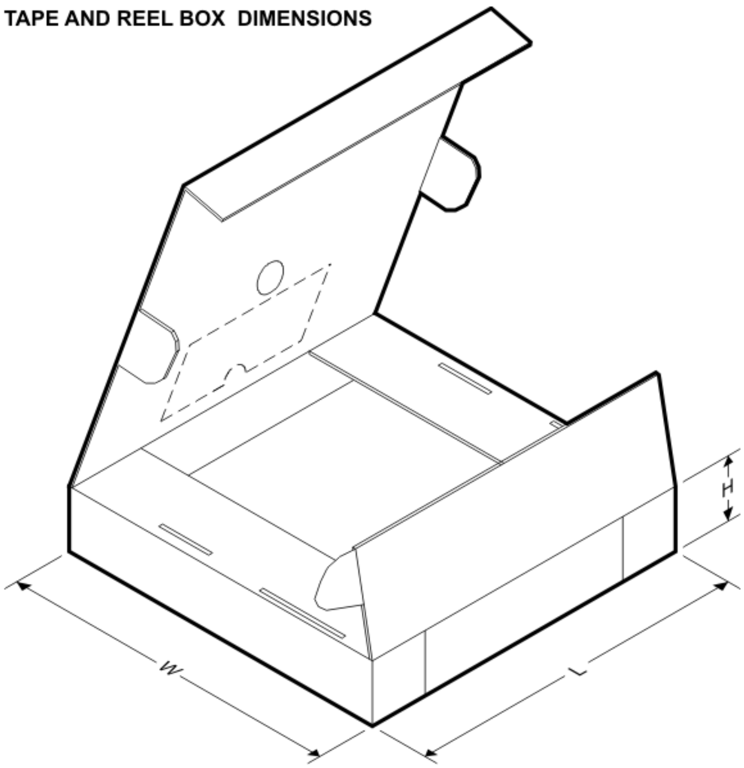
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

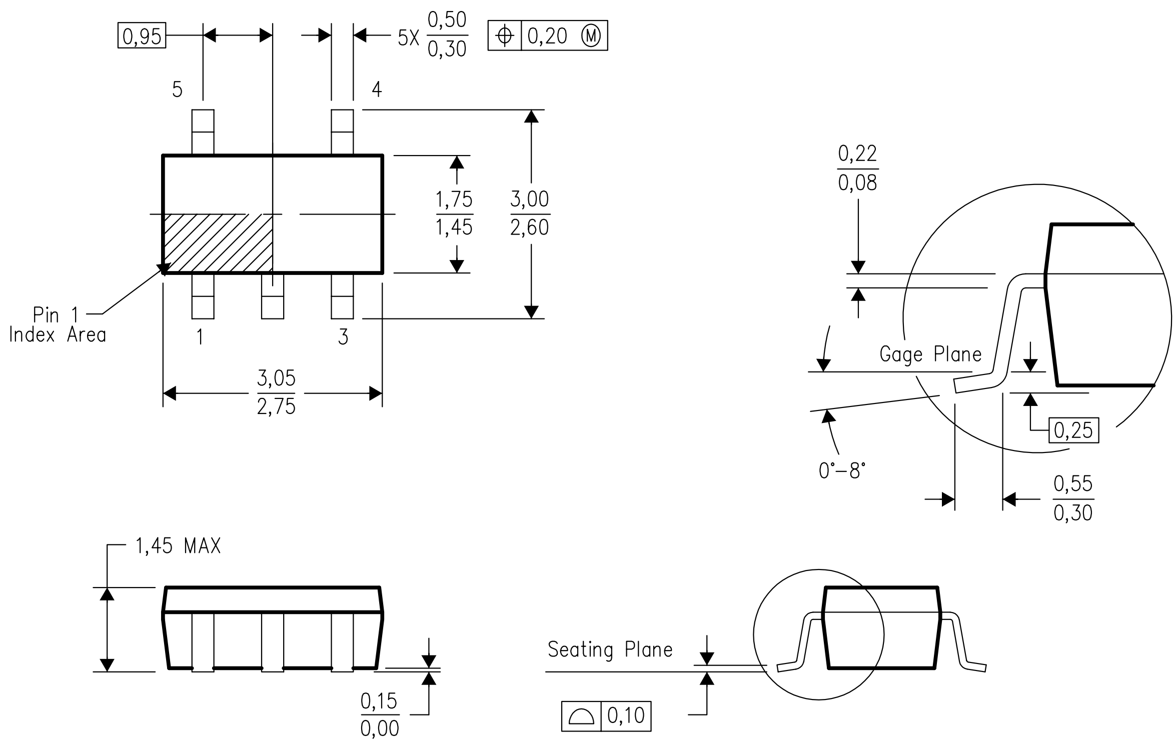
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6640MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6640MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6640MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6640MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6640MF	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMH6640MF/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMH6640MFX	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMH6640MFX/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0

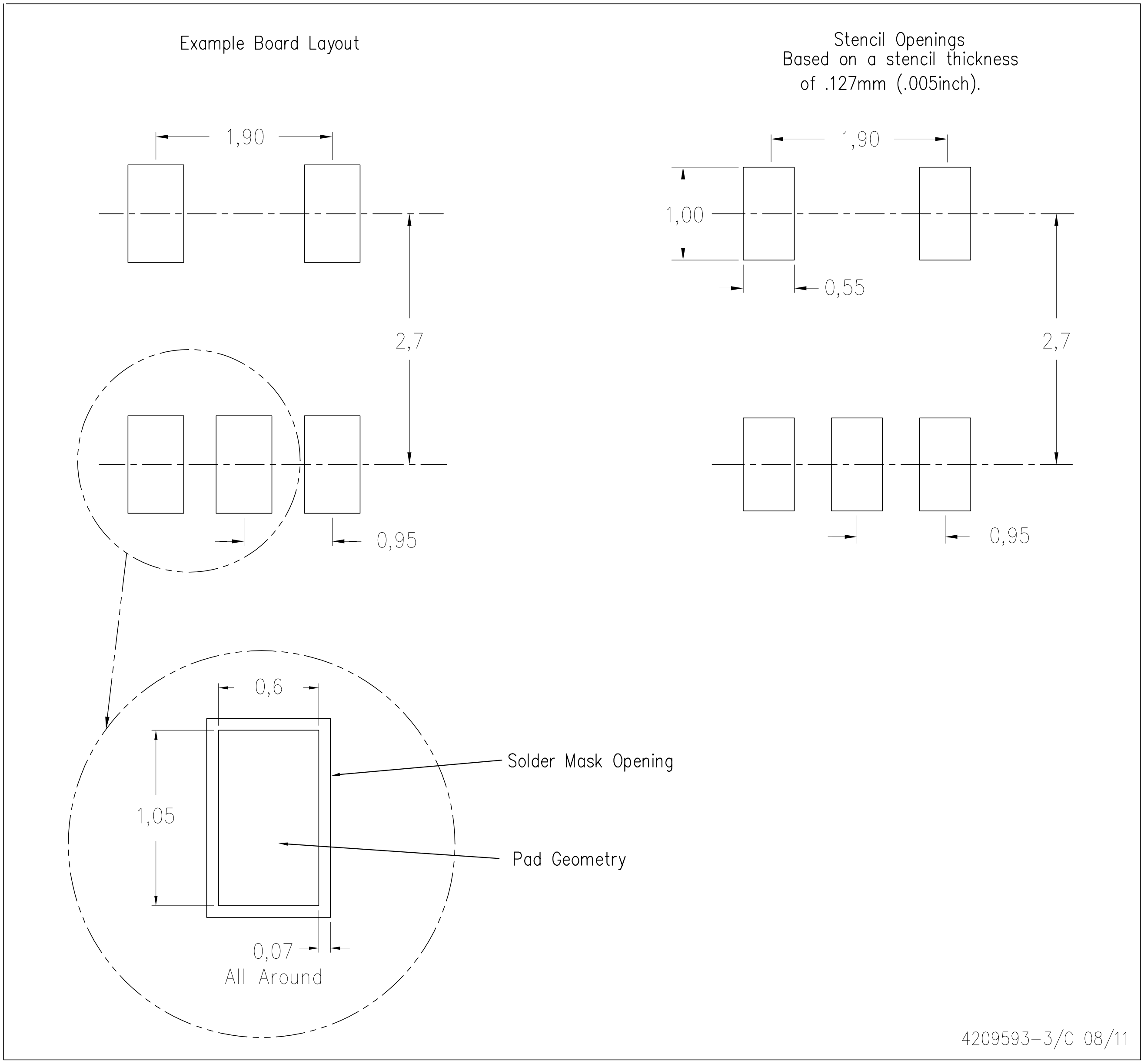
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265