LMK03806 Ultra Low Jitter Clock Generator with 14 Programmable Outputs

Check for Samples: LMK03806

FEATURES

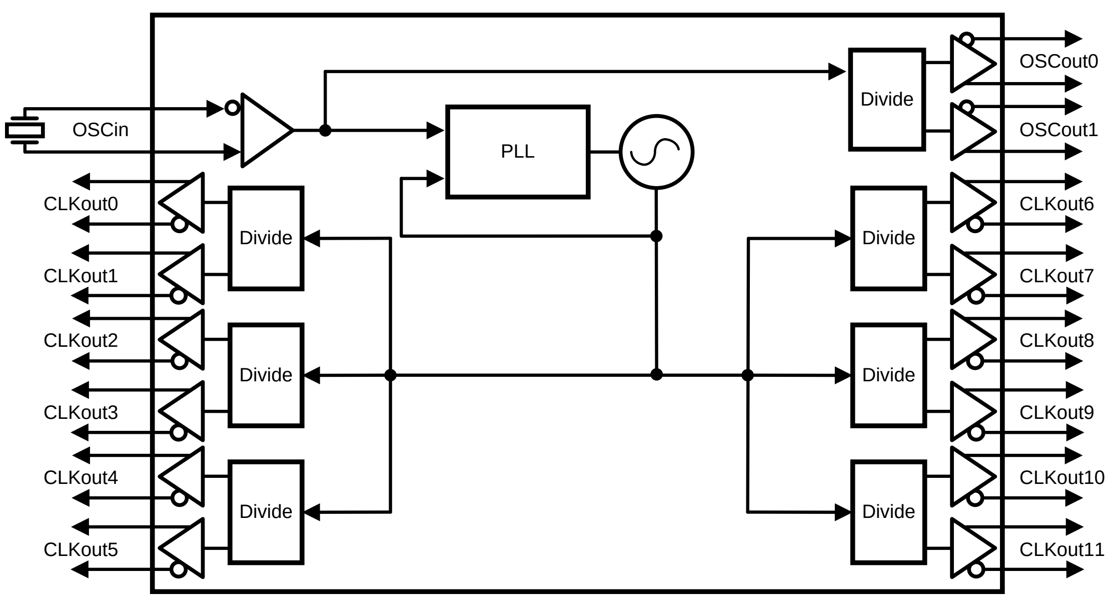
- **High Performance, Ultra Low Jitter Clock Generator**
- **Low Jitter**
  - **< 50 fs Jitter (1.875 MHz - 20 MHz) at 312.5 MHz Output Frequency**
  - **< 150 fs Jitter (12 kHz - 20 MHz) at 312.5 MHz Output Frequency**
- **Generates Multiple Clocks from a Low Cost Crystal or External Clock.**
- **14 Outputs with Programmable Output Format (LVDS, LVPECL, CMOS)**
- **Up to 8 Unique Output Frequencies.**
- **Industrial Temperature Range: -40 to 85 °C**
- **Tunable VCO Frequency from 2.37 - 2.6 GHz**
- **Programmable Dividers to Generate Multiple Clocks from a Low Cost Crystal.**
- **3.15 V to 3.45 V Operation**

TARGET APPLICATIONS

- **Ultra High Speed Serial Interfaces in SONET/SDH**
- **Multi-Gigabit Ethernet & Fiber Channel Line Cards**
- **Base Band Units (BBUs) for RAN applications**
- **GPON OLT/ONU , High Speed Serial Interface such as PCIe, XAUI, SATA, SAS**
- **Clocking ADC and DACs**
- **Clocking DSP, Microprocessors and FPGAs**

DESCRIPTION

The LMK03806 is a high performance, ultra low-jitter, multi-rate clock generator capable of synthesizing 8 different frequencies on 14 outputs at frequencies of up to 2.6 GHz. Each output clock is programmable in LVDS, LVPECL or LVCMOS format. The LMK03806 integrates a high performance integer-N PLL, low noise VCO, and programmable output dividers to generate multiple reference clocks for SONET, Ethernet, Fiber Channel, XAUI, Backplane, PCIe, SATA and Network Processors from a low cost crystal.



Common Frequency Plans

Standard/Application	Output Frequencies (MHz)	VCO Frequency	Recommended Crystal Value
Infiniband	100, 200	2400 MHz	20 MHz
SATA	75, 150, 300, 600		
SAS	37.5, 75, 120, 150		
Fast Ethernet	25	2500 MHz	
1 GbE	125		
10 GbE	156.25, 312.5, 625		
XAUI	78.125, 156.25, 312.5		
Backplane	227.27...		
2G/4G/16G Fiber Channel	106.25, 212.5	2550 MHz	
10G Fiber Channel	159.375		
40/100 GbE	644.53125, 322.265625, 161.1328125	2578.125 MHz	12.5 MHz
SONET	19.44, 38.88, 77.76, 155.52, 311.04, 622.08	2488.32 MHz	19.44 MHz
A/D Clocking	30.72, 61.44, 122.88, 153.6, 245.76, 491.52, 983.04	2457.6 MHz	19.2 MHz or 12.288 MHz

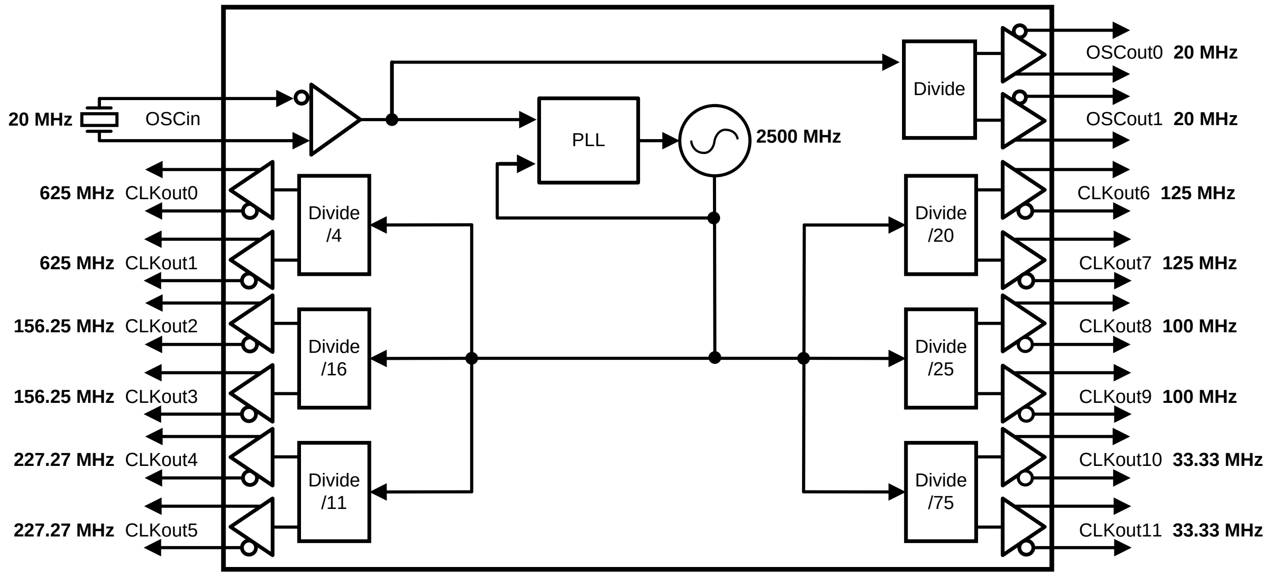
Achievable Frequencies

By using the tunable range of the VCO followed by a programmable divider, the LMK03806 can achieve any of the frequencies in the table below

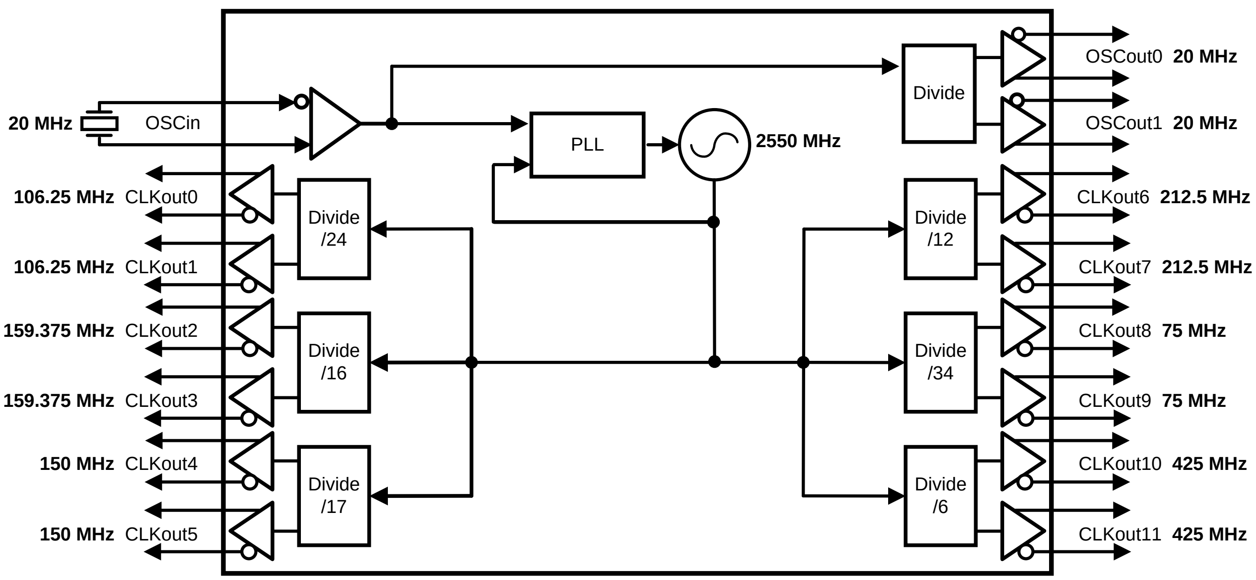
Output Divider Value	Achieved Frequency (MHz)
1	2370 - 2600
2	1185 - 1300
3	790 - 866.7
4	592.5 - 650
5	474 - 520
6	395.7 - 433
7	338.6 - 371.4
8	296.25 - 325
9	263.3 - 288.9
10	237 - 260
11 to 1045	Any frequency in the range of 2.27 - 236.36

Functional Block Diagrams

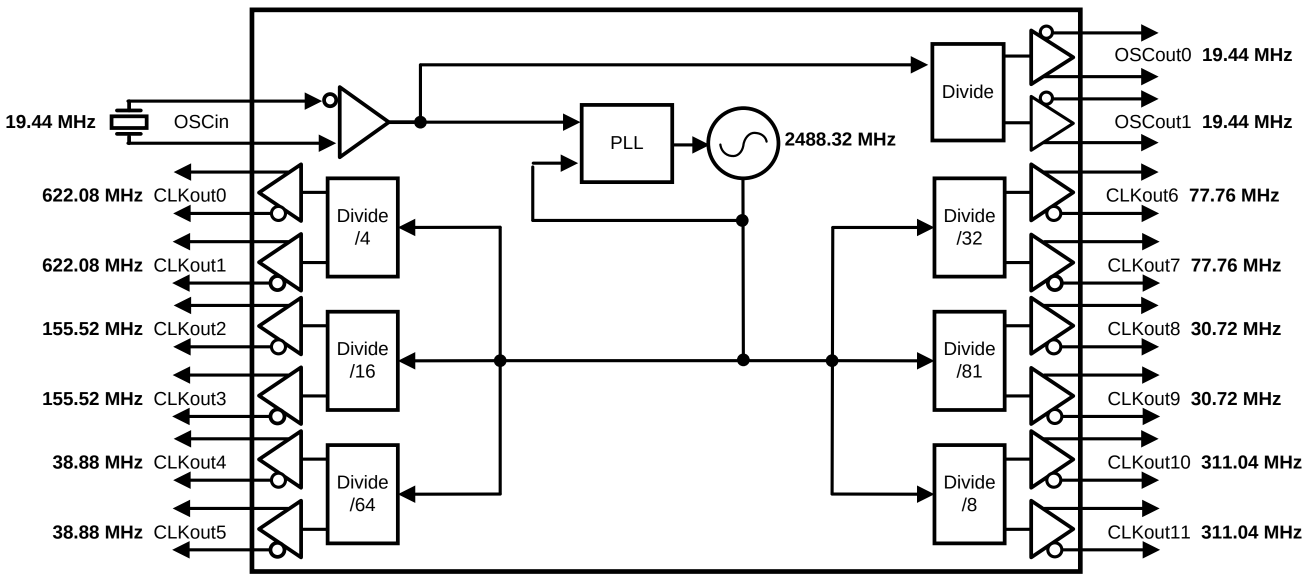
10 Gigabit Ethernet Reference Clocks



Fiber Channel Reference Clocks



SONET/SDH Reference Clocks



Detailed LMK03806 Block Diagram

Figure 1 illustrates the complete LMK03806 block diagram.

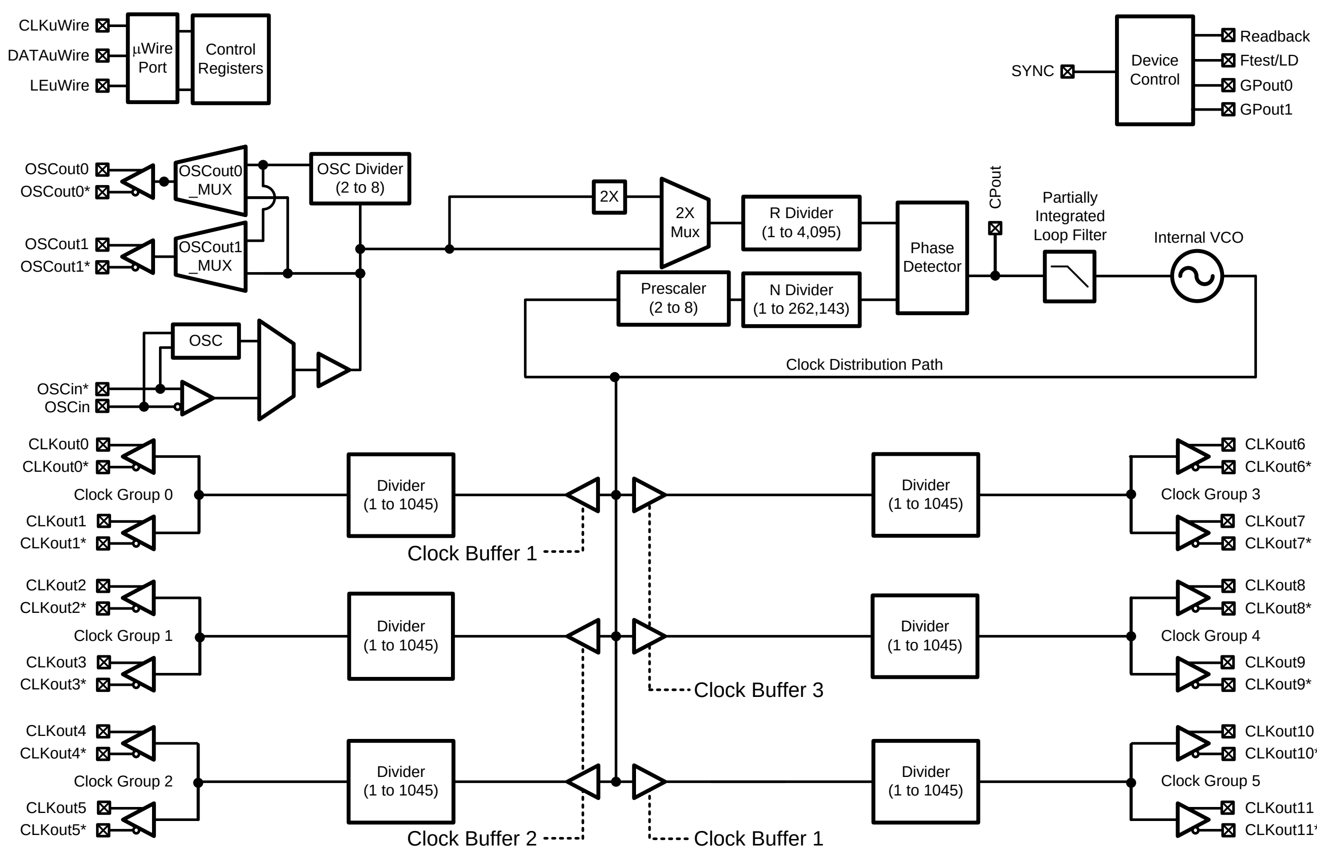


Figure 1.

Connection Diagram

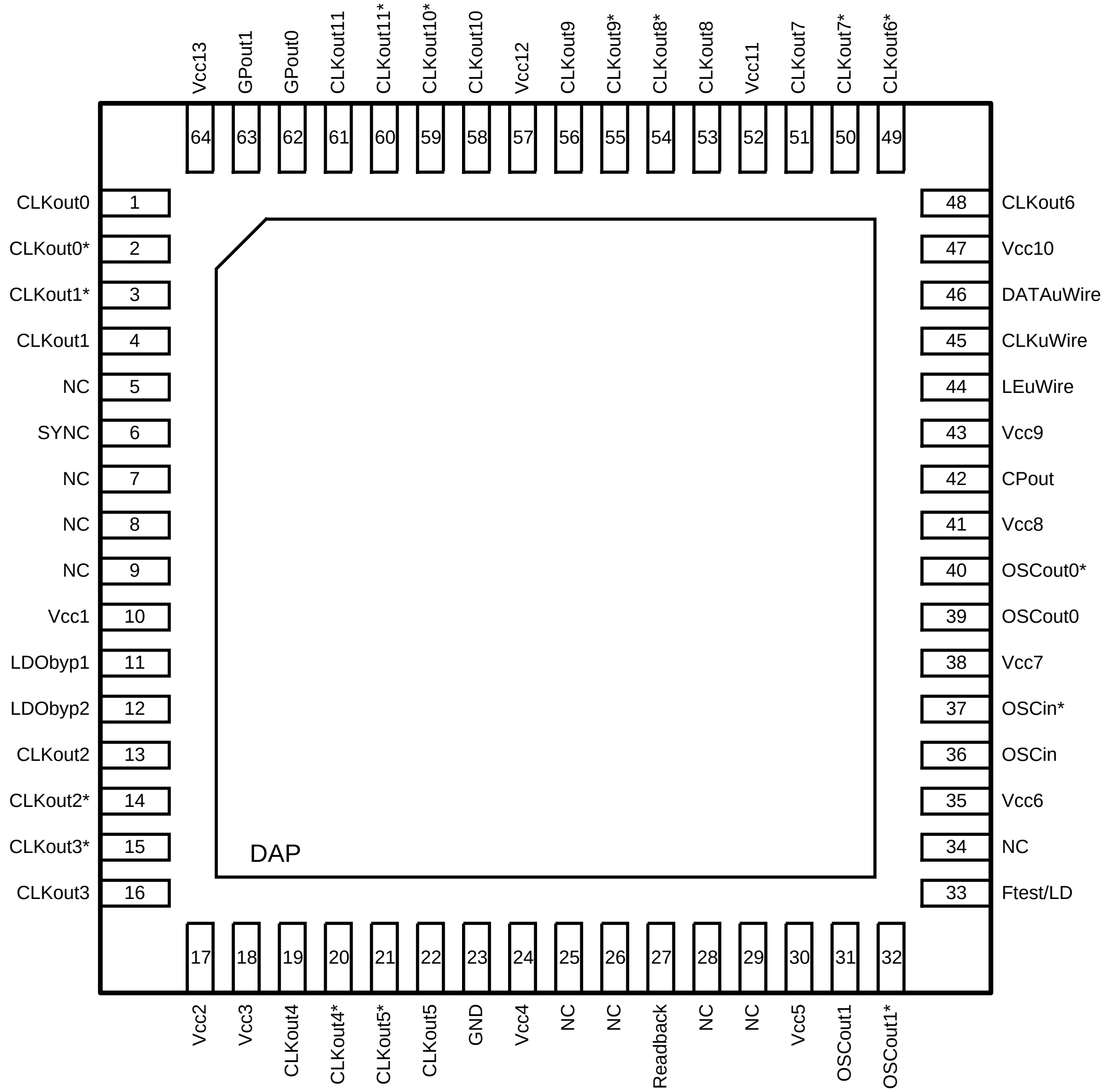


Figure 2. WQFN 64-Pin Package
Top Down View

PIN DESCRIPTIONS

Pin Number	Name(s)	I/O	Type	Description
1, 2	CLKout0, CLKout0*	O	Programmable	Clock output 0 (clock group 0).
3, 4	CLKout1*, CLKout1	O	Programmable	Clock output 1 (clock group 0).
5, 7, 8, 9, 25, 26, 28,29, 34	NC	-	Do Not Connect	These pins must be left floating. Do NOT ground.
6	SYNC	I	CMOS	Clock synchronization input.
10	Vcc1	-	PWR	Power supply for VCO LDO.
11	LDObyp1	-	ANLG	LDO Bypass, bypassed to ground with 10 µF capacitor.
12	LDObyp2	-	ANLG	LDO Bypass, bypassed to ground with a 0.1 µF capacitor.
13, 14	CLKout2, CLKout2*	O	Programmable	Clock output 2 (clock group 1).
15, 16	CLKout3*, CLKout3	O	Programmable	Clock output 3 (clock group 1).

PIN DESCRIPTIONS (continued)

Pin Number	Name(s)	I/O	Type	Description
17	Vcc2	-	PWR	Power supply for clock group 1: CLKout2 and CLKout3.
18	Vcc3	-	PWR	Power supply for clock group 2: CLKout4 and CLKout5.
19, 20	CLKout4, CLKout4*	O	Programmable	Clock output 4 (clock group 2).
21, 22	CLKout5*, CLKout5	O	Programmable	Clock output 5 (clock group 2).
23	GND	-	PWR	Ground
24	Vcc4	-	PWR	Power supply for digital.
27	Readback	O	CMOS	Pin that can be used to readback register information.
30	Vcc5	-	PWR	Power supply for clock inputs.
31, 32	OSCout1, OSCout1*	O	LVPECL	Buffered output 1 of OSCin port.
33	Ftest/LD	O	Programmable	Multiplexed Lock Detect and Test output pin.
35	Vcc6	-	PWR	Power supply. No bypassing required on this pin.
36, 37	OSCin, OSCin*	I	ANLG	Reference input to PLL. Reference input may be: A Crystal for use with the internal crystal oscillator circuit. A XO, TCXO, or other external clock. Must be AC Coupled.
38	Vcc7	-	PWR	Power supply for OSCin port.
39, 40	OSCout0, OSCout0*	O	Programmable	Buffered output 0 of OSCin port.
41	Vcc8	-	PWR	Power supply for PLL charge pump.
42	CPout	O	ANLG	Charge pump output.
43	Vcc9	-	PWR	Power supply for PLL.
44	LEuWire	I	CMOS	MICROWIRE Latch Enable Input.
45	CLKuWire	I	CMOS	MICROWIRE Clock Input.
46	DATAuWire	I	CMOS	MICROWIRE Data Input.
47	Vcc10	-	PWR	Power supply for clock group 3: CLKout6 and CLKout7.
48, 49	CLKout6, CLKout6*	O	Programmable	Clock output 6 (clock group 3).
50, 51	CLKout7*, CLKout7	O	Programmable	Clock output 7 (clock group 3).
52	Vcc11	-	PWR	Power supply for clock group 4: CLKout8 and CLKout9.
53, 54	CLKout8, CLKout8*	O	Programmable	Clock output 8 (clock group 4).
55, 56	CLKout9*, CLKout9	O	Programmable	Clock output 9 (clock group 4).
57	Vcc12	-	PWR	Power supply for clock group 5: CLKout10 and CLKout11.
58, 59	CLKout10, CLKout10*	O	Programmable	Clock output 10 (clock group 5).
60, 61	CLKout11*, CLKout11	O	Programmable	Clock output 11 (clock group 5).
62, 63	GPout0, GPout1	O	CMOS	These pins can be programmed for general purpose output.
64	Vcc13	-	PWR	Power supply for clock group 0: CLKout0 and CLKout1.
DAP	DAP	-	GND	DIE ATTACH PAD, connect to GND.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)(4)

Parameter	Symbol	Ratings	Units
Supply Voltage (5)	V_{CC}	-0.3 to 3.6	V
Input Voltage	V_{IN}	-0.3 to (V_{CC} + 0.3)	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (solder 4 seconds)	T_L	+260	°C
Junction Temperature	T_J	150	°C
Differential Input Current (OSCin/OSCin*)	I_{IN}	± 5	mA
Moisture Sensitivity Level	MSL	3	

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only to the test conditions listed.
(2) This device is a high performance RF integrated circuit with an ESD rating up to 2 kV Human Body Model, up to 150 V Machine Model, and up to 750 V Charged Device Model and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.
(3) Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is only implied at these or any other conditions in excess of those given in the operation sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.
(4) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(5) Never to exceed 3.6 V.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Ambient Temperature	T_A	V_{CC} = 3.3 V	-40	25	85	°C
Junction Temperature	T_J	V_{CC} = 3.3 V			125	°C
Supply Voltage	V_{CC}		3.15	3.3	3.45	V

Electrical Characteristics(1)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C, Junction Temperature T_J ≤ 125 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Current Consumption						
I_{CC_PD}	Power Down Supply Current	No DC path to ground on OSCout1/1* (2)		1		mA
I_{CC_CLKS}	Supply Current with all clocks enabled (3)	CLKoutX_Y_DIV = 16, CLKoutX_TYPE = 1 (LVDS), PLL locked		445		mA
External Clock (OSCin) Specifications						
f_{OSCin}	PLL Reference Input (4)		1		500	MHz

(1) In order to meet the jitter performance listed in the subsequent sections of this data sheet, the minimum recommended slew rate for all input clocks is 0.5 V/ns. This is especially true for single-ended clocks. Phase noise performance will begin to degrade as the clock input slew rate is reduced. However, the device will function at slew rates down to the minimum listed. When compared to single-ended clocks, differential clocks (LVDS, LVPECL) will be less susceptible to degradation in phase noise performance at lower slew rates due to their common mode noise rejection. However, it is also recommended to use the highest possible slew rate for differential clocks to achieve optimal phase noise performance at the device outputs.
(2) If emitter resistors are placed on the OSCout1/1* pins, there will be a DC current to ground which will cause powerdown Icc to increase.
(3) Load conditions for output clocks: LVDS: 100 Ω differential. See applications section Current Consumption / Power Dissipation Calculations for Icc for specific part configuration and how to calculate Icc for a specific design.
(4) F_{OSCin} maximum frequency guaranteed by characterization. Production tested at 200 MHz.

Electrical Characteristics[1] (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C, Junction Temperature T_J ≤ 125 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$SLEW_{OSCin}$	PLL Reference Clock minimum slew rate on OSCin (5)	20% to 80%	0.15	0.5		V/ns
V_{OSCin}	Input Voltage for OSCin or OSCin* (5)	AC coupled; Single-ended (Unused pin AC coupled to GND)	0.2		2.4	Vpp
$V_{ID}OSCin$	Differential voltage swing Figure 4	AC coupled	0.2		1.55	|V|
$V_{SS}OSCin$			0.4		3.1	Vpp
$V_{OSCin\text{-}offset}$	DC offset voltage between OSCin/OSCin* OSCinX* - OSCinX	Each pin AC coupled		20		mV
$f_{doubler\_max}$	Doubler input frequency (5)	EN_PLL_REF_2X = 1; OSCin Duty Cycle 40% to 60%			155	MHz
Crystal Oscillator Mode Specifications						
f_{XTAL}	Crystal Frequency Range (5)	R_{ESR} ≤ 40 Ω C_L ≤ 20 pF	16		20.5	MHz
		R_{ESR} ≤ 80 Ω C_L ≤ 22 pF	6		16	MHz
P_{XTAL}	Crystal Power Dissipation	Vectron VXB1 crystal, 20.48 MHz, R_{ESR} ≤ 40 Ω C_L ≤ 20 pF		120		µW
C_{IN}	Input Capacitance of the OSCin port	-40 to +85 °C		6		pF
RMS Jitter Performance						
XO Mode (6) (7) (8)	Integration Bandwidth 10 kHz to 1 MHz	156.25 MHz, LVDS/LVPECL		81		fs
		312.5 MHz, LVDS/LVPECL		85		
	Integration Bandwidth 12 kHz to 20 MHz	100 MHz, LVDS		139		
		100 MHz, LVPECL		117		
		106.25 MHz, LVDS		145		
		106.25 MHz, LVPECL		126		
		156.25 MHz, LVDS		111		
		156.25 MHz, LVPECL		100		
		312.5 MHz, LVDS		108		
		312.5 MHz, LVPECL		95		
		622.08 MHz, LVDS/LVPECL		141		
	Integration Bandwidth 637 kHz to 10 MHz	106.25 MHz, LVDS		78		
		106.25 MHz, LVPECL		60		
	Integration Bandwidth 1.875 MHz to 20 MHz	156.25 MHz, LVDS		70		
		156.25 MHz, LVPECL		57		
		312.5 MHz, LVDS		57		
		312.5 MHz, LVPECL		43		

(5) Guaranteed by characterization.
(6) Jitter and phase noise data for 100 MHz, 156.25, and 312.5 MHz collected using a Wenzel crystal oscillator, part number 501–04623G. Loop filter values are C1 = 39 pF, C2 = 3.3 nF, R2 = 680 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler disabled. VCO frequency = 2500 MHz using a phase detector frequency = 100 MHz the loop bandwidth = 80 kHz and phase margin = 60°.
(7) Jitter and phase noise data for 106.25 MHz collected using a Wenzel crystal oscillator, part number 501–04623G. Loop filter values are C1 = 39pF, C2 = 3.3 nF, R2 = 820Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler disabled. VCO frequency = 2550 MHz using a phase detector frequency = 10 MHz the loop bandwidth = 80 kHz and phase margin = 60°.
(8) Jitter and phase noise data for 622.08 MHz collected using a Crystec oscillator, part number CVHD-950. Loop filter values are C1 = 39 pF, C2 = 3.3 nF, R2 = 680 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler enabled. VCO frequency = 2488.32 MHz using a phase detector frequency = 30.72 MHz the loop bandwidth = 80 kHz and phase margin = 60°.

Electrical Characteristics(1) (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C, Junction Temperature T_J ≤ 125 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Crystal Mode Jitter (9) (10) (11)	Integration Bandwidth 10 kHz to 1 MHz	156.25 MHz, LVDS/LVPECL		190		fs
		312.5 MHz, LVDS/LVPECL		200		
	Integration Bandwidth 12 kHz to 20 MHz	100 MHz, LVDS		235		
		100 MHz, LVPECL		210		
		106.25 MHz, LVDS		280		
		106.25 MHz, LVPECL		250		
		156.25 MHz, LVDS		200		
		156.25 MHz, LVPECL		195		
		312.5 MHz, LVDS		220		
		312.5 MHz, LVPECL		190		
		622.08 MHz, LVDS/LVPECL		255		
	Integration Bandwidth 637 kHz to 10 MHz	106.25 MHz, LVDS		90		
		106.25 MHz, LVPECL		65		
	Integration Bandwidth 1.875 MHz to 20 MHz	156.25 MHz, LVDS		75		
		156.25 MHz, LVPECL		65		
		312.5 MHz, LVDS		60		
		312.5 MHz, LVPECL		45		

(9) Jitter and phase noise data for 100 MHz, 156.25, and 312.5 MHz collected using an ECS crystal, part number ECS-200-20-30B-DU. Loop filter values are C1 = 220 pF, C2 = 18 nF, R2 = 820 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler disabled. VCO frequency = 2500 MHz using a phase detector frequency = 20 MHz the loop bandwidth = 62 kHz and phase margin = 76°.

(10) Jitter and phase noise data for 106.25 MHz collected using an ECS crystal, part number ECS-200-20-30B-DU. Loop filter values are C1 = 220 pF, C2 = 18 nF, R2 = 820 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler disabled. VCO frequency = 2550 MHz using a phase detector frequency = 10 MHz the loop bandwidth = 32 kHz and phase margin = 69°.

(11) Jitter and phase noise data for 622.08 MHz collected using a Vectron crystal, part number VXB1-1137-15M360. Loop filter values are C1 = 100 pF, C2 = 120 nF, R2 = 470 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler enabled. VCO frequency = 2488.32 MHz using a phase detector frequency = 30.72 MHz the loop bandwidth = 54 kHz and phase margin = 86°.

Electrical Characteristics[1] (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C, Junction Temperature T_J ≤ 125 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Phase Noise Performance						
XO Mode Phase Noise	100 MHz (LVDS/LVPECL) (12)	10 kHz		-142		dBc/Hz
		100 kHz		-143		
		1 MHz		-157		
		10 MHz (LVDS)		-159		
		20 MHz (LVDS)		-160		
		10 MHz (LVPECL)		-160		
		20 MHz (LVPECL)		-161		
	106.25 MHz (LVDS/LVPECL) (13)	10 kHz		-141		
		100 kHz		-140		
		1 MHz		-156		
		10 MHz (LVDS)		-159		
		20 MHz (LVDS)		-160		
		10 MHz (LVPECL)		-162		
		20 MHz (LVPECL)		-163		
	156.25 MHz (LVDS/LVPECL) (12)	10 kHz		-139		
		100 kHz		-140		
		1 MHz		-153		
		10 MHz (LVDS)		-159		
		20 MHz (LVDS)		-159		
		10 MHz (LVPECL)		-160		
		20 MHz (LVPECL)		-160		
	312.5 MHz (LVDS/LVPECL) (12)	10 kHz		-132		
		100 kHz		-133		
		1 MHz		-148		
		10 MHz (LVDS)		-154		
		20 MHz (LVDS)		-155		
		10 MHz (LVPECL)		-157		
		20 MHz (LVPECL)		-158		
	622.08 MHz (LVDS/LVPECL) (14)	10 kHz		-123		
		100 kHz		-121		
		1 MHz		-143		
		10 MHz (LVDS)		-154		
		20 MHz (LVDS)		-154		
		10 MHz (LVPECL)		-157		
		20 MHz (LVPECL)		-158		

(12) Jitter and phase noise data for 100 MHz, 156.25, and 312.5 MHz collected using a Wenzel crystal oscillator, part number 501–04623G. Loop filter values are C1 = 39 pF, C2 = 3.3 nF, R2 = 680 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler disabled. VCO frequency = 2500 MHz using a phase detector frequency = 100 MHz the loop bandwidth = 80 kHz and phase margin = 60°.

(13) Jitter and phase noise data for 106.25 MHz collected using a Wenzel crystal oscillator, part number 501–04623G. Loop filter values are C1 = 39pF, C2 = 3.3 nF, R2 = 820Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler disabled. VCO frequency = 2550 MHz using a phase detector frequency = 10 MHz the loop bandwidth = 80 kHz and phase margin = 60°.

(14) Jitter and phase noise data for 622.08 MHz collected using a Crystec oscillator, part number CVHD-950. Loop filter values are C1 = 39 pF, C2 = 3.3 nF, R2 = 680 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler enabled. VCO frequency = 2488.32 MHz using a phase detector frequency = 30.72 MHz the loop bandwidth = 80 kHz and phase margin = 60°.

Electrical Characteristics[1] (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C, Junction Temperature T_J ≤ 125 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Crystal Mode Phase Noise	100 MHz (LVDS/LVPECL) (15)	10 kHz		-129		dBc/Hz
		100 kHz		-137		
		1 MHz		-156		
		10 MHz (LVDS)		-158		
		20 MHz (LVDS)		-159		
		10 MHz (LVPECL)		-160		
		20 MHz (LVPECL)		-161		
	106.25 MHz (LVDS/LVPECL) (16)	10 kHz		-124		
		100 kHz		-137		
		1 MHz		-156		
		10 MHz (LVDS)		-158		
		20 MHz (LVDS)		-159		
		10 MHz (LVPECL)		-160		
		20 MHz (LVPECL)		-161		
	156.25 MHz (LVDS/LVPECL) (15)	10 kHz		-125		
		100 kHz		-132		
		1 MHz		-153		
		10 MHz (LVDS)		-158		
		20 MHz (LVDS)		-159		
		10 MHz (LVPECL)		-160		
		20 MHz (LVPECL)		-160		
	312.5 MHz (LVDS/LVPECL) (15)	10 kHz		-119		
		100 kHz		-126		
		1 MHz		-147		
		10 MHz (LVDS)		-153		
		20 MHz (LVDS)		-154		
		10 MHz (LVPECL)		-156		
		20 MHz (LVPECL)		-157		
	622.08 MHz (LVDS/LVPECL) (17)	10 kHz		-110		
		100 kHz		-120		
		1 MHz		-140		
		10 MHz (LVDS)		-153		
		20 MHz (LVDS)		-153		
		10 MHz (LVPECL)		-154		
		20 MHz (LVPECL)		-154		

(15) Jitter and phase noise data for 100 MHz, 156.25, and 312.5 MHz collected using an ECS crystal, part number ECS-200-20-30B-DU. Loop filter values are C1 = 220 pF, C2 = 18 nF, R2 = 820 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler disabled. VCO frequency = 2500 MHz using a phase detector frequency = 20 MHz the loop bandwidth = 62 kHz and phase margin = 76°.
(16) Jitter and phase noise data for 106.25 MHz collected using an ECS crystal, part number ECS-200-20-30B-DU. Loop filter values are C1 = 220 pF, C2 = 18 nF, R2 = 820 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler disabled. VCO frequency = 2550 MHz using a phase detector frequency = 10 MHz the loop bandwidth = 32 kHz and phase margin = 69°.
(17) Jitter and phase noise data for 622.08 MHz collected using a Vectron crystal, part number VXB1-1137-15M360. Loop filter values are C1 = 100 pF, C2 = 120 nF, R2 = 470 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω. Charge pump current = 3.2 mA. LVPECL emitter resistors, R_e = 240 Ω. Reference doubler enabled. VCO frequency = 2488.32 MHz using a phase detector frequency = 30.72 MHz the loop bandwidth = 54 kHz and phase margin = 86°.

Electrical Characteristics[1] (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C, Junction Temperature T_J ≤ 125 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PLL Phase Detector and Charge Pump Specifications						
f_{PD}	Phase Detector Frequency				155	MHz
I_{CPout}SOURCE	PLL Charge Pump Source Current	V_{CPout}=V_{CC}/2, PLL_CP_GAIN = 0		100		µA
		V_{CPout}=V_{CC}/2, PLL_CP_GAIN = 1		400		
		V_{CPout}=V_{CC}/2, PLL_CP_GAIN = 2		1600		
		V_{CPout}=V_{CC}/2, PLL_CP_GAIN = 3		3200		
I_{CPout}SINK	PLL Charge Pump Sink Current	V_{CPout}=V_{CC}/2, PLL_CP_GAIN = 0		-100		µA
		V_{CPout}=V_{CC}/2, PLL_CP_GAIN = 1		-400		
		V_{CPout}=V_{CC}/2, PLL_CP_GAIN = 2		-1600		
		V_{CPout}=V_{CC}/2, PLL_CP_GAIN = 3		-3200		
I_{CPout}%MIS	Charge Pump Sink/Source Mismatch	V_{CPout}=V_{CC}/2, T_A = 25 °C		3	10	%
$I_{CPout}V_{TUNE}$	Magnitude of Charge Pump Current vs. Charge Pump Voltage Variation	0.5 V < V_{CPout} < V_{CC} - 0.5 V T_A = 25 °C		4		%
I_{CPout}%TEMP	Charge Pump Current vs. Temperature Variation			4		%
I_{CPout}TRI	Charge Pump Leakage	0.5 V < V_{CPout} < V_{CC} - 0.5 V			10	nA
PN10kHz	PLL 1/f Noise at 10 kHz offset [18]. Normalized to 1 GHz Output Frequency	PLL_CP_GAIN = 400 µA		-118		dBc/Hz
		PLL_CP_GAIN = 3200 µA		-121		
PN1Hz	Normalized Phase Noise Contribution [19]	PLL_CP_GAIN = 400 µA		-222.5		dBc/Hz
		PLL_CP_GAIN = 3200 µA		-227		
L(f)	PLL Phase Noise (Assumes a very wide bandwidth, noiseless crystal, 2500 MHz output frequency, and 25 MHz phase detector frequency)	1 kHz Offset		-93		dBc/Hz
		10 kHz		-103		
		100 kHz Offset		-116		
		1 MHz Offset		-116		
Internal VCO Specifications						
f_{VCO}	VCO Tuning Range		2370		2600	MHz
K_{VCO}	Fine Tuning Sensitivity (The range displayed in the typical column indicates the lower sensitivity is typical at the lower end of the tuning range, and the higher tuning sensitivity is typical at the higher end of the tuning range).			16 to 21		MHz/V
$\|\Delta T_{CL}\|$	Allowable Temperature Drift for Continuous Lock [20] [21]	After programming R30 for lock, no changes to output configuration are permitted to guarantee continuous lock			125	°C

(18) A specification in modeling PLL in-band phase noise is the 1/f flicker noise, $L_{PLL\_flicker}(f)$, which is dominant close to the carrier. Flicker noise has a 10 dB/decade slope. PN10kHz is normalized to a 10 kHz offset and a 1 GHz carrier frequency. PN10kHz = $L_{PLL\_flicker}$(10 kHz) - 20log(Fout / 1 GHz), where $L_{PLL\_flicker}(f)$ is the single side band phase noise of only the flicker noise's contribution to total noise, L(f). To measure $L_{PLL\_flicker}(f)$ it is important to be on the 10 dB/decade slope close to the carrier. A high compare frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f). $L_{PLL\_flicker}(f)$ can be masked by the reference oscillator performance if a low power or noisy source is used. The total PLL in-band phase noise performance is the sum of $L_{PLL\_flicker}(f)$ and $L_{PLL\_flat}(f)$.

(19) A specification modeling PLL in-band phase noise. The normalized phase noise contribution of the PLL, $L_{PLL\_flat}(f)$, is defined as: PN1HZ=$L_{PLL\_flat}(f)$ - 20log(N) - 10log(f_{PD}). $L_{PLL\_flat}(f)$ is the single side band phase noise measured at an offset frequency, f, in a 1 Hz bandwidth and f_{PD} is the phase detector frequency of the synthesizer. $L_{PLL\_flat}(f)$ contributes to the total noise, L(f).

(20) Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the R30 register was last programmed, and still have the part stay in lock. The action of programming the R30 register, even to the same value, activates a frequency calibration routine. This implies the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the R30 register to ensure it stays in lock. Regardless of what temperature the part was initially programmed at, the temperature can never drift outside the frequency range of -40 °C to 85 °C without violating specifications.

(21) Guaranteed by characterization.

Electrical Characteristics[1] (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C, Junction Temperature T_J ≤ 125 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
L(f)	Phase Noise (Assumes a very narrow loop bandwidth)	10 kHz Offset		-87		dBc/Hz
		100 kHz Offset		-112		
		1 MHz Offset		-133		
Clock Skew						
$\|T_{SKEW}\|$	Maximum CLKoutX to CLKoutY (22) (21)	LVDS-to-LVDS, T = 25 °C, f_{CLK} = 800 MHz, R_L= 100 Ω AC coupled		30		ps
		LVPECL-to-LVPECL, T = 25 °C, f_{CLK} = 800 MHz, R_L= 100 Ω emitter resistors = 240 Ω to GND AC coupled		30		
	Maximum skew between any two LVCMOS outputs, same CLKout or different CLKout (22) (21)	R_L = 50 Ω, C_L = 5 pF, T = 25 °C, F_{CLK} = 100 MHz. (22)		100		
$Mixed_{SKEW}$	LVDS or LVPECL to LVCMOS	Same device, T = 25 °C, 250 MHz		750		ps
LVDS Clock Outputs (CLKoutX), CLKoutX_TYPE = 1						
f_{CLKout}	Operating Frequency (21) (23)	R_L = 100 Ω			1300	MHz
V_{OD}	Differential Output Voltage Figure 5	T = 25 °C, DC measurement AC coupled to receiver input R = 100 Ω differential termination	250	400	450	|mV|
V_{SS}			500	800	900	mVpp
ΔV_{OD}	Change in Magnitude of V_{OD} for complementary output states		-50		50	mV
V_{OS}	Output Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} for complementary output states				35	|mV|
T_R / T_F	Output Rise Time	20% to 80%, R_L = 100 Ω		200		ps
	Output Fall Time	80% to 20%, R_L = 100 Ω				
I_{SA} I_{SB}	Output short circuit current - single-ended	Single-ended output shorted to GND, T = 25 °C	-24		24	mA
I_{SAB}	Output short circuit current - differential	Complimentary outputs tied together, T = 25 °C	-12		12	mA
LVPECL Clock Outputs (CLKoutX)						
f_{CLKout}	Operating Frequency (24) (25)				1300	MHz
T_R / T_F	20% to 80% Output Rise	R_L = 100 Ω, emitter resistors = 240 Ω to GND CLKoutX_TYPE = 4 or 5 (1600 or 2000 mVpp)		150		ps
	80% to 20% Output Fall Time					

(22) Equal loading and identical clock output configuration on each clock output is required for specification to be valid.
(23) Refer to typical performance charts for output operation performance at higher frequencies than the minimum maximum output frequency.
(24) Guaranteed by characterization.
(25) Refer to typical performance charts for output operation performance at higher frequencies than the minimum maximum output frequency.

Electrical Characteristics(1) (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C, Junction Temperature T_J ≤ 125 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
700 mVpp LVPECL Clock Outputs (CLKoutX), CLKoutX_TYPE = 2						
V_{OH}	Output High Voltage	T = 25 °C, DC measurement Termination = 50 Ω to V_{CC} - 1.4 V		V_{CC} - 1.03		V
V_{OL}	Output Low Voltage			V_{CC} - 1.41		V
V_{OD}	Output Voltage Figure 5		305	380	440	|mV|
V_{SS}			610	760	880	mVpp
1200 mVpp LVPECL Clock Outputs (CLKoutX), CLKoutX_TYPE = 3						
V_{OH}	Output High Voltage	T = 25 °C, DC measurement Termination = 50 Ω to V_{CC} - 1.7 V		V_{CC} - 1.07		V
V_{OL}	Output Low Voltage			V_{CC} - 1.69		V
V_{OD}	Output Voltage Figure 5		545	625	705	|mV|
V_{SS}			1090	1250	1410	mVpp
1600 mVpp LVPECL Clock Outputs (CLKoutX), CLKoutX_TYPE = 4						
V_{OH}	Output High Voltage	T = 25 °C, DC Measurement Termination = 50 Ω to V_{CC} - 2.0 V		V_{CC} - 1.10		V
V_{OL}	Output Low Voltage			V_{CC} - 1.97		V
V_{OD}	Output Voltage Figure 5		660	870	965	|mV|
V_{SS}			1320	1740	1930	mVpp
2000 mVpp LVPECL (2VPECL) Clock Outputs (CLKoutX), CLKoutX_TYPE = 5						
V_{OH}	Output High Voltage	T = 25 °C, DC Measurement Termination = 50 Ω to V_{CC} - 2.3 V		V_{CC} - 1.13		V
V_{OL}	Output Low Voltage			V_{CC} - 2.20		V
V_{OD}	Output Voltage Figure 5		800	1070	1200	|mV|
V_{SS}			1600	2140	2400	mVpp
LVCMOS Clock Outputs (CLKoutX)						
f_{CLKout}	Operating Frequency (26)	5 pF Load			250	MHz
V_{OH}	Output High Voltage	1 mA Load	V_{CC} - 0.1			V
V_{OL}	Output Low Voltage	1 mA Load			0.1	V
I_{OH}	Output High Current (Source)	V_{CC} = 3.3 V, V_O = 1.65 V		28		mA
I_{OL}	Output Low Current (Sink)	V_{CC} = 3.3 V, V_O = 1.65 V		28		mA
$DUTY_{CLK}$	Output Duty Cycle (26)	V_{CC}/2 to V_{CC}/2, F_{CLK} = 100 MHz, T = 25 °C	45	50	55	%
T_R	Output Rise Time	20% to 80%, R_L = 50 Ω, CL = 5 pF		400		ps
T_F	Output Fall Time	80% to 20%, R_L = 50 Ω, CL = 5 pF		400		ps
Digital Outputs (Ftest/LD, Readback, GPoutX)						
V_{OH}	High-Level Output Voltage	I_{OH} = -500 µA	V_{CC} - 0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 500 µA			0.4	V

(26) Guaranteed by characterization.

Electrical Characteristics[1] (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C, Junction Temperature T_J ≤ 125 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital Inputs (SYNC)						
V_{IH}	High-Level Input Voltage		1.6		V_{CC}	V
V_{IL}	Low-Level Input Voltage				0.4	V
Digital Inputs (CLKuWire, DATAuWire, LEuWire)						
V_{IH}	High-Level Input Voltage		1.6		V_{CC}	V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IH}	High-Level Input Current	V_{IH} = V_{CC}	5		25	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0	-5		5	µA
MICROWIRE Interface Timing						
T_{ECS}	LE to Clock Set Up Time	See MICROWIRE Input Timing	25			ns
T_{DCS}	Data to Clock Set Up Time	See MICROWIRE Input Timing	25			ns
T_{CDH}	Clock to Data Hold Time	See MICROWIRE Input Timing	8			ns
T_{CWH}	Clock Pulse Width High	See MICROWIRE Input Timing	25			ns
T_{CWL}	Clock Pulse Width Low	See MICROWIRE Input Timing	25			ns
T_{CES}	Clock to LE Set Up Time	See MICROWIRE Input Timing	25			ns
T_{EWH}	LE Pulse Width	See MICROWIRE Input Timing	25			ns
T_{CR}	Falling Clock to Readback Time	See MICROWIRE Readback Timing	25			ns

MEASUREMENT DEFINITIONS

SERIAL MICROWIRE TIMING DIAGRAM AND TERMINOLOGY

Register programming information on the DATAuWire pin is clocked into a shift register on each rising edge of the CLKuWire signal. On the rising edge of the LEuWire signal, the register is sent from the shift register to the register addressed. A few programming considerations are listed below:

- A slew rate of at least 30 V/us is recommended for the programming signals
- After the programming is complete, the CLKuWire, DATAuWire, and LEuWire signals should be returned to a low state
- If the CLKuWire or DATAuWire lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during this programming.

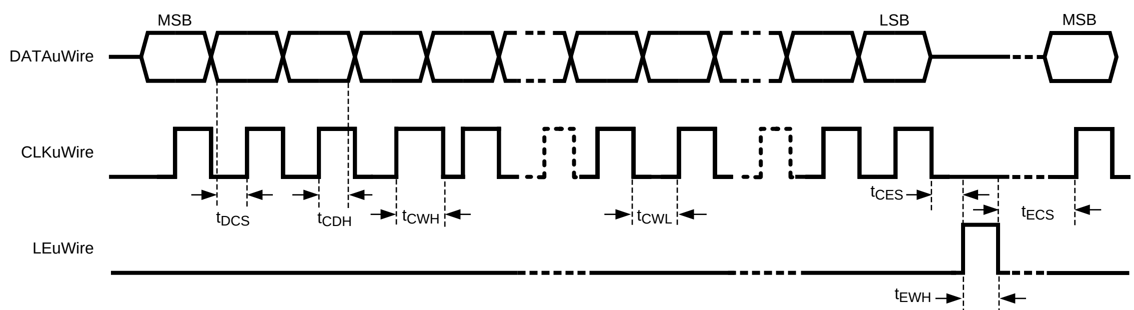


Figure 3. MICROWIRE Timing Diagram

DIFFERENTIAL VOLTAGE MEASUREMENT TERMINOLOGY

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 4 illustrates the two different definitions side-by-side for inputs and Figure 5 illustrates the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

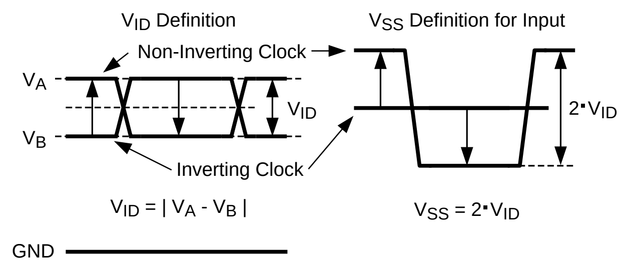


Figure 4. Two Different Definitions for Differential Input Signals

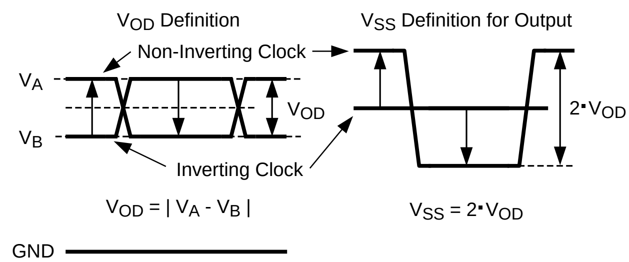


Figure 5. Two Different Definitions for Differential Output Signals

Refer to application note AN-912 Common Data Transmission Parameters and their Definitions for more information.

Typical Performance Characteristics

CLOCK OUTPUT AC CHARACTERISTICS

LVDS V_{OD} vs. Frequency

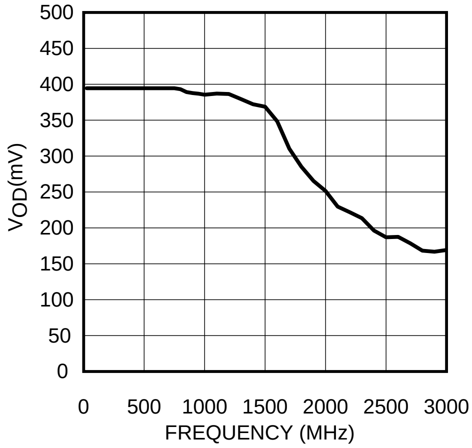


Figure 6.

LVPECL /w 240 ohm emitter resistors V_{OD} vs. Frequency

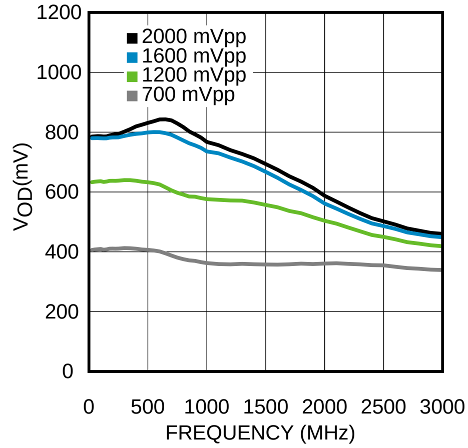


Figure 7.

LVPECL /w 120 ohm emitter resistors V_{OD} vs. Frequency

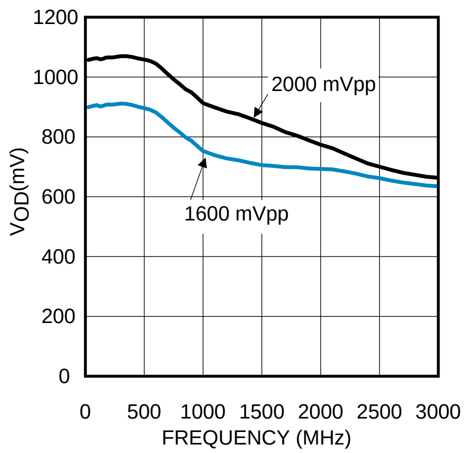


Figure 8.

FEATURES

CRYSTAL SUPPORT WITH BUFFERED OUTPUTS

The LMK03806 provides 2 dedicated outputs which are a buffered copy of the PLL reference input. This reference input is typically a low noise external clock or Crystal.

The OSCout0 buffer output type is programmable to LVDS, LVPECL, or LVCMOS. The OSCout1 buffer is fixed to LVPECL.

The dedicated output buffers OSCout0 and OSCout1 can output frequency lower than the Input frequency by programming the OSC Divider. The OSC Divider value range is 1 to 8. Each OSCoutX can individually choose to use the OSC Divider output or to bypass the OSC Divider.

Crystal buffered outputs cannot be synchronized to the VCO clock distribution outputs. The assertion of SYNC will still cause these outputs to become low. Since these outputs will turn off and on asynchronously with respect to the VCO sourced clock outputs during a SYNC, it is possible for glitches to occur on the buffered clock outputs when SYNC is asserted and unasserted. If the NO_SYNC_CLKoutX_Y bits are set these outputs will not be affected by the SYNC event except that the phase relationship will change with the other synchronized clocks unless a buffered clock output is used as a qualification clock during SYNC.

INTEGRATED LOOP FILTER POLES

The LMK03806 features programmable 3rd and 4th order loop filter poles for PLL. These internal resistors and capacitor values may be selected from a fixed range of values to achieve either a 3rd or 4th order loop filter response. The integrated programmable resistors and capacitors compliment external components mounted near the chip.

These integrated components can be effectively disabled by programming the integrated resistors and capacitors to their minimum values.

INTEGRATED VCO

The output of the internal VCO is routed to the Clock Distribution Path and also fed back to the PLL phase detector through a prescaler and N-divider.

CLOCK DISTRIBUTION

The LMK03806 features a total of 12 outputs driven from the internal or external VCO.

All VCO driven outputs have programmable output types. They can be programmed to LVPECL, LVDS, or LVCMOS. When all distribution outputs are configured for LVCMOS or single-ended LVPECL a total of 24 outputs are available.

CLKout DIVIDER

Each clock group, which is a pair of outputs such as CLKout0 and CLKout1, has a single clock output divider. The divider supports a divide range of 1 to 1045 (even and odd) with 50% output duty cycle. When divides of 26 or greater are used, the divider block uses extended mode.

PROGRAMMABLE OUTPUT TYPE

For increased flexibility all LMK03806 clock outputs (CLKoutX) and OSCout0 can be programmed to an LVDS, LVPECL, or LVCMOS output type. OSCout1 is fixed as LVPECL.

Any LVPECL output type can be programmed to 700, 1200, 1600, or 2000 mVpp amplitude levels. The 2000 mVpp LVPECL output type is a National Semiconductor proprietary configuration that produces a 2000 mVpp differential swing for compatibility with many data converters and is also known as 2VPECL.

CLOCK OUTPUT SYNCHRONIZATION

Using the SYNC input causes all active clock outputs to share a rising edge.

By toggling the SYNC_POL_INV bit, it is possible to generate a SYNC through uWire eliminating the need for connecting the external SYNC pin to external circuitry.

DEFAULT STARTUP CLOCKS

Before the LMK03806 is programmed some clocks will operate at default frequencies upon power up. The active output clocks depend upon the reference input type. If a crystal reference is used with OSCin, only CLKout8 will operate at a nominal VCO frequency /25. When an XO or other external reference is used as a reference with OSCin, OSCout0 will buffer the OSCin frequency in addition to CLKout8 operating at a nominal VCO frequency /25. These clocks can be used to clock external devices such as microcontrollers, FPGAs, CPLDs, etc. before the LMK03806 is programmed. Refer to Figure 9 or Figure 10 for illustration of startup clocks.

The nominal VCO frequency of CLKout8 on power up will typically be 98 MHz.

Note during programming CLKout8 may momentarily stop or glitch during the VCO calibration routine.

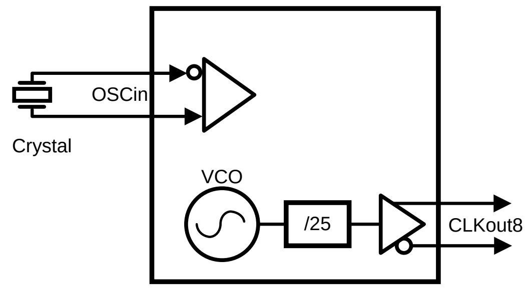


Figure 9. Startup Clock using Crystal Reference

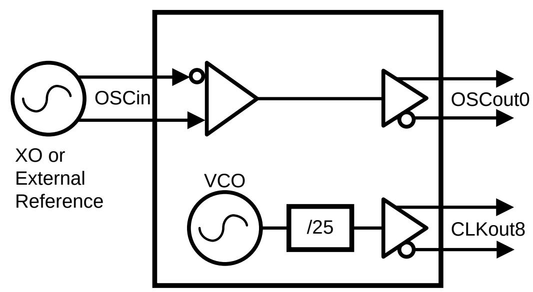


Figure 10. Startup Clock using XO or other External Reference

General Programming Information

LMK03806 devices are programmed using 32-bit registers. Each register consists of a 5-bit address field and 27-bit data field. The address field is formed by bits 0 through 4 (LSBs) and the data field is formed by bits 5 through 31 (MSBs). The contents of each register is clocked in MSB first (bit 31), and the LSB (bit 0) last. During programming, the LEuWire signal should be held *low*. The serial data is clocked in on the rising edge of the CLKuWire signal. After the LSB (bit 0) is clocked in the LEuWire signal should be toggled *low*-to-*high*-to-*low* to latch the contents into the register selected in the address field. It is recommended to program registers in numeric order, for example R0 to R14, R16, R24, R26, and R28 to R31 to achieve proper device operation. Refer to the electric specifications sections for the timing for the programming.

To achieve proper frequency calibration, the OSCin port must be driven with a valid signal before programming register R30. Changes to PLL R divider or the OSCin port frequency require register R30 to be reloaded in order to activate the frequency calibration process.

SPECIAL PROGRAMMING CASE FOR R0 to R5 for CLKoutX_Y_DIV > 25

When programming register R0 to R5 to change the CLKoutX_Y_DIV divide value, the register must be programmed twice if the CLKoutX_Y_DIV value is greater than 25.

RECOMMENDED INITIAL PROGRAMMING SEQUENCE

The registers are to be programmed in numeric order with R0 being the first and R31 being the last register programmed as shown below:

1. Program R0 with RESET bit = 1. This ensures that the device is configured with default settings. When RESET = 1, all other R0 bits are ignored.
   – If R0 is programmed again during the initial configuration of the device, the RESET bit must be cleared.
2. R0 through R5: CLKouts.
   – Program as necessary to configure the clock outputs, CLKout0 to CLKout11 as desired. These registers configure clock output controls such as powerdown, divider value, and clock source select.
3. R6 through R8: CLKouts.
   – Program as necessary to configure the clock outputs, CLKout0 to CLKout11 as desired. These registers configure the output format for each clock output.
4. R9: Undisclosed bits.
   – Program this register as shown in the register map for proper operation.
5. R10: OSCouts.
6. R11: SYNC, and XTAL.
7. R12: LD pin and SYNC.
8. R13: Readback pin & GPout0.
9. R14: GPout1.
10. R16: Undisclosed bits.
    – Program this register as shown in the register map for proper operation.
11. R24: Partially integrated PLL filter values.
12. R26, R28, R29, and R30: PLL.
13. R31: uWire readback and uWire lock.

READBACK

At no time should the MICROWIRE registers be programmed to any value other than what is specified in the datasheet.

For debug of the MICROWIRE interface or programming, it is recommended to simply program an LD_MUX to active low and then toggle the output type register between output and inverting output while observing the output pin for a low to high transition. For example, to verify MICROWIRE programming, set the LD_MUX = 0 (Low) and then toggle the LD_TYPE register between 3 (Output, push-pull) and 4 (Output inverted, pushpull). The result will be that the Ftest/LD pin will toggle from low to high.

Readback from the MICROWIRE programming registers is available. The MICROWIRE readback function can be accessed on the Readback pin. The READBACK_TYPE register can be programmed to "Output (push-pull)" for active output, or for communication with FPGAs/microcontrollers with lower voltage rails than 3.3 V the READBACK_TYPE register can be programmed to "Output (Open-Drain)" while connecting an external pull-up resistor to the voltage rail needed.

To perform a readback operation:

1. Write the register address to be read back by programming the READBACK_ADDR register in R31.
2. With the LEuWire pin held low continue to clock the CLKuWire pin. On every rising edge of the CLKuWire pin a new data bit is clocked onto the Readback pin.
3. Data is clocked out MSB first. After 32 clocks all the data values will have been read and the read operation is complete. The 5 LSB bits which are the address will be undefined during readback.

Readback example

To readback register R3 perform the following steps:

1. Write R31 with READBACK_ADDR = 3. DATAuWire and CLKuWire are toggled as shown in Figure 3 with new data being clocked in on rising edges of CLKuWire
2. Toggle LEuWire high and low as shown in Figure 3.

3. Toggle CLKuWire high and then low 32 times to read back all 32 bits of register R3. Data is read MSB first. Data is valid on falling edge of CLKuWire.

REGISTER MAP

Table 1 provides the register map for device programming. At no time should registers be programmed to undefined values. Only valid register values should be written.

Table 1. Register Map

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data [26:0]																											Address [4:0]				
R0	CLKout0_1_PD	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET	0	CLKout0_1_DIV [15:5]											0	0	0	0	0
R1	CLKout2_3_PD	0	0	0	0	0	0	0	0	0	0	0	0	0	POWERDOWN	0	CLKout2_3_DIV [15:5]											0	0	0	0	1
R2	CLKout4_5_PD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout4_5_DIV [15:5]											0	0	0	1	0
R3	CLKout6_7_PD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout6_7_DIV [15:5]											0	0	0	1	1
R4	CLKout8_9_PD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout8_9_DIV [15:5]											0	0	1	0	0
R5	CLKout10_11_PD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout10_11_DIV [15:5]											0	0	1	0	1
R6	CLKout3_TYPE [31:28]				CLKout2_TYPE [27:24]				CLKout1_TYPE [23:20]				CLKout0_TYPE [19:16]				0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R7	CLKout7_TYPE [31:28]				CLKout6_TYPE [27:24]				CLKout5_TYPE [23:20]				CLKout4_TYPE [19:16]				0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R8	CLKout11_TYPE [31:28]				CLKout10_TYPE [27:24]				CLKout9_TYPE [23:20]				CLKout8_TYPE [19:16]				0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R9	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	0	1	0	0	1
R10	OSCout1_TYPE [31:30]		0	**1**	OSCout0_TYPE [27:24]				EN_OSCout1	EN_OSCout0	OSCout1_MUX	OSCout0_MUX	0	OSCout_DIV [18:16]			0	**1**	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R11	0	0	**1**	**1**	0	**1**	NO_SYNC_CLKout10_11	NO_SYNC_CLKout8_9	NO_SYNC_CLKout6_7	NO_SYNC_CLKout4_5	NO_SYNC_CLKout2_3	NO_SYNC_CLKout0_1	0	0	0	SYNC_POL_INV	0	0	SYNC_TYPE [13:12]		0	0	0	0	0	0	EN_PLL_XTAL	0	1	0	1	1
R12	LD_MUX [31:27]					Ftest/LD_TYPE [26:24]			SYNC_PLL_DLD	0	0	0	**1**	**1**	0	0	0	0	0	0	0	0	0	0	0	**1**	**1**	0	1	1	0	0
R13	0	0	**1**	**1**	**1**	READBACK_TYPE [26:24]			0	0	0	0	0	GPout0 [18:16]			**1**	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
R14	0	0	0	0	0	GPout1 [26:24]			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
R16	**1**	**1**	0	0	0	0	0	**1**	0	**1**	0	**1**	0	**1**	0	**1**	0	0	0	0	0	**1**	0	0	0	0	0	1	0	0	0	0
R24	PLL_C4_LF [31:28]				PLL_C3_LF [27:24]				0	PLL_R4_LF [22:20]			0	PLL_R3_LF [18:16]			0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
R26	**1**	0	EN_PLL_REF_2X	0	PLL_CP_GAIN [27:26]		**1**	**1**	**1**	0	**1**	0	PLL_DLD_CNT [19:6]														0	1	1	0	1	0

Table 1. Register Map (continued)

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data [26:0]																											Address [4:0]				
R28	PLL_R												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
R29	0	0	0	0	0	OSCin_FREQ [26:24]			**1**	PLL_N_CAL [22:5]																		1	1	1	0	1
R30	0	0	0	0	0	PLL_P			0	PLL_N [22:5]																		1	1	1	1	0
R31	0	0	0	0	0	0	0	0	0	0	0	READBACK_ADDR [20:16]					0	0	0	0	0	0	0	0	0	0	uWire_LOCK	1	1	1	1	1

DEFAULT DEVICE REGISTER SETTINGS AFTER POWER ON RESET

Table 2 illustrates the default register settings programmed in silicon for the LMK03806 after power on or asserting the reset bit. Capital X and Y represent numeric values.

Table 2. Default Device Register Settings after Power On/Reset

Group	Field Name	Default Value (decimal)	Default State	Field Description	Register	Bit Location (MSB:LSB)
Clock Output Control	CLKout0_1_PD	1	PD	Powerdown control for divider, and both output buffers	R0	31
	CLKout2_3_PD	1	PD		R1	
	CLKout4_5_PD	1	PD		R2	
	CLKout6_7_PD	0	Normal		R3	
	CLKout8_9_PD	0	Normal		R4	
	CLKout10_11_PD	1	PD		R5	
	RESET	0	Not in reset	Performs power on reset for device	R0	17
	POWERDOWN	0	Disabled (device is active)	Device power down control	R1	17
	CLKout0_1_DIV	25	Divide-by-25	Divide for clock outputs	R0	15:5 [11]
	CLKout2_3_DIV	25	Divide-by-25		R1	
	CLKout4_5_DIV	25	Divide-by-25		R2	
	CLKout6_7_DIV	1	Divide-by-1		R3	
	CLKout8_9_DIV	25	Divide-by-25		R4	
	CLKout10_11_DIV	25	Divide-by-25		R5	
	CLKout3_TYPE	0	Powerdown	Individual clock output format. Select from LVDS/LVPECL/LVCMOS.	R6	31:28 [4]
	CLKout7_TYPE	0	Powerdown		R7	
	CLKout11_TYPE	0	Powerdown		R8	
	CLKout2_TYPE	0	Powerdown		R6	27:24 [4]
	CLKout6_TYPE	8	LVCMOS (Norm/Norm)		R7	
	CLKout10_TYPE	0	Powerdown		R8	
	CLKout1_TYPE	0	Powerdown		R6	23:20 [4]
	CLKout5_TYPE	0	Powerdown		R7	
	CLKout9_TYPE	0	Powerdown		R8	
	CLKout0_TYPE	0	Powerdown		R6	19:16 [4]
	CLKout4_TYPE	0	Powerdown		R7	
	CLKout8_TYPE	1	LVDS		R8	
Osc Buffer Control Mode	OSCout1_TYPE	2	1600 mVpp LVPECL	Set LVPECL amplitude	R10	31:30 [2]
	OSCout0_TYPE	1	LVDS	OSCout0 default clock output	R10	27:24 [4]
	EN_OSCout1	0	Disabled	Disable OSCout1 output buffer	R10	23
	EN_OSCout0	1	Enabled	Enable OSCout0 output buffer	R10	22
	OSCout1_MUX	0	Bypass Divider	Select OSCout divider for OSCout1 or bypass	R10	21
	OSCout0_MUX	0	Bypass Divider	Select OSCout divider for OSCout0 or bypass	R10	20
	OSCout_DIV	0	Divide-by-8	OSCout divider value	R10	18:16 [3]

Table 2. Default Device Register Settings after Power On/Reset (continued)

Group	Field Name	Default Value (decimal)	Default State	Field Description	Register	Bit Location (MSB:LSB)
SYNC Control	NO_SYNC_CLKout10_11	0	Will sync	Disable individual clock groups from becoming synchronized.	R11	25
	NO_SYNC_CLKout8_9	1	Will not sync		R11	24
	NO_SYNC_CLKout6_7	1	Will not sync		R11	23
	NO_SYNC_CLKout4_5	0	Will sync		R11	22
	NO_SYNC_CLKout2_3	0	Will sync		R11	21
	NO_SYNC_CLKout0_1	0	Will sync		R11	20
	SYNC_POL_INV	1	Logic Low	Sets the polarity of the SYNC pin when input. (Use for software SYNC)	R11	16
	SYNC_TYPE	1	Input /w Pull-up	SYNC IO pin type	R11	13:12 [2]
Other Mode Control	EN_PLL_XTAL	0	Disabled	Enable Crystal oscillator for OSCin	R11	5
	LD_MUX	3	Reserved	Ftest/LD pin selection when output	R12	31:27 [5]
	LD_TYPE	3	Output (Push-Pull)	LD IO pin type	R12	26:24 [3]
	SYNC_PLL_DLD	0	No effect	When set, force SYNC until PLL locks	R12	23
	READBACK_TYPE	3	Output (Push-Pull)	Readback Pin Type	R13	26:24 [3]
GPout	GPout0	2	Weak pull-down	GPout0 output state	R13	18:16 [3]
	GPout1	2	Weak pull-down	GPout1 output state	R14	28:26 [3]
PLL Control	PLL_C4_LF	0	10 pF	PLL integrated capacitor C4 value	R24	31:28 [4]
	PLL_C3_LF	0	10 pF	PLL integrated capacitor C3 value	R24	27:24 [4]
	PLL_R4_LF	0	200 Ω	PLL integrated resistor R4 value	R24	22:20 [3]
	PLL_R3_LF	0	200 Ω	PLL integrated resistor R3 value	R24	18:16 [3]
	EN_PLL_REF_2X	0	Disabled, 1x	Doubles reference frequency of PLL.	R26	29
	PLL_CP_GAIN	3	3.2 mA	PLL Charge Pump Gain	R26	27:26 [2]
	PLL_DLD_CNT	8192	8192 Counts	Number of PDF cycles which phase error must be within DLD window before LD state is asserted.	R26	19:6 [14]
	PLL_R	4	Divide-by-4	PLL R Divider (1 to 4095)	R28	31:20 [12]
	OSCin_FREQ	7	448 to 500 MHz	OSCin frequency range	R29	26:24 [3]
	PLL_N_CAL	48	Divide-by-48	Must be programmed to PLL_N value.	R29	22:5 [18]
	PLL_P	2	Divide-by-2	PLL N Divider Prescaler (2 to 8)	R30	26:24 [3]
	PLL_N	48	Divide-by-48	PLL N Divider (1 to 262143)	R30	22:5 [18]
uWire	uWire_LOCK	0	Writable	The values of registers R0 to R30 are lockable	R31	5

REGISTER R0 TO R5

Registers R0 through R5 control the 12 clock outputs CLKout0 to CLKout11. Register R0 controls CLKout0 and CLKout1, Register R1 controls CLKout2 and CLKout3, and so on. The X and Y in CLKoutX_Y_PD, CLKoutX_Y_DIV denote the actual clock output which may be from 0 to 11 where X is even and Y is odd. Two clock outputs CLKoutX and CLKoutY form a clock output group and are often run together in bit names as CLKoutX_Y.

Two additional bits within the R0 to R5 register range are:

- The RESET bit, which is only in register R0.
- The POWERDOWN bit, which is only in register R1.

CLKoutX_Y_PD, Powerdown CLKoutX_Y Output Path

This bit powers down the clock group as specified by CLKoutX and CLKoutY. This includes the divider and output buffers.

Table 3. CLKoutX_Y_PD

R0-R5[31]	State
0	Power up clock group
1	Power down clock group

RESET

The RESET bit is located in register R0 only. Setting this bit will cause the silicon default values to be loaded. When programming register R0 with the RESET bit set, all other programmed values are ignored. After resetting the device, the register R0 must be programmed again (with RESET = 0) to set non-default values in register R0.

The reset occurs on the falling edge of the LEuWire pin which loaded R0 with RESET = 1.

The RESET bit is automatically cleared upon writing any other register. For instance, when R0 is written to again with default values.

Table 4. RESET

R0[17]	State
0	Normal operation
1	Reset (automatically cleared)

POWERDOWN

The POWERDOWN bit is located in register R1 only. Setting the bit causes the device to enter powerdown mode. Normal operation is resumed by clearing this bit with MICROWIRE.

Table 5. POWERDOWN

R1[17]	State
0	Normal operation
1	Powerdown

CLKoutX_Y_DIV, Clock Output Divide

CLKoutX_Y_DIV sets the divide value for the clock group. The divide may be even or odd. Both even and odd divides output a 50% duty cycle clock.

Using a divide value of 26 or greater will cause the clock group to operate in extended mode.

Programming CLKoutX_Y_DIV can require special attention.

Table 6. CLKoutX_Y_DIV, 11 bits

R0-R5[15:5]	Divide Value	Power Mode
0 (0x00)	Reserved	Normal Mode
1 (0x01)	1	
2 (0x02)	2 (1)	
3 (0x03)	3	
4 (0x04)	4 (1)	
5 (0x05)	5 (1)	
6 (0x06)	6	
...	...	
24 (0x18)	24	
25 (0x19)	25	
26 (0x1A)	26	Extended Mode
27 (0x1B)	27	
...	...	
1044 (0x414)	1044	
1045 (0x415)	1045	

(1) After programming PLL_N value, a SYNC must occur on channels using this divide value. Programming PLL_N does generate a SYNC event automatically which satisfies this requirement, but NO_SYNC_CLKoutX_Y must be set to 0 for these clock groups.

REGISTERS R6 TO R8

CLKoutX_TYPE

The clock output types of the LMK03806 are individually programmable. The CLKoutX_TYPE registers set the output type of an individual clock output to LVDS, LVPECL, LVCMOS, or powers down the output buffer. Note that LVPECL supports four different amplitude levels and LVCMOS supports single LVCMOS outputs, inverted, and normal polarity of each output pin for maximum flexibility.

The programming addresses table shows at what register and address the specified clock output CLKoutX_TYPE register is located.

The CLKoutX_TYPE table shows the programming definition for these registers.

Table 7. CLKoutX_TYPE Programming Addresses

CLKoutX	Programming Address
CLKout0	R6[19:16]
CLKout1	R6[23:20]
CLKout2	R6[27:24]
CLKout3	R6[31:28]
CLKout4	R7[19:16]
CLKout5	R7[23:20]
CLKout6	R7[27:24]
CLKout7	R7[31:28]
CLKout8	R8[19:16]
CLKout9	R8[23:20]
CLKout10	R8[27:24]
CLKout11	R8[31:28]

Table 8. CLKoutX_TYPE, 4 bits

R6-R8[31:28, 27:24, 23:20]	Definition
0 (0x00)	Power down
1 (0x01)	LVDS

Table 8. CLKoutX_TYPE, 4 bits (continued)

R6-R8[31:28, 27:24, 23:20]	Definition
2 (0x02)	LVPECL (700 mVpp)
3 (0x03)	LVPECL (1200 mVpp)
4 (0x04)	LVPECL (1600 mVpp)
5 (0x05)	LVPECL (2000 mVpp)
6 (0x06)	LVCMOS (Norm/Inv)
7 (0x07)	LVCMOS (Inv/Norm)
8 (0x08) (1)	LVCMOS (Norm/Norm)
9 (0x09) (1)	LVCMOS (Inv/Inv)
10 (0x0A) (1)	LVCMOS (Low/Norm)
11 (0x0A) (1)	LVCMOS (Low/Inv)
12 (0x0C) (1)	LVCMOS (Norm/Low)
13 (0x0D) (1)	LVCMOS (Inv/Low)
14 (0x0E) (2)	LVCMOS (Low/Low)

(1) It is recommended to use one of the complementary LVCMOS modes. Best noise performance is achieved using LVCMOS (Norm/Inv) or LVCMOS (Inv/Norm) due to the differential switching of the outputs. The next best performance is achieved using an LVCMOS mode with only one output on. Finally, LVCMOS (Norm/Norm) or LVCMOS (Inv/Inv) have the create the most switching noise.
(2) It is recommended to use one of the complementary LVCMOS modes. Best noise performance is achieved using LVCMOS (Norm/Inv) or LVCMOS (Inv/Norm) due to the differential switching of the outputs. The next best performance is achieved using an LVCMOS mode with only one output on. Finally, LVCMOS (Norm/Norm) or LVCMOS (Inv/Inv) have the create the most switching noise.

REGISTER R9

Register 9 contains no user programmable bits, but must be programmed as described in the register map.

REGISTER R10

OSCout1_TYPE, LVPECL Output Amplitude Control

The OSCout1 clock output can only be used as an LVPECL output type. OSCout1_TYPE sets the LVPECL output amplitude of the OSCout1 clock output.

Table 9. OSCout1_TYPE, 2 bits

R10[31:30]	Output Format
0 (0x00)	LVPECL (700 mVpp)
1 (0x01)	LVPECL (1200 mVpp)
2 (0x02)	LVPECL (1600 mVpp)
3 (0x03)	LVPECL (2000 mVpp)

OSCout0_TYPE

The OSCout0 clock output has a programmable output type. The OSCout0_TYPE register sets the output type to LVDS, LVPECL, LVCMOS, or powers down the output buffer. Note that LVPECL supports four different amplitude levels and LVCMOS supports dual and single LVCMOS outputs with inverted, and normal polarity of each output pin for maximum flexibility.

To turn on the output, the OSCout0_TYPE must be set to a non-power down setting and enabled with EN_OSCoutX, OSCout Output Enable.

Table 10. OSCout0_TYPE, 4 bits

R10[27:24]	Definition
0 (0x00)	Powerdown
1 (0x01)	LVDS
2 (0x02)	LVPECL (700 mVpp)
3 (0x03)	LVPECL (1200 mVpp)

Table 10. OSCout0_TYPE, 4 bits (continued)

R10[27:24]	Definition
4 (0x04)	LVPECL (1600 mVpp)
5 (0x05)	LVPECL (2000 mVpp)
6 (0x06)	LVCMOS (Norm/Inv)
7 (0x07)	LVCMOS (Inv/Norm)
8 (0x08) (1)	LVCMOS (Norm/Norm)
9 (0x09) (1)	LVCMOS (Inv/Inv)
10 (0x0A) (1)	LVCMOS (Low/Norm)
11 (0x0B) (1)	LVCMOS (Low/Inv)
12 (0x0C) (1)	LVCMOS (Norm/Low)
13 (0x0D) (1)	LVCMOS (Inv/Low)
14 (0x0E) (1)	LVCMOS (Low/Low)

(1) It is recommended to use one of the complementary LVCMOS modes. Best noise performance is achieved using LVCMOS (Norm/Inv) or LVCMOS (Inv/Norm) due to the differential switching of the outputs. The next best performance is achieved using an LVCMOS mode with only one output on. Finally, LVCMOS (Norm/Norm) or LVCMOS (Inv/Inv) have the create the most switching noise.

EN_OSCoutX, OSCout Output Enable

EN_OSCoutX is used to enable an oscillator buffered output.

Table 11. EN_OSCout1

R10[23]	Output State
0	OSCout1 Disabled
1	OSCout1 Enabled

Table 12. EN_OSCout0

R10[22]	Output State
0	OSCout0 Disabled
1	OSCout0 Enabled

OSCout0 note: In addition to enabling the output with EN_OSCout0. The OSCout0_TYPE must be programmed to a non-power down value for the output buffer to power up.

OSCoutX_MUX, Clock Output Mux

Sets OSCoutX buffer to output a divided or bypassed OSCin signal. .

Table 13. OSCout1_MUX

R10[21]	Mux Output
0	Bypass divider
1	Divided

Table 14. OSCout0_MUX

R10[20]	Mux Output
0	Bypass divider
1	Divided

OSCout_DIV, Oscillator Output Divide

The OSCout divider can be programmed from 2 to 8. Divide by 1 is achieved by bypassing the divider with OSCoutX_MUX, Clock Output Mux.

Table 15. OSCout_DIV, 3 bits

R10[18:16]	Divide
0 (0x00)	8
1 (0x01)	2
2 (0x02)	2
3 (0x03)	3
4 (0x04)	4
5 (0x05)	5
6 (0x06)	6
7 (0x07)	7

REGISTER R11

NO_SYNC_CLKoutX_Y

The NO_SYNC_CLKoutX_Y bits prevent individual clock groups from becoming synchronized during a SYNC event. A reason to prevent individual clock groups from becoming synchronized is that during synchronization, the clock output is in a fixed low state or can have a glitch pulse.

By disabling SYNC on a clock group, it will continue to operate normally during a SYNC event.

Setting the NO_SYNC_CLKoutX_Y bit has no effect on clocks already synchronized together.

Table 16. NO_SYNC_CLKoutX_Y Programming Addresses

NO_SYNC_CLKoutX_Y	Programming Address
CLKout0 and 1	R11:20
CLKout2 and 3	R11:21
CLKout4 and 5	R11:22
CLKout6 and 7	R11:23
CLKout8 and 9	R11:24
CLKout10 and 11	R11:25

Table 17. NO_SYNC_CLKoutX_Y

R11[25, 24, 23, 22, 21, 20]	Definition
0	CLKoutX_Y will synchronize
1	CLKoutX_Y will not synchronize

SYNC_POL_INV

Sets the polarity of the SYNC pin when input. When SYNC is asserted the clock outputs will transition to a low state.

Table 18. SYNC_POL_INV

R11[16]	Polarity
0	SYNC is active high
1	SYNC is active low

SYNC_TYPE

Sets the IO type of the SYNC pin.

Table 19. SYNC_TYPE, 2 bits

R11[13:12]	Polarity
0 (0x00)	Input
1 (0x01)	Input /w pull-up resistor
2 (0x02)	Input /w pull-down resistor

EN_PLL_XTAL

If an external crystal is being used to implement a discrete VCXO, the internal feedback amplifier must be enabled with this bit in order to complete the oscillator circuit.

Table 20. EN_PLL_XTAL

R11[5]	Oscillator Amplifier State
0	Disabled
1	Enabled

REGISTER R12

LD_MUX

LD_MUX sets the output value of the Ftest/LD pin.

All the outputs logic is active high when LD_TYPE = 3 (Output). All the outputs logic is active low when LD_TYPE = 4 (Output Inverted). For example, when LD_MUX = 0 (Logic Low) and LD_TYPE = 3 (Output) then Ftest/LD pin outputs a logic low. When LD_MUX = 0 (Logic Low) and LD_TYPE = 4 (Output Inverted) then Ftest/LD pin outputs a logic high.

Table 21. LD_MUX, 5 bits

R12[31:27]	Divide
0 (0x00)	Logic Low
1 (0x01)	Reserved
2 (0x02)	PLL DLD
3 (0x03)	Reserved
...	...
12 (0x0C)	Reserved
13 (0x0D)	PLL N
14 (0x0E)	PLL N/2
15 (0x0F)	Reserved
16 (0x10)	Reserved
17 (0x11)	PLL R (1)
18 (0x12)	PLL R/2 (1)

(1) Only valid when LD_MUX is not set to 2 (PLL_DLD).

LD_TYPE

Sets the IO type of the LD pin.

Table 22. LD_TYPE, 3 bits

R12[26:24]	Polarity
0 (0x00)	Reserved
1 (0x01)	Reserved

Table 22. LD_TYPE, 3 bits (continued)

R12[26:24]	Polarity
2 (0x02)	Reserved
3 (0x03)	Output (push-pull)
4 (0x04)	Output inverted (push-pull)
5 (0x05)	Output (open source)
6 (0x06)	Output (open drain)

SYNC_PLL_DLD

By setting SYNC_PLL_DLD a SYNC mode will be engaged (asserted SYNC) until the PLL locks.

Table 23. SYNC_PLL_DLD

R12[23]	Sync Mode Forced
0	No
1	Yes

REGISTER R13

READBACK_TYPE

Sets the IO format of the readback pin. The open drain output type can be used to interface the LMK03806 with low voltage IO rails.

Table 24. READBACK_TYPE, 3 bits

R13[26:24]	Polarity
0 (0x00)	Reserved
1 (0x01)	Reserved
2 (0x02)	Reserved
3 (0x03)	Output (push-pull)
4 (0x04)	Output inverted (push-pull)
5 (0x05)	Output (open source)
6 (0x06)	Output (open drain)

GPout0

Sets the output state of the GPout0 pin.

Table 25. GPout0, 3 bits

R13[18:16]	Output State
0 (0x00)	Reserved
1 (0x01)	Reserved
2 (0x02)	Weak pull-down
3 (0x03)	Low (0 V)
4 (0x04)	High (3.3 V)

REGISTER 14

GPout1

Sets the output state of the GPout1 pin.

Table 26. GPout1, 3 bits

R14[26:24]	Output State
0 (0x00)	Reserved
1 (0x01)	Reserved
2 (0x02)	Weak pull-down
3 (0x03)	Low (0 V)
4 (0x04)	High (3.3 V)

REGISTER 16

Register 16 contains no user programmable bits, but must be programmed as described in the register map.

REGISTER 24

PLL_C4_LF, PLL Integrated Loop Filter Component

Internal loop filter components are available for the PLL, enabling either 3rd or 4th order loop filters without requiring external components.

Internal loop filter capacitor C4 can be set according to the following table.

Table 27. PLL_C4_LF, 4 bits

R24[31:28]	Loop Filter Capacitance (pF)
0 (0x00)	10 pF
1 (0x01)	15 pF
2 (0x02)	29 pF
3 (0x03)	34 pF
4 (0x04)	47 pF
5 (0x05)	52 pF
6 (0x06)	66 pF
7 (0x07)	71 pF
8 (0x08)	103 pF
9 (0x09)	108 pF
10 (0x0A)	122 pF
11 (0x0B)	126 pF
12 (0x0C)	141 pF
13 (0x0D)	146 pF
14 (0x0E)	Reserved
15 (0x0F)	Reserved

PLL_C3_LF, PLL Integrated Loop Filter Component

Internal loop filter components are available for the PLL, enabling either 3rd or 4th order loop filters without requiring external components.

Internal loop filter capacitor C3 can be set according to the following table.

Table 28. PLL_C3_LF, 4 bits

R24[27:24]	Loop Filter Capacitance (pF)
0 (0x00)	10 pF
1 (0x01)	11 pF
2 (0x02)	15 pF
3 (0x03)	16 pF
4 (0x04)	19 pF

Table 28. PLL_C3_LF, 4 bits (continued)

R24[27:24]	Loop Filter Capacitance (pF)
5 (0x05)	20 pF
6 (0x06)	24 pF
7 (0x07)	25 pF
8 (0x08)	29 pF
9 (0x09)	30 pF
10 (0x0A)	33 pF
11 (0x0B)	34 pF
12 (0x0C)	38 pF
13 (0x0D)	39 pF
14 (0x0E)	Reserved
15 (0x0F)	Reserved

PLL_R4_LF, PLL Integrated Loop Filter Component

Internal loop filter components are available for the PLL, enabling either 3rd or 4th order loop filters without requiring external components.

Internal loop filter resistor R4 can be set according to the following table.

Table 29. PLL_R4_LF, 3 bits

R24[22:20]	Resistance
0 (0x00)	200 Ω
1 (0x01)	1 kΩ
2 (0x02)	2 kΩ
3 (0x03)	4 kΩ
4 (0x04)	16 kΩ
5 (0x05)	Reserved
6 (0x06)	Reserved
7 (0x07)	Reserved

PLL_R3_LF, PLL Integrated Loop Filter Component

Internal loop filter components are available for the PLL, enabling either 3rd or 4th order loop filters without requiring external components.

Internal loop filter resistor R3 can be set according to the following table.

Table 30. PLL_R3_LF, 3 bits

R24[18:16]	Resistance
0 (0x00)	200 Ω
1 (0x01)	1 kΩ
2 (0x02)	2 kΩ
3 (0x03)	4 kΩ
4 (0x04)	16 kΩ
5 (0x05)	Reserved
6 (0x06)	Reserved
7 (0x07)	Reserved

REGISTER 26

EN_PLL_REF_2X, PLL Reference Frequency Doubler

Enabling the PLL reference frequency doubler allows for higher phase detector frequencies on the PLL than would normally be allowed with the given VCXO or Crystal frequency.

Higher phase detector frequencies reduces the PLL N values which makes the design of wider loop bandwidth filters possible.

Table 31. EN_PLL_REF_2X

R26[29]	Description
0	Reference frequency normal
1	Reference frequency doubled (2x)

PLL_CP_GAIN, PLL Charge Pump Current

This bit programs the PLL charge pump output current level.

Table 32. PLL_CP_GAIN, 2 bits

R26[27:26]	Charge Pump Current (µA)
0 (0x00)	100
1 (0x01)	400
2 (0x02)	1600
3 (0x03)	3200

PLL_DLD_CNT

The reference and feedback of the PLL must be within the window of acceptable phase error for **PLL_DLD_CNT** cycles before PLL digital lock detect is asserted.

Table 33. PLL_DLD_CNT, 14 bits

R26[19:6]	Divide
0 (0x00)	Reserved
1 (0x01)	1
2 (0x02)	2
3 (0x03)	3
...	...
16,382 (0x3FFE)	16,382
16,383 (0x3FFF)	16,383

REGISTER 28

PLL_R, PLL R Divider

The reference path into the PLL phase detector includes the PLL R divider.

The valid values for PLL_R are shown in the table below.

Table 34. PLL_R, 12 bits

R28[31:20]	Divide
0 (0x00)	Not Valid
1 (0x01)	1
2 (0x02)	2
3 (0x03)	3
...	...

Table 34. PLL_R, 12 bits (continued)

R28[31:20]	Divide
4,094 (0xFFE)	4,094
4,095 (0xFFF)	4,095

REGISTER 29

OSCin_FREQ, PLL Oscillator Input Frequency Register

The frequency of the PLL reference input to the PLL Phase Detector (OSCin/OSCin* port) must be programmed in order to support proper operation of the frequency calibration routine which locks the internal VCO to the target frequency.

Table 35. OSCin_FREQ, 3 bits

R29[26:24]	OSCin Frequency
0 (0x00)	0 to 63 MHz
1 (0x01)	>63 MHz to 127 MHz
2 (0x02)	>127 MHz to 255 MHz
3 (0x03)	Reserved
4 (0x04)	>255 MHz to 500 MHz

PLL_N_CAL, PLL N Calibration Divider

During the frequency calibration routine, the PLL uses the divide value of the PLL_N_CAL register instead of the divide value of the PLL_N register to lock the VCO to the target frequency.

Table 36. PLL_N_CAL, 18 bits

R29[22:5]	Divide
0 (0x00)	Not Valid
1 (0x01)	1
2 (0x02)	2
...	...
262,143 (0x3FFFF)	262,143

REGISTER 30

Programming Register 30 triggers the frequency calibration routine. This calibration routine will also generate a SYNC event.

PLL_P, PLL N Prescaler Divider

The PLL N Prescaler divides the output of the VCO and is connected to the PLL N divider.

Table 37. PLL_P, 3 bits

R30[26:24]	Divide Value
0 (0x00)	8
1 (0x01)	2
2 (0x02)	2
3 (0x03)	3
4 (0x04)	4
5 (0x05)	5
6 (0x06)	6
7 (0x07)	7

PLL_N, PLL N Divider

The feeback path into the PLL phase detector includes the PLL N divider.

Each time register 30 is updated via the MICROWIRE interface, a frequency calibration routine runs to lock the VCO to the target frequency. During this calibration PLL_N is substituted with PLL_N_CAL.

The valid values for PLL_N are shown in the table below.

Table 38. PLL_N, 18 bits

R30[22:5]	Divide
0 (0x00)	Not Valid
1 (0x01)	1
2 (0x02)	2
	...
262,143 (0x3FFFF)	262,143

REGISTER 31

READBACK_ADDR

Table 39. READBACK_ADDR

R31[20:16]	State
0	R0
1	R1
2	R2
3	R3
4	R4
5	R5
6	R6
7	R7
8	R8
9	R9
10	R10
11	R11
12	R12
13	R13
14	R14
15	Reserved
16	R16
17	Reserved
...	...
23	Reserved
24	R24
25	Reserved
26	R26
27	Reserved
28	R28
29	R29
30	R30

uWire_LOCK

Setting uWire_LOCK will prevent any changes to uWire registers R0 to R30. Only by clearing the uWire_LOCK bit in R31 can the uWire registers be unlocked and written to once more.

It is not necessary to lock the registers to perform a readback operation.

Table 40. uWire_LOCK

R31[5]	State
0	Registers unlocked
1	Registers locked, Write-protect

APPLICATION INFORMATION

Crystal Interface

The LMK03806 has an integrated crystal oscillator circuit on that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in Figure 11.

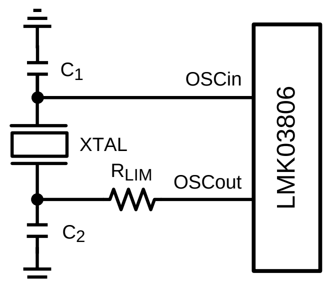


Figure 11. Crystal Interface

The load capacitance (C_L) is specific to the crystal, but usually on the order of 18 - 20 pF. While C_L is specified for the crystal, the OSCin input capacitance (C_{IN} = 6 pF typical) of the device and PCB stray capacitance (C_{STRAY} ~ 1~3 pF) can affect the discrete load capacitor values, C_1 and C_2.

For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically, $C_1 = C_2$ for optimum symmetry, so Equation 1 can be rewritten in terms of C_1 only:

$$C_L = C_1^{\,2} / (2 * C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for C_1:

$$C_1 = (C_L – C_{IN} – C_{STRAY})*2 \quad (3)$$

Electrical Characteristics provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal, P_{XTAL}, can be computed by:

$$P_{XTAL} = I_{RMS}^{\,2} * R_{ESR}*(1 + C_0/C_L)^2 \quad (4)$$

Where:

- I_{RMS} is the RMS current through the crystal.
- R_{ESR} is the max. equivalent series resistance specified for the crystal
- C_L is the load capacitance specified for the crystal
- C_0 is the min. shunt capacitance specified for the crystal

I_{RMS} can be measured using a current probe (e.g. Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCin* with the oscillation circuit active.

As shown in Figure 11, an external resistor, R_{LIM}, can be used to limit the crystal drive level, if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_{LIM} shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_{LIM} shorted, then a zero value for R_{LIM} can be used. As a starting point, a suggested value for R_{LIM} is 1.5 kΩ.

External Reference Interface

The LMK03806 has an the ability to be driven by an external reference. Typical external reference interfaces are shown in Figure 12 and Figure 13.

In applications where the external reference amplitude is less than the V_{OSCin} specification of 2.4 V_{pp} Figure 12 is an appropriate method of interfacing the reference to the LMK03806.

In applications where the external reference amplitude is greater than the V_{OSCin} specification of 2.4 V_{pp} Figure 13 is an appropriate method of interfacing the reference to the LMK03806.

In both cases C1 and C2 should be present a low impedance at the reference frequency. A typical value for C1 and C2 is 0.1 µF.

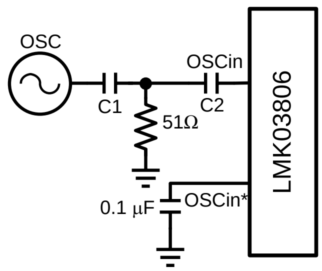


Figure 12. LVCMOS External Reference Interface

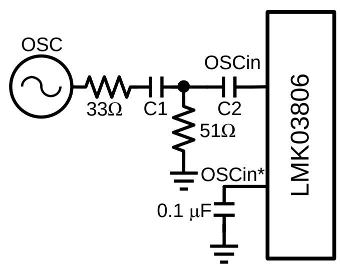


Figure 13. 3.3 V_{pp} External Reference Interface

Using an external reference, such as a crystal oscillator (XO), may provide better phase noise than a crystal at offsets below the loop bandwidth. If the jitter integration bandwidth for the application of interest is above the loop filter bandwidth, the added phase noise of a crystal will not be a significant jitter contributor and may be a more cost effective solution than an XO. Also, operating at higher reference frequencies allows higher phase detector frequencies, which also improves in band PLL phase noise performance.

DIGITAL LOCK DETECT

The digital lock detect circuit is used to determine the lock status of the PLL. The flowchart in Figure 14 shows the general way this circuit works.

Event	PLL	Window size (ε)	Lock count
PLL Locked	PLL	3.7 ns	PLL_DLD_CNT

For a digital lock detect event to occur there must be a number of PLL phase detector cycles during which the time/phase error of the PLL_R reference and PLL_N feedback signal edges are within the 3.7 ns window size of the LMK03806. “Lock count” is the term which is used to specify how many PLL phase detector cycles have been within the window size of 3.7 ns at any given time. Since there must be a specified number phase detector events before a lock event occurs, a minimum digital lock event time can be calculated as "lock count" / f_{PD}.

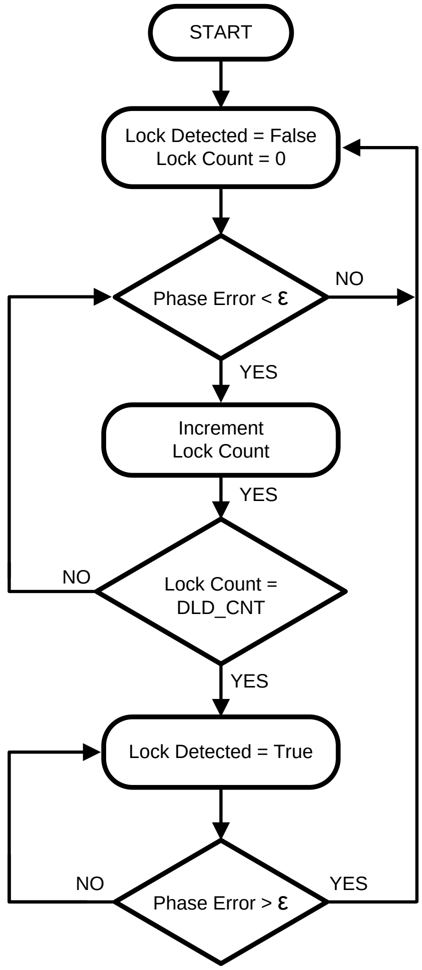


Figure 14. Digital Lock Detect Flow Diagram

A user specified ppm accuracy for lock detect is programmable using a lock count register. By using Equation 5, values for a "lock count" and "window size" can be chosen to set the frequency accuracy required by the system in ppm before the digital lock detect event occurs. Units of $_{PD}$ are Hertz:

$$ppm = \frac{2e6 \times 3.7\ ns \times f_{PD}}{PLL\_DLD\_CNT} \quad (5)$$

The effect of the "lock count" value is that it shortens the effective lock window size by dividing the "window size" by "lock count".

If at any time the PLL_R reference and PLL_N feedback signals are outside the time window set by "window size", then the “lock count” value is reset to 0.

For example, to calculate the minimum PLL digital lock time given a PLL phase detector frequency of 40 MHz and PLL_DLD_CNT = 10,000. Then the minimum lock time of PLL will be 10,000 / 40 MHz = 250 µs.

POWER SUPPLY

Current Consumption / Power Dissipation Calculations

From Table 41 the current consumption can be calculated for any configuration.

For example, the current for the entire device with 1 LVDS (CLKout0) and 1 LVPECL 1.6 Vpp /w 240 ohm emitter resistors (CLKout1) output active with a clock output divide = 1, and no other features enabled can be calculated by adding up the following blocks: core current, base clock distribution, clock output group, clock divider, one LVDS output buffer current, and one LVPECL output buffer current. There will also be one LVPECL output drawing emitter current, which means some of the power from the current draw of the device is dissipated in the external emitter resistors which doesn't add to the thermal power dissipation budget for the device. In addition to emitter resistor power, power dissipated in the load for LVDS/LVPECL do not contribute to the thermal power dissipation budget for the device.

For total current consumption of the device, add up the significant functional blocks. In this example, 212.9 mA =

- 122 mA (core current)
- 17.3 mA (base clock distribution)
- 2.8 mA (CLKout group for 2 outputs)
- 25.5 mA (CLKout0 & 1 divider)
- 14.3 mA (LVDS buffer)
- 31 mA (LVPECL 1.6 Vpp buffer /w 240 ohm emitter resistors)

Once total current consumption has been calculated, power dissipated by the device can be calculated. The power dissipation of the device is equation to the total current entering the device multiplied by the voltage at the device minus the power dissipated in any emitter resistors connected to any of the LVPECL outputs or any other external load power dissipation. Continuing the above example which has 212.9 mA total Icc and one output with 240 ohm emitter resistors and one LVDS output. Total IC power = 666 mW = 3.3 V * 212.9 mA - 35 mW - 1.5 mW.

Table 41. Typical Current Consumption for Selected Functional Blocks (T_A = 25 °C, V_{CC} = 3.3 V)

Block	Condition	Typical I_{CC} (mA)	Power dissipated in device (mW)(1)	Power dissipated externally (mW)(2)
Core and Functional Blocks				
Core	Internal VCO Locked	122	403	-
Base Clock Distribution	At least 1 CLKoutX_Y_PD = 0	17.3	57.1	-
CLKout Group	Each CLKout group (CLKout0/1 & 10/11, CLKout2/3 & 4/5, CLKout 6/7 & 8/9)	2.8	9.2	-
Clock Divider	Divide < 25	25.5	84.1	-
	Divide >= 25	29.6	97.7	-
SYNC Asserted	While SYNC is asserted, this extra current is drawn	1.7	5.6	-
Crystal Mode	Crystal Oscillator Buffer	1.8	5.9	-
OSCin Doubler	EN_OSCin_2X = 1	2.8	9.2	-
Clock Output Buffers				
LVDS	100 ohm differential termination	14.3	45.7	1.5

(1) Assuming θ_{JA} = 15 °C/W, the total power dissipated on chip must be less than (125 °C – 85 °C) / 16 °C/W = 2.5 W to guarantee a junction temperature is less than 125 °C.
(2) Worst case power dissipation can be estimated by multiplying typical power dissipation with a factor of 1.15.

Table 41. Typical Current Consumption for Selected Functional Blocks (T_A = 25 °C, V_{CC} = 3.3 V) (continued)

Block	Condition		Typical I_{CC} (mA)	Power dissipated in device (mW)(1)	Power dissipated externally (mW)(2)
LVPECL (3)	LVPECL 2.0 Vpp, AC coupled using 240 ohm emitter resistors		32	70.6	35
	LVPECL 1.6 Vpp, AC coupled using 240 ohm emitter resistors		31	67.3	35
	LVPECL 1.6 Vpp, AC coupled using 120 ohm emitter resistors		46	91.8	60
	LVPECL 1.2 Vpp, AC coupled using 240 ohm emitter resistors		30	59	40
	LVPECL 0.7 Vpp, AC coupled using 240 ohm emitter resistors		29	55.7	40
LVCMOS	LVCMOS Pair (CLKoutX_Y_TYPE = 6 to 10) C_L = 5 pF	3 MHz	24	79.2	-
		30 MHz	26.5	87.5	-
		150 MHz	36.5	120.5	-
	LVCMOS Single (CLKoutX_Y_TYPE = 11 to 13) C_L = 5 pF	3 MHz	15	49.5	-
		30 MHz	16	52.8	-
		150 MHz	21.5	71	-

(3) Power is dissipated externally in LVPECL emitter resistors. The externally dissipated power is calculated as twice the DC voltage level of one LVPECL clock output pin squared over the emitter resistance. That is to say power dissipated in emitter resistors = 2 * Vem^2 / Rem.

THERMAL MANAGEMENT

Power consumption of the LMK03806 can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125 °C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125 °C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to a printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in Figure 15. More information on soldering WQFN packages and gerber footprints can be obtained: http://www.national.com/analog/packaging/.

A recommended footprint including recommended solder mask and solder paste layers can be found at: http://www.national.com/analog/packaging/gerber for the NKD0064A package.

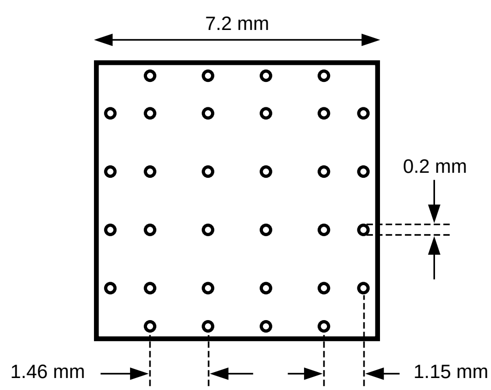


Figure 15. Recommended Land and Via Pattern

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in Figure 15 should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMK03806BISQ/NOPB	ACTIVE	WQFN	NKD	64	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	K03806BISQ	Samples
LMK03806BISQE/NOPB	ACTIVE	WQFN	NKD	64	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	K03806BISQ	Samples
LMK03806BISQX/NOPB	ACTIVE	WQFN	NKD	64	2000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	K03806BISQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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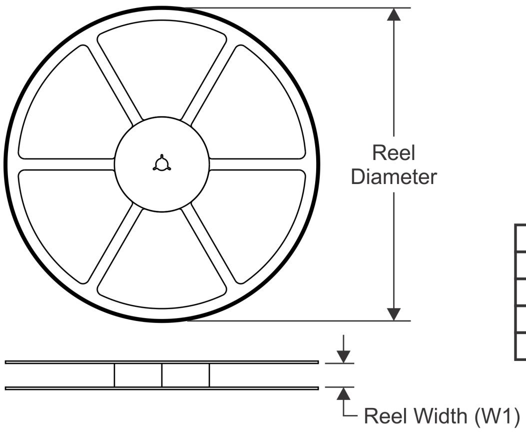
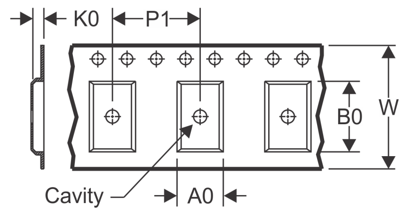
TAPE AND REEL INFORMATION

REEL DIMENSIONS

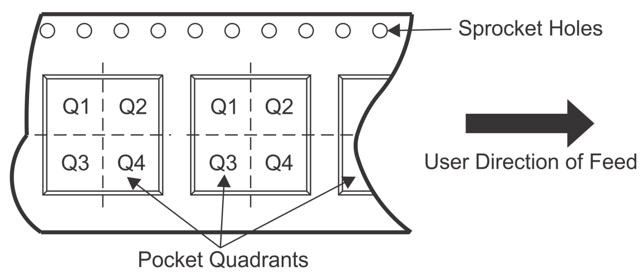


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

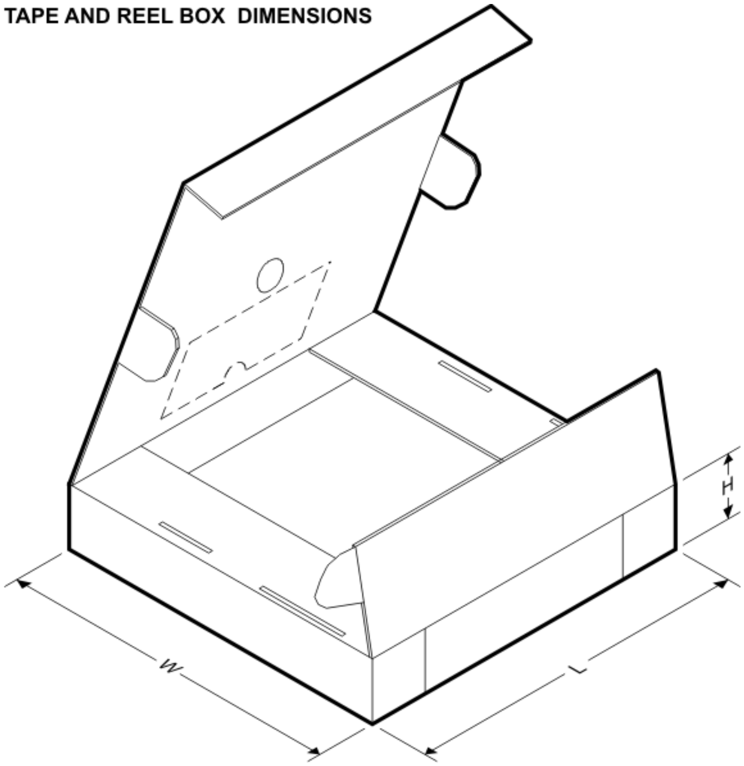
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK03806BISQ/NOPB	WQFN	NKD	64	1000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
LMK03806BISQE/NOPB	WQFN	NKD	64	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
LMK03806BISQX/NOPB	WQFN	NKD	64	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

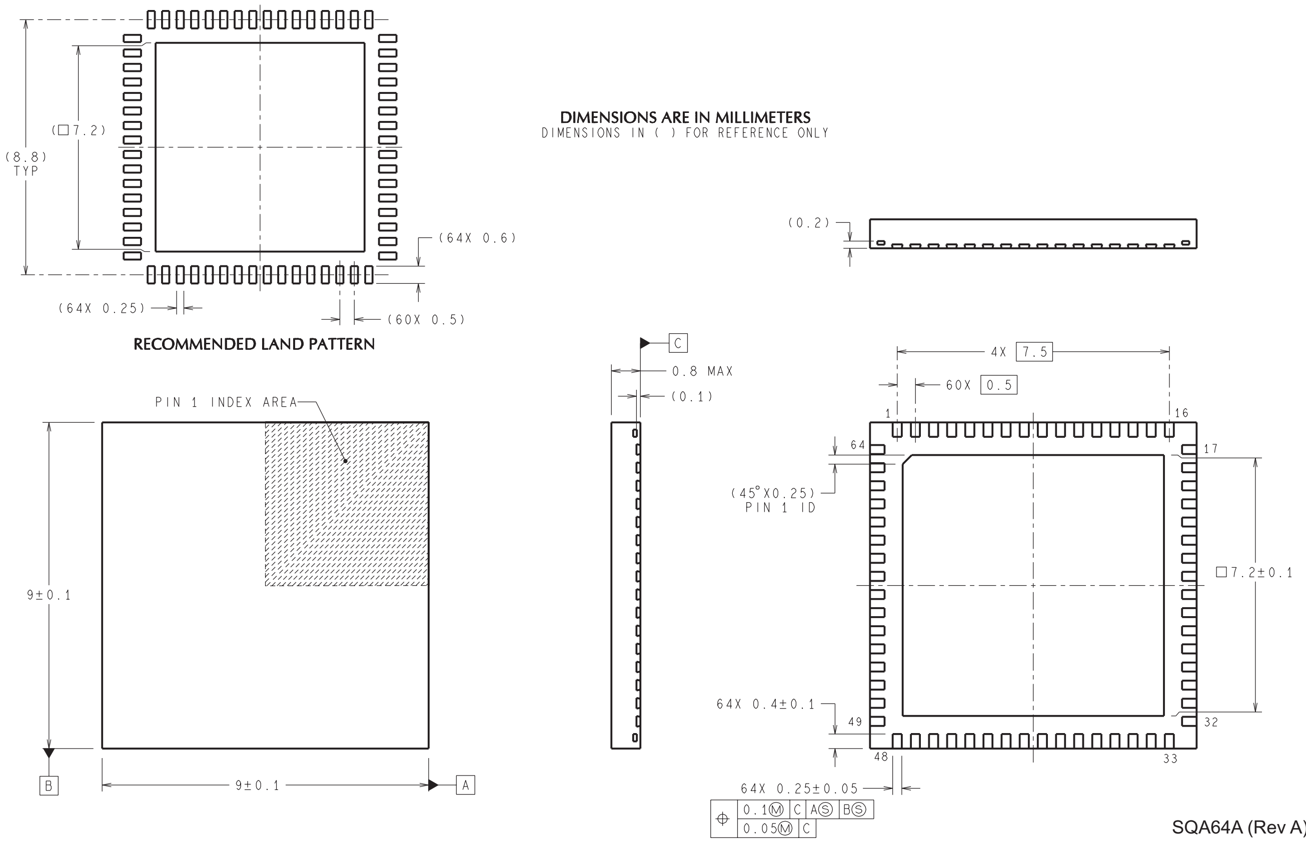
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK03806BISQ/NOPB	WQFN	NKD	64	1000	367.0	367.0	38.0
LMK03806BISQE/NOPB	WQFN	NKD	64	250	213.0	191.0	55.0
LMK03806BISQX/NOPB	WQFN	NKD	64	2000	367.0	367.0	38.0

NKD0064A



SQA64A (Rev A)

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