LMP2021/LMP2022 Zero Drift, Low Noise, EMI Hardened Amplifiers

Check for Samples: LMP2021, LMP2022

FEATURES

(Typical Values, T_A = 25°C, V_S = 5V)

- **Input Offset Voltage (typical) −0.4 µV**
- **Input Offset Voltage (max) ±5 µV**
- **Input Offset Voltage Drift (typical) -0.004 µV/°C**
- **Input Offset Voltage Drift (max) ±0.02 µV/°C**
- **Input Voltage Noise, A_V = 1000 11 nV/√Hz**
- **Open Loop Gain 160 dB**
- **CMRR 139 dB**
- **PSRR 130 dB**
- **Supply Voltage Range 2.2V to 5.5V**
- **Supply Current (per Amplifier) 1.1 mA**
- **Input Bias Current ±25 pA**
- **GBW 5 MHz**
- **Slew Rate 2.6 V/µs**
- **Operating Temperature Range −40°C to 125°C**
- **5-Pin SOT-23, 8-Pin VSSOP and 8-Pin SOIC Packages**

APPLICATIONS

- **Precision Instrumentation Amplifiers**
- **Battery Powered Instrumentation**
- **Thermocouple Amplifiers**
- **Bridge Amplifiers**

DESCRIPTION

The LMP2021/LMP2022 are single and dual precision operational amplifiers offering ultra low input offset voltage, near zero input offset voltage drift, very low input voltage noise and very high open loop gain. They are part of the LMP™ precision family and are ideal for instrumentation and sensor interfaces.

The LMP2021/LMP2022 have only 0.004 µV/°C of input offset voltage drift, and 0.4 µV of input offset voltage. These attributes provide great precision in high accuracy applications.

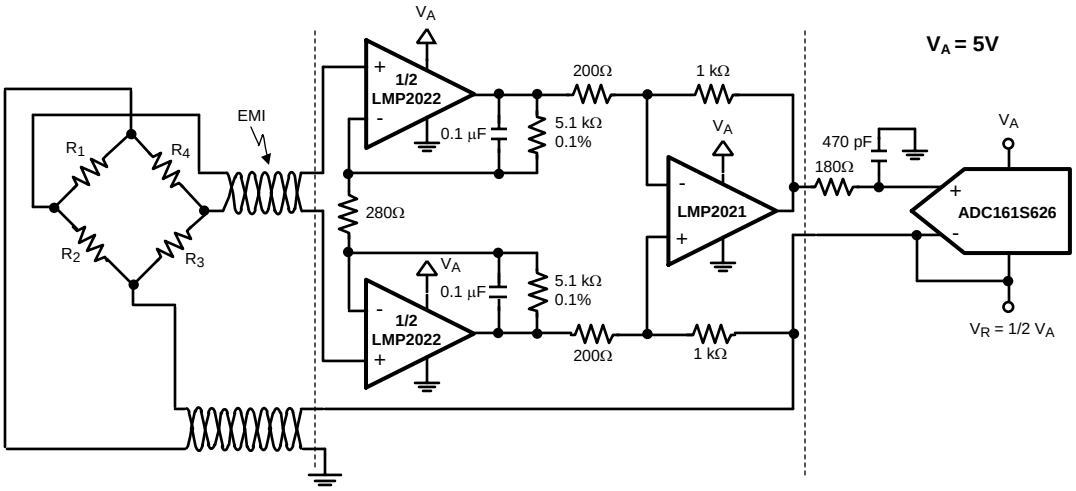
The proprietary continuous correction circuitry guarantees impressive CMRR and PSRR, removes the 1/f noise component, and eliminates the need for calibration in many circuits.

With only 260 nV_{PP} (0.1 Hz to 10 Hz) of input voltage noise and no 1/f noise component, the LMP2021/LMP2022 are suitable for low frequency applications such as industrial precision weigh scales. The low input bias current of 23 pA makes these excellent choices for high source impedance circuits such as non-invasive medical instrumentation as well as test and measurement equipment. The extremely high open loop gain of 160 dB drastically reduces gain error in high gain applications. With ultra precision DC specifications and very low noise, the LMP2021/LMP2022 are ideal for position sensors, bridge sensors, pressure sensors, medical equipment and other high accuracy applications with very low error budgets.

The LMP2021 is offered in 5-Pin SOT-23 and 8-Pin SOIC packages. The LMP2022 is offered in 8-Pin VSSOP and 8-Pin SOIC packages.

TYPICAL APPLICATION

Figure 1. Bridge Amplifier



The LMP2021/LMP2022 support systems with up to 24 bits of accuracy.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	Human Body Model	2000V
	Machine Model	200V
	Charge Device Model	1000V
V_{IN} Differential		$\pm V_S$
Supply Voltage ($V_S = V^+ - V^-$)		6.0V
All Other Pins		V^+ + 0.3V, V^- − 0.3V
Output Short-Circuit Duration to V^+ or V^- (4)		5s
Storage Temperature Range		−65°C to 150°C
Junction Temperature (5)		150°C max
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temperature (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model per MIL-STD-883, Method 3015.7. Machine Model, per JESD22-A115-A. Field-Induced Charge-Device Model, per JESD22-C101-C.
(4) Package power dissipation should be observed.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta J_A$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Temperature Range		−40°C to 125°C
Supply Voltage ($V_S = V^+ – V^–$)		2.2V to 5.5V
Package Thermal Resistance (θ_{JA})	5-Pin SOT-23	164 °C/W
	8-Pin SOIC (LMP2021)	106 °C/W
	8-Pin SOIC (LMP2022)	106 °C/W
	8-Pin VSSOP	217 °C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

2.5V Electrical Characteristics (1)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 2.5V, $V^–$ = 0V, $V_{CM} = V^+/2$, R_L >10 kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage				–0.9	±5 **±10**	µV
TCV_{OS}	Input Offset Voltage Drift (4)				0.001	±0.02	µV/°C
I_B	Input Bias Current				±23	±100 **±300**	pA
I_{OS}	Input Offset Current				±57	±200 **±250**	pA
CMRR	Common Mode Rejection Ratio	−0.2V ≤ V_{CM} ≤ 1.7V 0V ≤ V_{CM} ≤ 1.5V		105 **102**	141		dB
CMVR	Input Common-Mode Voltage Range	Large Signal CMRR ≥ 105 dB Large Signal CMRR ≥ 102 dB		−0.2 **0**		1.7 **1.5**	V
EMIRR	Electro-Magnetic Interference Rejection Ratio (5)	IN+ and IN−	$V_{RF\text{-}PEAK}$ = 100 mV_P (−20 dBV_P) f = 400 MHz		40		dB
			$V_{RF\text{-}PEAK}$ = 100 mV_P (−20 dBV_P) f = 900 MHz		48		
			$V_{RF\text{-}PEAK}$ = 100 mV_P (−20 dBV_P) f = 1800 MHz		67		
			$V_{RF\text{-}PEAK}$ = 100 mV_P (−20 dBV_P) f = 2400 MHz		79		
PSRR	Power Supply Rejection Ratio	2.5V ≤ V^+ ≤ 5.5V, V_{CM} = 0		115 **112**	130		dB
		2.2V ≤ V^+ ≤ 5.5V, V_{CM} = 0		110	130		
A_{VOL}	Large Signal Voltage Gain	R_L = 10 kΩ to $V^+/2$ V_{OUT} = 0.5V to 2V		124 **119**	150		dB
		R_L = 2 kΩ to $V^+/2$ V_{OUT} = 0.5V to 2V		120 **115**	150		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are guaranteed by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) The EMI Rejection Ratio is defined as EMIRR = 20Log ($V_{RF\text{-}PEAK}/\Delta V_{OS}$).

2.5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 2.5V, V^- = 0V, V_{CM} = V^+/2, R_L >10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OUT}	Output Swing High	R_L = 10 kΩ to V^+/2		38	50 **70**	mV from either rail
		R_L = 2 kΩ to V^+/2		62	85 **115**	
	Output Swing Low	R_L = 10 kΩ to V^+/2		30	45 **55**	
		R_L = 2 kΩ to V^+/2		58	75 **95**	
I_{OUT}	Linear Output Current	Sourcing, V_{OUT} = 2V	30	50		mA
		Sinking, V_{OUT} = 0.5V	30	50		
I_S	Supply Current	Per Amplifier		0.95	1.10 **1.37**	mA
SR	Slew Rate (6)	A_V = +1, C_L = 20 pF, R_L = 10 kΩ V_O = 2 V_{PP}		2.5		V/µs
GBW	Gain Bandwidth Product	C_L = 20 pF, R_L = 10 kΩ		5		MHz
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ		10		dB
Φ_M	Phase Margin	C_L = 20 pF, R_L = 10 kΩ		60		deg
C_{IN}	Input Capacitance	Common Mode		12		pF
		Differential Mode		12		
e_n	Input-Referred Voltage Noise Density	f = 0.1 kHz or 10 kHz, A_V = 1000		11		nV/√Hz
		f = 0.1 kHz or 10 kHz, A_V = 100		15		
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz		260		nV_{PP}
		0.01 Hz to 10 Hz		330		
i_n	Input-Referred Current Noise	f = 1 kHz		350		fA/√Hz
t_r	Recovery time	to 0.1%, R_L = 10 kΩ, A_V = −50, V_{OUT} = 1.25 V_{PP} Step, Duration = 50 µs		50		µs
CT	Cross Talk	LMP2022, f = 1 kHz		150		dB

(6) The number specified is the average of rising and falling slew rates and is measured at 90% to 10%.

5V Electrical Characteristics (1)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, R_L > 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage			−0.4	±5 **±10**	µV
TCV_{OS}	Input Offset Voltage Drift (4)			−0.004	±0.02	µV/°C
I_B	Input Bias Current			±25	±100 **±300**	pA
I_{OS}	Input Offset Current			±48	±200 **±250**	pA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are guaranteed by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.

5V Electrical Characteristics [1] (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, R_L > 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min [2]	Typ [3]	Max [2]	Units
CMRR	Common Mode Rejection Ratio	−0.2V ≤ V_{CM} ≤ 4.2V 0V ≤ V_{CM} ≤ 4.0V		120 **115**	139		dB
CMVR	Input Common-Mode Voltage Range	Large Signal CMRR ≥ 120 dB Large Signal CMRR ≥ 115 dB		–0.2 **0**		4.2 **4.0**	V
EMIRR	Electro-Magnetic Interference Rejection Ratio [5]	IN+ and IN−	$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 400 MHz		58		dB
			$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 900 MHz		64		
			$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 1800 MHz		72		
			$V_{RF-PEAK}$ = 100 mV_P (−20 dBV_P) f = 2400 MHz		82		
PSRR	Power Supply Rejection Ratio	2.5V ≤ V^+ ≤ 5.5V, V_{CM} = 0		115 **112**	130		dB
		2.2V ≤ V^+ ≤ 5.5V, V_{CM} = 0		110	130		
A_{VOL}	Large Signal Voltage Gain	R_L = 10 kΩ to V^+/2 V_{OUT} = 0.5V to 4.5V		125 **120**	160		dB
		R_L = 2 kΩ to V^+/2 V_{OUT} = 0.5V to 4.5V		123 **118**	160		
V_{OUT}	Output Swing High	R_L = 10 kΩ to V^+/2			83	135 **170**	mV from either rail
		R_L = 2 kΩ to V^+/2			120	160 **204**	
	Output Swing Low	R_L = 10 kΩ to V^+/2			65	80 **105**	
		R_L = 2 kΩ to V^+/2			103	125 **158**	
I_{OUT}	Linear Output Current	Sourcing, V_{OUT} = 4.5V		30	50		mA
		Sinking, V_{OUT} = 0.5V		30	50		
I_S	Supply Current	Per Amplifier			1.1	1.25 **1.57**	mA
SR	Slew Rate [6]	A_V = +1, C_L = 20 pF, R_L = 10 kΩ V_O = 2 V_{PP}			2.6		V/µs
GBW	Gain Bandwidth Product	C_L = 20 pF, R_L = 10 kΩ			5		MHz
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ			10		dB
Φ_M	Phase Margin	C_L = 20 pF, R_L = 10 kΩ			60		deg
C_{IN}	Input Capacitance	Common Mode			12		pF
		Differential Mode			12		
e_n	Input-Referred Voltage Noise Density	f = 0.1 kHz or 10 kHz, A_V= 1000			11		nV/√Hz
		f = 0.1 kHz or 10 kHz, A_V= 100			15		
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz Noise			260		nV_{PP}
		0.01 Hz to 10 Hz Noise			330		
i_n	Input-Referred Current Noise	f = 1 kHz			350		fA/√Hz
t_r	Input Overload Recovery time	to 0.1%, R_L = 10 kΩ, A_V = −50, V_{OUT} = 2.5 V_{PP} Step, Duration = 50 µs			50		µs
CT	Cross Talk	LMP2022, f = 1 kHz			150		dB

(5) The EMI Rejection Ratio is defined as EMIRR = 20Log ($V_{RF-PEAK}/\Delta V_{OS}$).
(6) The number specified is the average of rising and falling slew rates and is measured at 90% to 10%.

Connection Diagrams

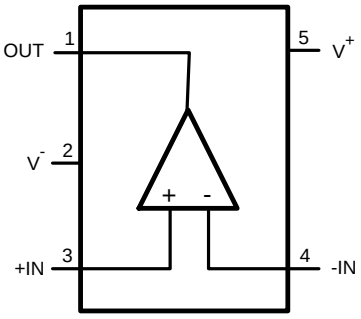


Figure 2. 5-Pin SOT-23
Top View

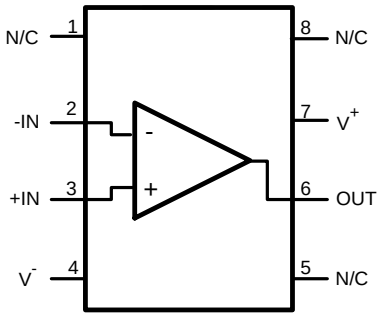


Figure 3. 8-Pin SOIC (LMP2021)
Top View

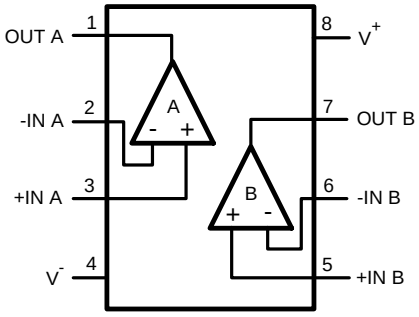


Figure 4. 8-Pin SOIC/VSSOP
(LMP2022)

Typical Performance Characteristics

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – V^-, V_S= 5V, V_{CM} = V_S/2.

Offset Voltage Distribution

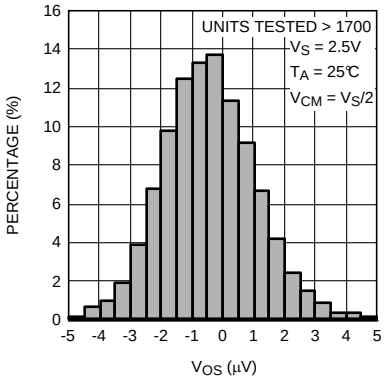


Figure 5.

TCV_{OS} Distribution

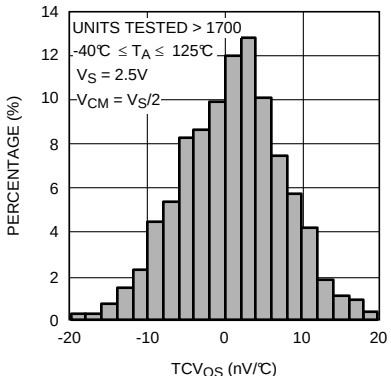


Figure 6.

Offset Voltage Distribution

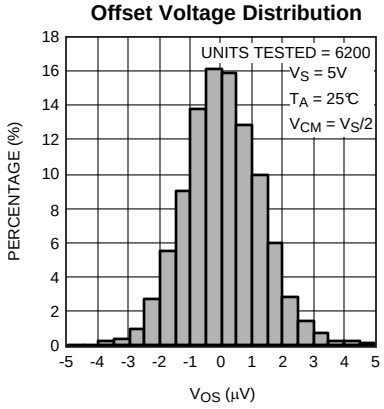


Figure 7.

TCV_{OS} Distribution

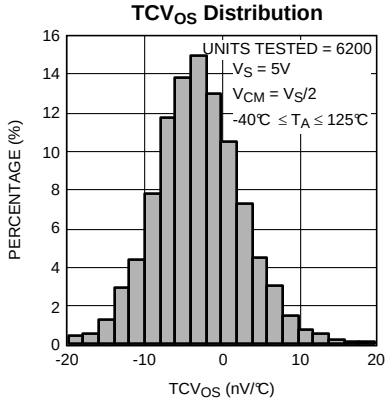


Figure 8.

Offset Voltage vs. Supply Voltage

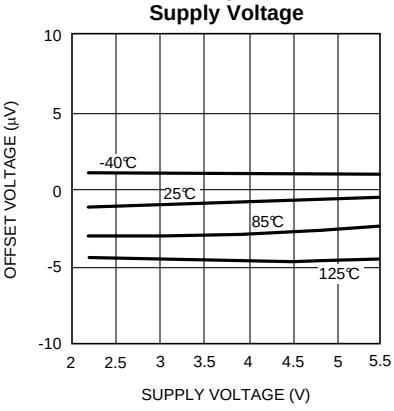


Figure 9.

PSRR vs. Frequency

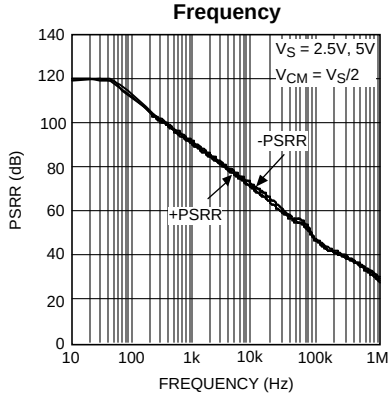


Figure 10.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – V^-, V_S= 5V, V_{CM} = V_S/2.

Input Bias Current vs. V_{CM}

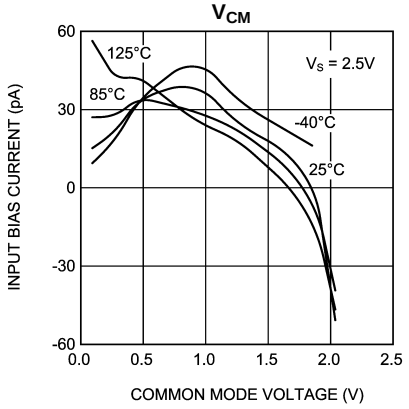


Figure 11.

Input Bias Current vs. V_{CM}

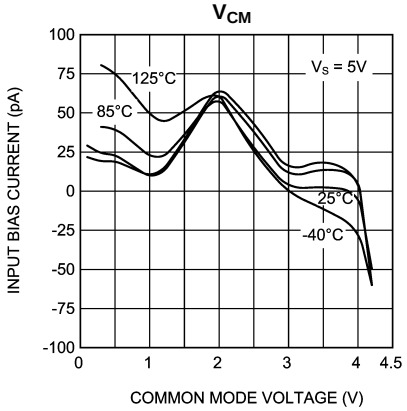


Figure 12.

Offset Voltage vs. V_{CM}

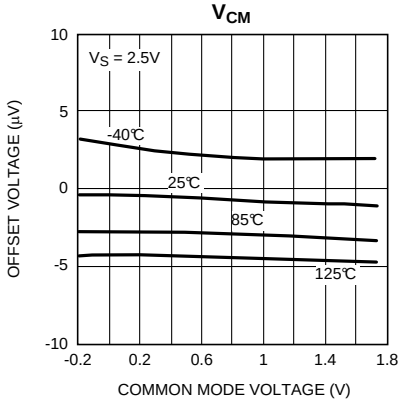


Figure 13.

Offset Voltage vs. V_{CM}

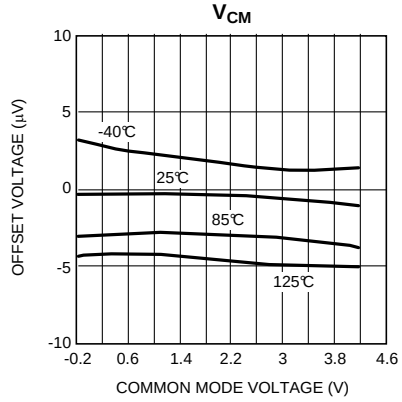


Figure 14.

Supply Current vs. Supply Voltage (Per Amplifier)

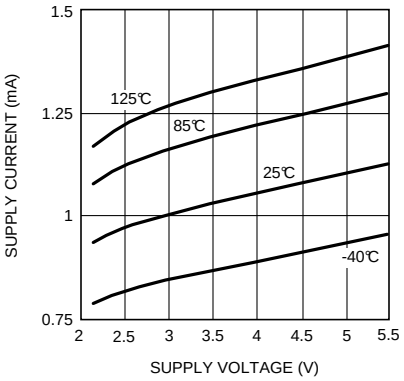


Figure 15.

Input Voltage Noise vs. Frequency

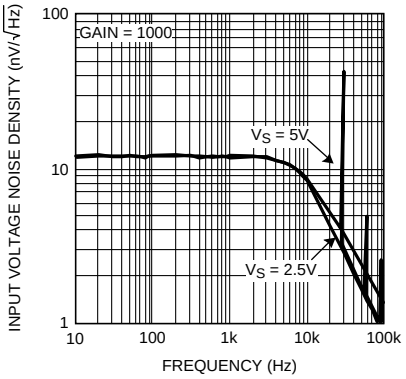


Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – V^-, V_S= 5V, V_{CM} = V_S/2.

Open Loop Frequency Response

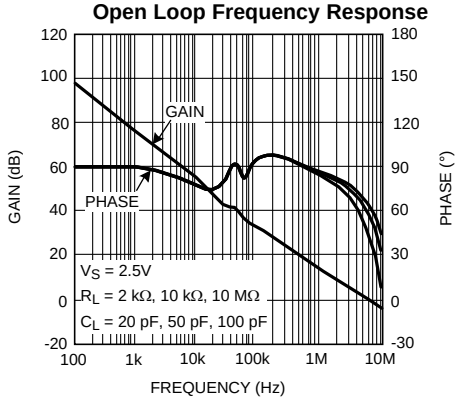


Figure 17.

Open Loop Frequency Response

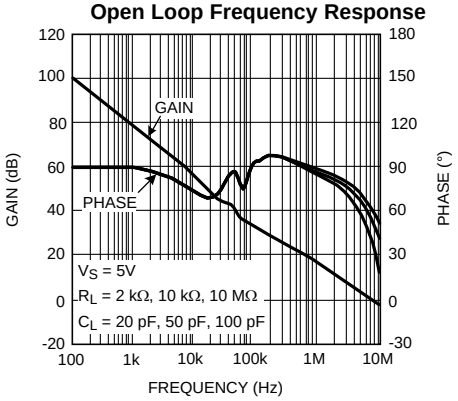


Figure 18.

Open Loop Frequency Response Over Temperature

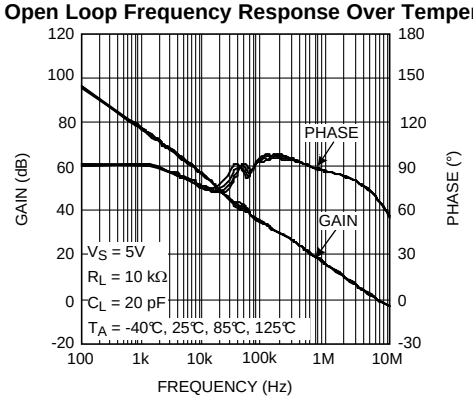


Figure 19.

EMIRR vs. Frequency

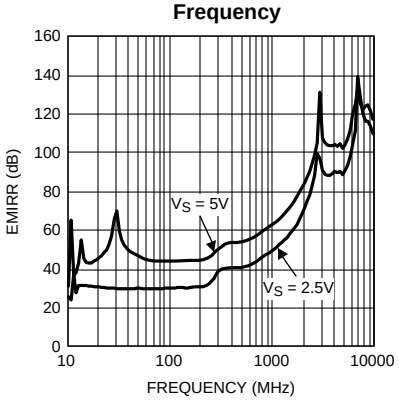


Figure 20.

EMIRR vs. Input Power

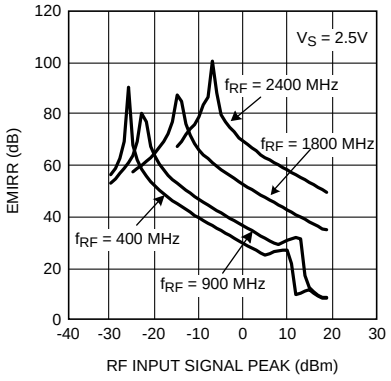


Figure 21.

EMIRR vs. Input Power

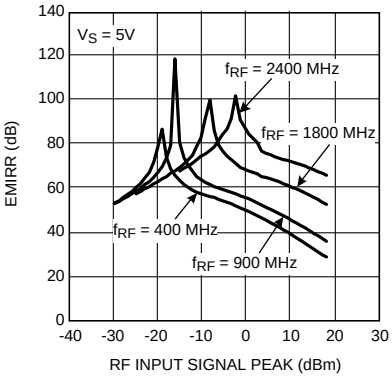


Figure 22.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – V^-, V_S= 5V, V_{CM} = V_S/2.

Time Domain Input Voltage Noise

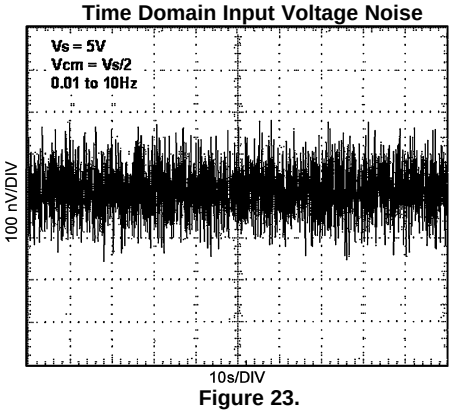


Figure 23.

Time Domain Input Voltage Noise

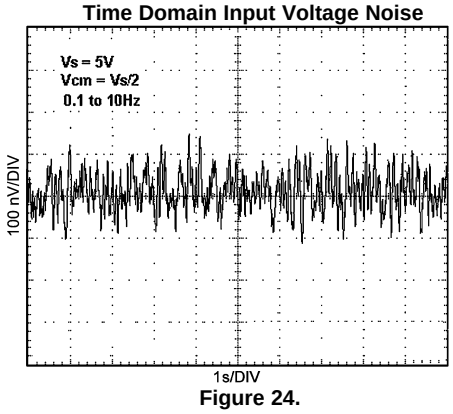


Figure 24.

CMRR vs. Frequency

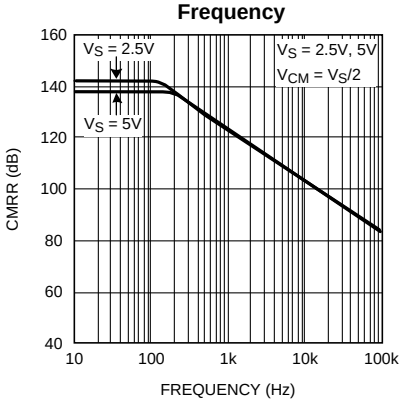


Figure 25.

Slew Rate vs. Supply Voltage

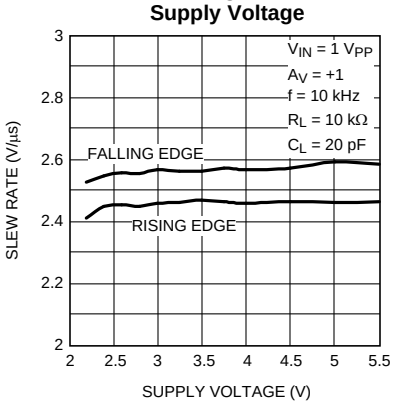


Figure 26.

Output Swing High vs. Supply Voltage

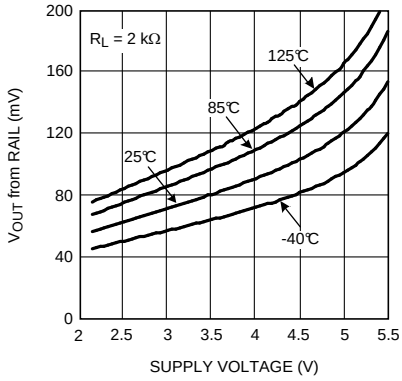


Figure 27.

Output Swing Low vs. Supply Voltage

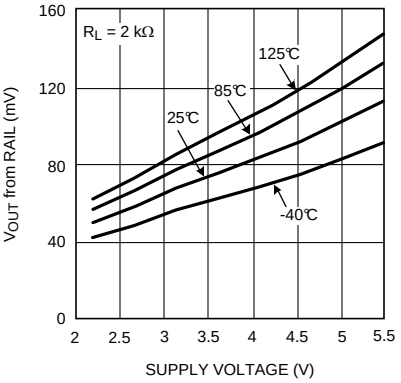


Figure 28.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – V^-, V_S= 5V, V_{CM} = V_S/2.

Output Swing High vs. Supply Voltage

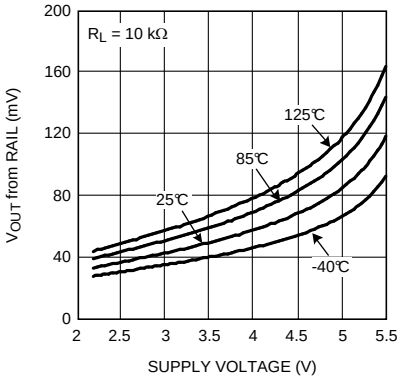


Figure 29.

Output Swing Low vs. Supply Voltage

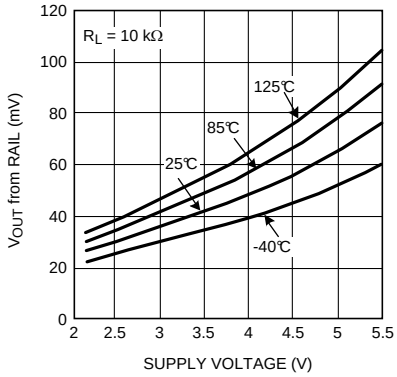


Figure 30.

Overload Recovery Time

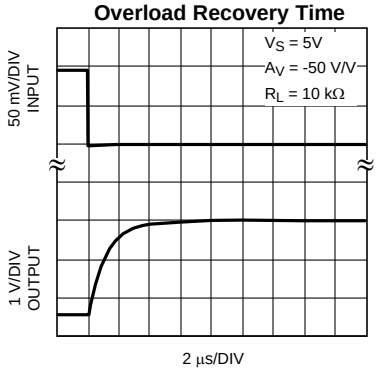


Figure 31.

Overload Recovery Time

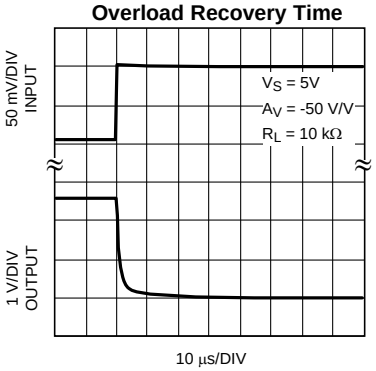


Figure 32.

Large Signal Step Response

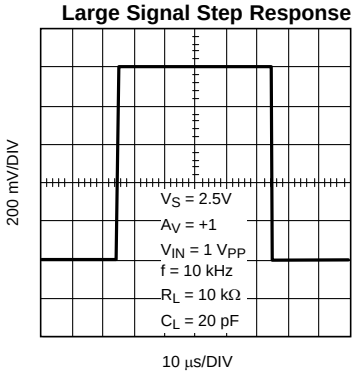


Figure 33.

Small Signal Step Response

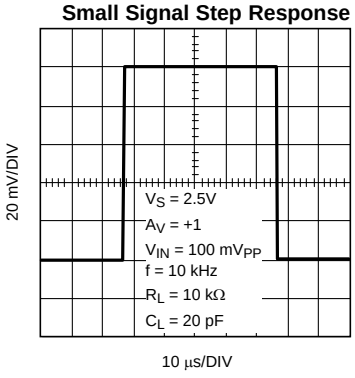


Figure 34.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, R_L > 10 kΩ, V_S= V^+ – V^-, V_S= 5V, V_{CM} = V_S/2.

Large Signal Step Response

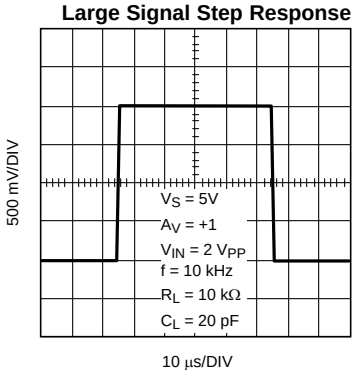


Figure 35.

Small Signal Step Response

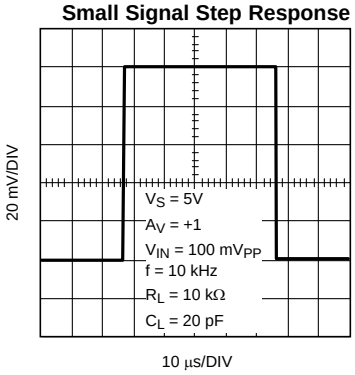


Figure 36.

Output Voltage vs. Output Current

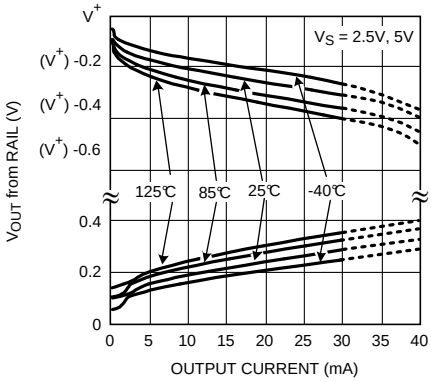


Figure 37.

Cross Talk Rejection Ratio vs. Frequency (LMP2022)

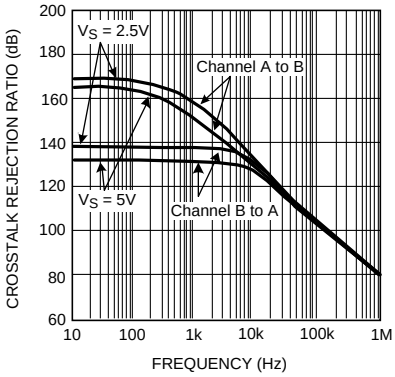


Figure 38.

APPLICATION INFORMATION

LMP2021/LMP2022

The LMP2021/LMP2022 are single and dual precision operational amplifiers with ultra low offset voltage, ultra low offset voltage drift, and very low input voltage noise with no 1/f and extended supply voltage range. The LMP2021/LMP2022 offer on chip EMI suppression circuitry which greatly enhances the performance of these precision amplifiers in the presence of radio frequency signals and other disturbances.

The LMP2021/LMP2022 utilize proprietary techniques to measure and continuously correct the input offset error voltage. The LMP2021/LMP2022 have a DC input offset voltage with a maximum value of ±5 µV and an input offset voltage drift maximum value of 0.02 µV/°C. The input voltage noise of the LMP2021/LMP2022 is less than 11 nV/√Hz at a voltage gain of 1000 V/V and has no flicker noise component. This makes the LMP2021/LMP2022 ideal for high accuracy, low frequency applications where lots of amplification is needed and the input signal has a very small amplitude.

The proprietary input offset correction circuitry enables the LMP2021/LMP2022 to have superior CMRR and PSRR performances. The combination of an open loop voltage gain of 160 dB, CMRR of 142 dB, PSRR of 130 dB, along with the ultra low input offset voltage of only −0.4 µV, input offset voltage drift of only −0.004 µV/°C, and input voltage noise of only 260 nV_{PP} at 0.1 Hz to 10 Hz make the LMP2021/LMP2022 great choices for high gain transducer amplifiers, ADC buffer amplifiers, DAC I-V conversion, and other applications requiring precision and long-term stability. Other features are rail-to-rail output, low supply current of 1.1 mA per amplifier, and a gain-bandwidth product of 5 MHz.

The LMP2021/LMP2022 have an extended supply voltage range of 2.2V to 5.5V, making them ideal for battery operated portable applications. The LMP2021 is offered in 5-pin SOT-23 and 8-pin SOIC packages. The LMP2022 is offered in 8-pin VSSOP and 8-Pin SOIC packages.

EMI SUPPRESSION

The near-ubiquity of cellular, bluetooth, and Wi-Fi signals and the rapid rise of sensing systems incorporating wireless radios make electromagnetic interference (EMI) an evermore important design consideration for precision signal paths. Though RF signals lie outside the op amp band, RF carrier switching can modulate the DC offset of the op amp. Also some common RF modulation schemes can induce down-converted components. The added DC offset and the induced signals are amplified with the signal of interest and thus corrupt the measurement. The LMP2021/LMP2022 use on chip filters to reject these unwanted RF signals at the inputs and power supply pins; thereby preserving the integrity of the precision signal path.

Twisted pair cabling and the active front-end's common-mode rejection provide immunity against low frequency noise (i.e. 60 Hz or 50 Hz mains) but are ineffective against RF interference. Figure 50 displays this. Even a few centimeters of PCB trace and wiring for sensors located close to the amplifier can pick up significant 1 GHz RF. The integrated EMI filters of LMP2021/LMP2022 reduce or eliminate external shielding and filtering requirements, thereby increasing system robustness. A larger EMIRR means more rejection of the RF interference. For more information on EMIRR, please refer to AN-1698.

INPUT VOLTAGE NOISE

The input voltage noise density of the LMP2021/LMP2022 has no 1/f corner, and its value depends on the feedback network used. This feature of the LMP2021/LMP2022 differentiates this family from other products currently available from other vendors. In particular, the input voltage noise density decreases as the closed loop voltage gain of the LMP2021/LMP2022 increases. The input voltage noise of the LMP2021/LMP2022 is less than 11 nV/√Hz when the closed loop voltage gain of the op amp is 1000. Higher voltage gains are required for smaller input signals. When the input signal is smaller, a lower input voltage noise is quite advantageous and increases the signal to noise ratio.

Figure 39 shows the input voltage noise of the LMP2021/LMP2022 as the closed loop gain increases.

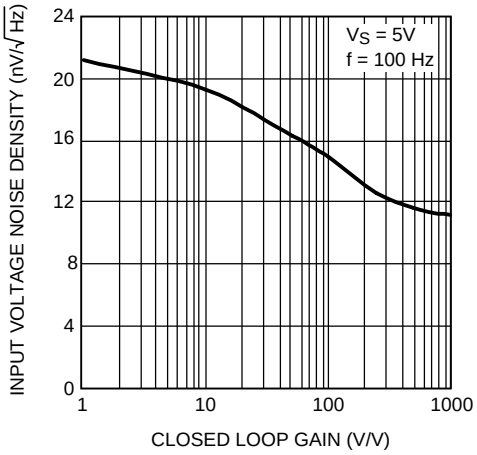


Figure 39. Input Voltage Noise Density decreases with Gain

Figure 40 shows the input voltage noise density does not have the 1/f component.

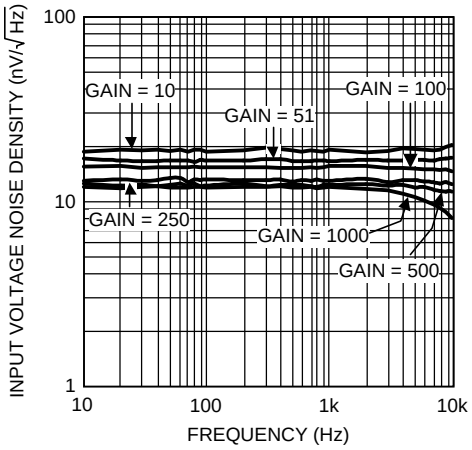


Figure 40. Input Voltage Noise Density with no 1/f

With smaller and smaller input signals and high precision applications with lower error budget, the reduced input voltage noise and no 1/f noise allow more flexibility in circuit design.

ACHIEVING LOWER NOISE WITH FILTERING

The low input voltage noise of the LMP2021/LMP2022, and no 1/f noise make these suitable for many applications with noise sensitive designs. Simple filtering can be done on the LMP2021/LMP2022 to remove high frequency noise. Figure 41 shows a simple circuit that achieves this.

In Figure 41 C_F and the corner frequency of the filter resulting from C_F and R_F will reduce the total noise.

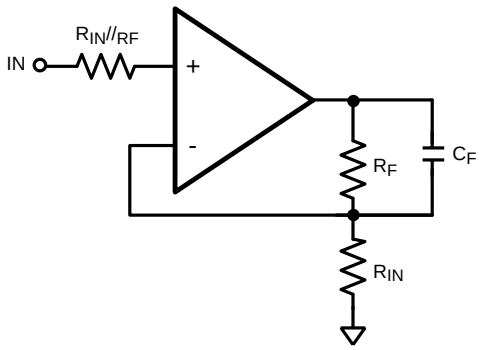


Figure 41. Noise Reducing Filter for Lower Gains

In order to achieve lower noise floors for even more noise stringent applications, a simple filter can be added to the op amp's output after the amplification stage. Figure 42 shows the schematic of a simple circuit which achieves this objective. Low noise amplifiers such as the LMV771 can be used to create a single pole low pass filter on the output of the LMP2021/LMP2022. The noise performance of the filtering amplifier, LMV771 in this circuit, will not be dominant as the input signal on LMP2021/LMP2022 has already been significantly gained up and as a result the effect of the input voltage noise of the LMV771 is effectively not noticeable.

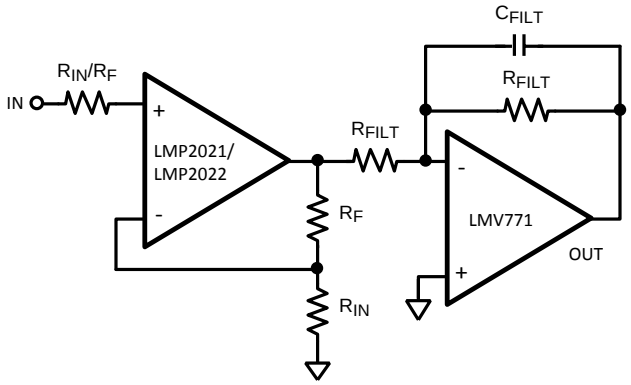


Figure 42. Enhanced Filter to Further Reduce Noise at Higher Gains

Using the circuit in Figure 42 has the advantage of removing the non-linear filter bandwidth dependency which is seen when the circuit in Figure 41 is used. The difference in noise performance of the circuits in Figure 41, 8 becomes apparent only at higher gains. At voltage gains of 10 V/V or less, there is no difference between the noise performance of the two circuits.

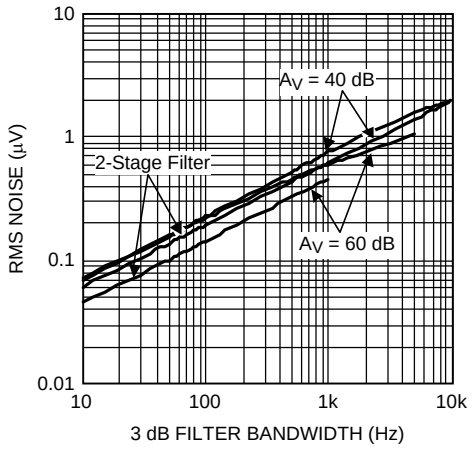


Figure 43. RMS Input Referred Noise vs. Frequency

Figure 43 shows the total input referred noise vs. 3 dB corner of both filters of Figure 41 and Figure 42 at gains of 100V/V and 1000V/V. For these measurements and using Figure 41's circuit, R_F = 49.7 kΩ and R_{IN} = 497Ω. Value of C_F has been changed to achieve the desired 3 dB filter corner frequency. In the case of Figure 42's circuit, R_F = 49.7 kΩ and R_{IN} = 497Ω, R_{FILT} = 49.7 kΩ, and C_{FILT} has been changed to achieve the desired 3 dB filter corner frequency. Figure 43 compares the RMS noise of these two circuits. As Figure 43 shows, the RMS noise measured the circuit in Figure 42 has lower values and also depicts a more linear shape.

DIGITAL ACQUISITION SYSTEMS

High resolution ADC's with 16-bits to 24-bits of resolution can be limited by the noise of the amplifier driving them. The circuit configuration, the value of the resistors used and the source impedance seen by the amplifier can affect the noise of the amplifier. The total noise at the output of the amplifier can be dominated by one of several sources of noises such as: white noise or broad band noise, 1/f noise, thermal noise, and current noise. In low frequency applications such as medical instrumentation, the source impedance is generally low enough that the current noise coupled into it does not impact the total noise significantly. However, as the 1/f or flicker noise is paramount to many application, the use of an auto correcting stabilized amplifier like the LMP2021/LMP2022 reduces the total noise.

Table 1: RMS Input Noise Performance summarizes the input and output referred RMS noise values for the LMP2021/LMP2022 compared to that of Competitor A. As described in previous sections, the outstanding noise performance of the LMP2021/LMP2022 can be even further improved by adding a simple low pass filter following the amplification stage.

The use of an additional filter, as shown in Figure 42 benefits applications with higher gain. For this reason, at a gain of 10, only the results of circuit in Figure 41 are shown. The RMS input noise of the LMP2021/LMP2022 are compared with Competitor A's input noise performance. Competitor A's RMS input noise behaves the same with or without an additional filter.

Table 1. RMS Input Noise Performance

Amplifier Gain (V/V)	System Bandwidth Requirement (Hz)	RMS Input Noise (nV)		
		LMP2021/LMP2022		Competitor A
		Figure 41 Circuit	Figure 42 Circuit	Figure 42 Figure 41 Circuit
10	100	229	See(1)	300
	1000	763	See(1)	1030
100	100	229	196	300
	1000	763	621	1030
1000	10	71	46	95
	100	158	146	300
	1000	608	462	1030

(1) No significant difference in Noise measurements at A_V = 10V/V

INPUT BIAS CURRENT

The bias current of the LMP2021/LMP2022 behaves differently than a conventional amplifier due to the dynamic transient currents created on the input of an auto-zero circuit. The input bias current is affected by the charge and discharge current of the input auto-zero circuit. The amount of current sunk or sourced from that stage is dependent on the combination of input impedance (resistance and capacitance), as well as the balance and matching of these impedances across the two inputs. This current, integrated in the auto-zero circuit, causes a shift in the apparent "bias current". Because of this, there is an apparent "bias current vs. input impedance" interaction. In the LMP2021/LMP2022 for an input resistive impedance of 1 GΩ, the shift in input bias current can be up to 40 pA. This input bias shift is caused by varying the input's capacitive impedance. Since the input bias current is dependent on the input impedance, it is difficult to estimate what the actual bias current is without knowing the end circuit and associated capacitive strays.

Figure 44 shows the input bias current of the LMP2021/LMP2022 and that of another commercially available amplifier from a competitor. As it can be seen, the shift in LMP2021/LMP2022 bias current is much lower than that of other chopper style or auto zero amplifiers available from other vendors.

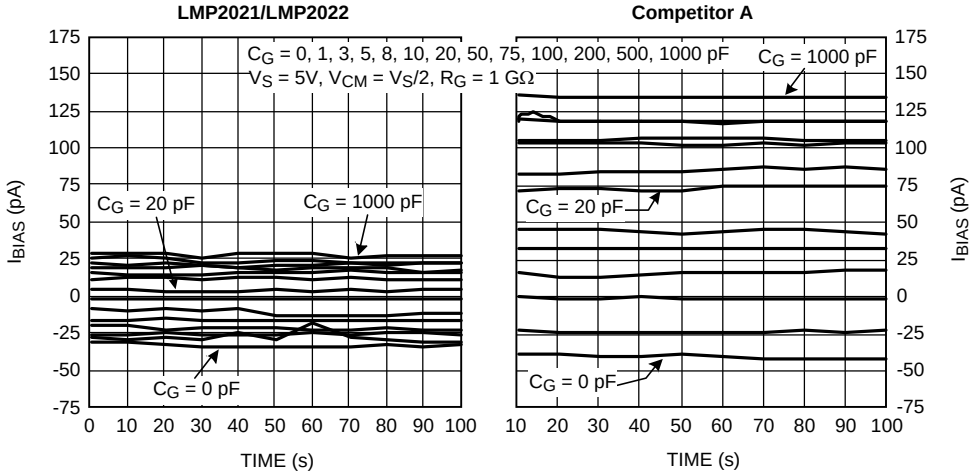


Figure 44. Input Bias Current of LMP2021/LMP2022 is lower than Competitor A

LOWERING THE INPUT BIAS CURRENT

As mentioned in the INPUT BIAS CURRENT section, the input bias current of an auto zero amplifier such as the LMP2021/LMP2022 varies with input impedance and feedback impedance. Once the value of a certain input resistance, i.e. sensor resistance, is known, it is possible to optimize the input bias current for this fixed input resistance by choosing the capacitance value that minimizes that current. Figure 45 shows the input bias current vs. input impedance of the LMP2021/LMP2022. The value of R_G or input resistance in this test is 1 GΩ. When

this value of input resistance is used, and when a parallel capacitance of 22 pF is placed on the circuit, the resulting input bias current is nearly 0 pA. Figure 45 can be used to extrapolate capacitor values for other sensor resistances. For this purpose, the total impedance seen by the input of the LMP2021/LMP2022 needs to be calculated based on Figure 45. By knowing the value of R_G, one can calculate the corresponding C_G which minimizes the non-inverting input bias current, positive bias current, value.

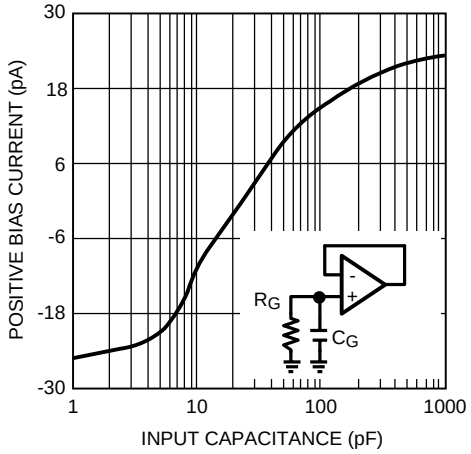


Figure 45. Input Bias Current vs. C_G with R_G = 1 GΩ

In a typical I-V converter, the output voltage will be the sum of DC offset plus bias current and the applied signal through the feedback resistor. In a conventional input stage, the inverting input's capacitance has very little effect on the circuit. This effect is generally on settling time and the dielectric soakage time and can be ignored. In auto zero amplifiers, the input capacitance effect will add another term to the output. This additional term means that the baseline reading on the output will be dependent on the input capacitance. The term input capacitance for this purpose includes circuit strays and any input cable capacitances. There is a slight variation in the capacitive offset as the duty cycle and amplitude of the pulses vary from part to part, depending on the correction at the time. The lowest input current will be obtained when the impedances, both resistive and capacitive, are matched between the inputs. By balancing the input capacitances, the effect can be minimized. A simple way to balance the input impedance is adding a capacitance in parallel to the feedback resistance. The addition of this feedback capacitance reduces the bias current and increases the stability of the operational amplifier. Figure 46 shows the input bias current of the LMP2021/LMP2022 when R_F is set to 1 GΩ. As it can be seen from Figure 46, choosing the optimum value of C_F will help reducing the input bias current.

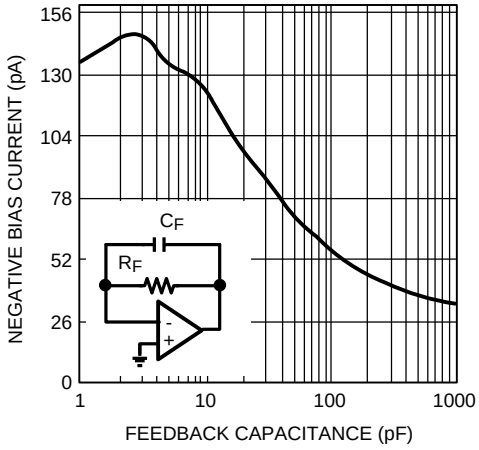


Figure 46. Input Bias Current vs. C_F with R_F = 1 GΩ

The effect of bias current on a circuit can be estimated with the following:

$$A_V * I_{BIAS+} * Z_S - I_{BIAS-} * Z_F \quad (1)$$

Where A_V is the closed loop gain of the system and I_{BIAS+} and I_{BIAS-} denote the positive and negative bias current, respectively. It is common to show the average of these bias currents in product datasheets. If I_{BIAS+} and I_{BIAS-} are not individually specified, use the I_{BIAS} value provided in datasheet graphs or tables for this calculation.

For the application circuit shown in Figure 50, the LMP2022 amplifiers each have a gain of 18. With a sensor impedance of 500Ω for the bridge, and using the above equation, the total error due to the bias current on the outputs of the LMP2022 amplifier will be less than 200 nV.

SENSOR IMPEDANCE

The sensor resistance, or the resistance connected to the inputs of the LMP2021/LMP2022, contributes to the total impedance seen by the auto correcting input stage.

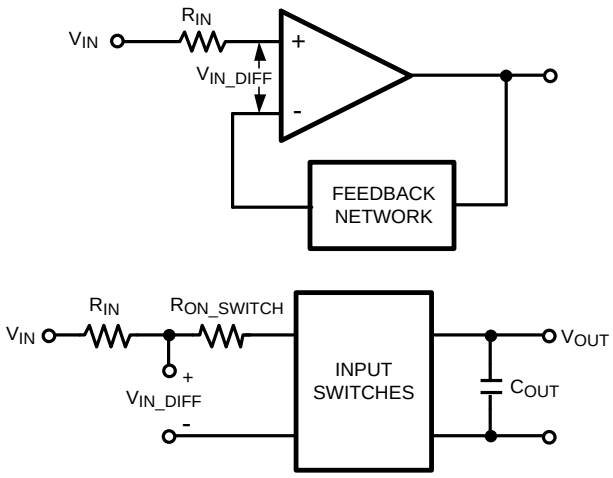
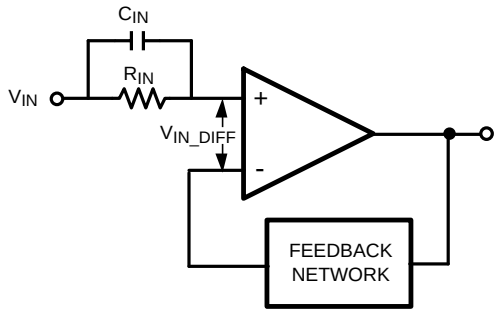


Figure 47. Auto Correcting Input Stage Model

As shown in Figure 47, the sum of R_{IN} and $R_{ON\text{-}SWITCH}$ will form a low pass filter with C_{OUT} during correction cycles. As R_{IN} increases, the time constant of this filter increases, resulting in a slower output signal which could have the effect of reducing the open loop gain, A_{VOL}, of the LMP2021/LMP2022. In order to prevent this reduction in A_{VOL} in presence of high impedance sensors or other high resistances connected to the input of the LMP2021/LMP2022, a capacitor can be placed in parallel to this input resistance. This is shown in Figure 48



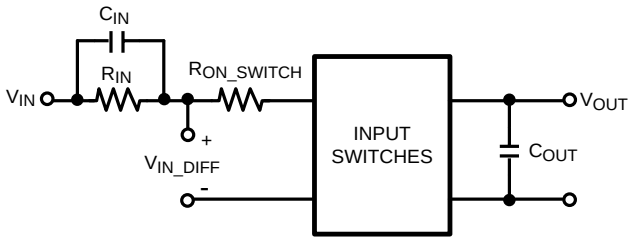


Figure 48. Sensor Impedance with Parallel Capacitance

C_{IN} in Figure 48 adds a zero to the low pass filter and hence eliminating the reduction in A_{VOL} of the LMP2021/LMP2022. An alternative circuit to achieve this is shown in Figure 49.

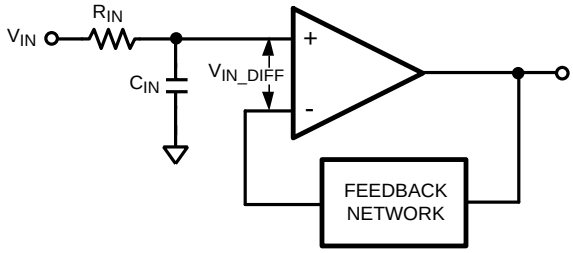


Figure 49. Alternative Sensor Impedance Circuit

TRANSIENT RESPONSE TO FAST INPUTS

On chip continuous auto zero correction circuitry eliminates the 1/f noise and significantly reduces the offset voltage and offset voltage drift; all of which are very low frequency events. For slow changing sensor signals this correction is transparent. For excitations which may otherwise cause the output to swing faster than 40 mV/µs, there are additional considerations which can be viewed two perspectives: for sine waves and for steps.

For sinusoidal inputs, when the output is swinging rail-to-rail on ±2.5V supplies, the auto zero circuitry will introduce distortions above 2.55 kHz. For smaller output swings, higher frequencies can be amplified without the auto zero slew limitation as shown in table below. Signals above 20 kHz, are not affected, though normally, closed loop bandwidth should be kept below 20 kHz so as to avoid aliasing from the auto zero circuit.

$V_{OUT-PEAK}$ (V)	$f_{MAX-SINE\ WAVE}$ (kHz)
0.32	20
1	6.3
2.5	2.5

For step-like inputs, such as those arising from disturbances to a sensing system, the auto zero slew rate limitation manifests itself as an extended ramping and settling time, lasting ~100 µs.

DIFFERENTIAL BRIDGE SENSOR

Bridge sensors are used in a variety of applications such as pressure sensors and weigh scales. Bridge sensors typically have a very small differential output signal. This very small signal needs to be accurately amplified before it can be fed into an ADC. As discussed in the previous sections, the accuracy of the op amp used as the ADC driver is essential to maintaining total system accuracy.

The high DC performance of the LMP2021/LMP2022 make these amplifiers ideal choices for use with a bridge sensor. The LMP2021/LMP2022 have very low input offset voltage and very low input offset voltage drift. The open loop gain of the LMP2021/LMP2022 is 160 dB.

The on chip EMI rejection filters available on the LMP2021/LMP2022 help remove the EMI interference introduced to the signal and hence improve the overall system performance.

The circuit in Figure 50 shows a signal path solution for a typical bridge sensor using the LMP2021/LMP2022. Bridge sensors are created by replacing at least one, and up to all four, of the resistors in a typical bridge with a sensor whose resistance varies in response to an external stimulus. Using four sensors has the advantage of increasing output dynamic range. Typical output voltage of one resistive pressure sensor is 2 mV per 1V of bridge excitation voltage. Using four sensors, the output of the bridge is 8 mV per 1V. The bridge voltage is this system is chosen to be 1/2 of the analog supply voltage and equal to the reference voltage of the ADC161S626, 2.5V. This excitation voltage results in 2.5V * 8 mV = 20 mV of differential output signal on the bridge. This 20 mV signal must be accurately amplified by the amplifier to best match the dynamic input range of the ADC. This is done by using one LMP2022 and one LMP2021 in front of the ADC161S626. The gaining of this 20 mV signal is achieved in 2 stages and through an instrumentation amplifier. The LMP2022 in Figure 50 amplifies each side of the differential output of the bridge sensor by a gain 18. Bridge sensor measurements are usually done up to 10s of Hz. Placing a 300 Hz filter on the LMP2022 helps removing the higher frequency noise from this circuit. This filter is created by placing two capacitors in the feedback path of the LMP2022 amplifiers. Using the LMP2022 with a gain of 18 reduces the input referred voltage noise of the op amps and the system as a result. Also, this gain allows direct filtering of the signal on the LMP2022 without compromising noise performance. The differential output of the two amplifiers in the LMP2022 are then fed into a LMP2021 configured as a difference amplifier. This stage has a gain of 5, with a total system having a gain of (18*2+1)*5 = 185. The LMP2021 has an outstanding CMRR value of 139. This impressive CMRR improves system performance by removing the common mode signal introduced by the bridge. With an overall gain of 185, the 20 mV differential input signal is gained up to 3.7V. This utilizes the amplifiers output swing as well as the ADC's input dynamic range.

This amplified signal is then fed into the ADC161S626. The ADC161S626 is a 16-bit, 50 kSPS to 250 kSPS 5V ADC. In order to utilize the maximum number of bits of the ADC161S626 in this configuration, a 2.5V reference voltage is used. This 2.5V reference is also used to power the bridge sensor and the inverting input of the ADC. Using the same voltage source for these three points helps reducing the total system error by eliminating error due to source variations.

With this system, the output signal of the bridge sensor which can be up to 20 mV is accurately gained to the full scale of the ADC and then digitized for further processing. The LMP2021/LMP2022 introduced minimal error to the system and improved the signal quality by removing common model signals and high frequency noise.

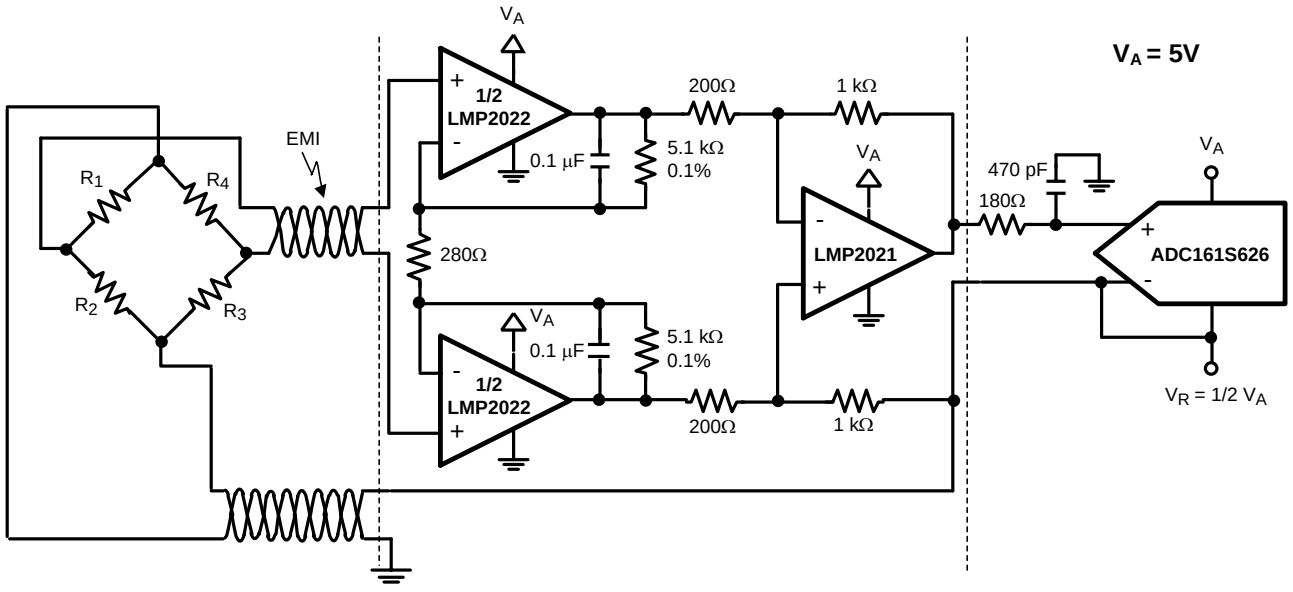


Figure 50. LMP2021/LMP2022 used with ADC161S626

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP2021MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP20 21MA	Samples
LMP2021MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP20 21MA	Samples
LMP2021MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AF5A	Samples
LMP2021MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AF5A	Samples
LMP2021MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AF5A	Samples
LMP2022MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP20 22MA	Samples
LMP2022MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP20 22MA	Samples
LMP2022MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV5A	Samples
LMP2022MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV5A	Samples
LMP2022MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV5A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

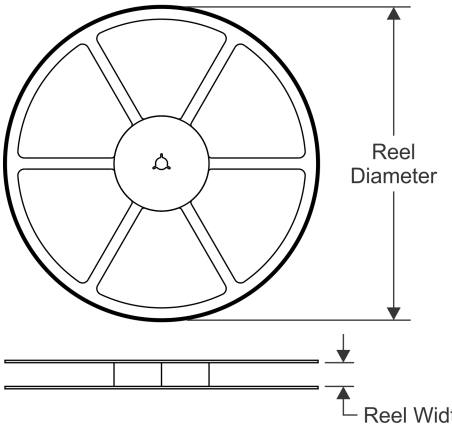
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

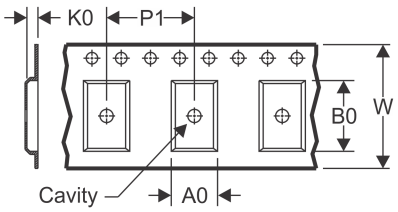
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

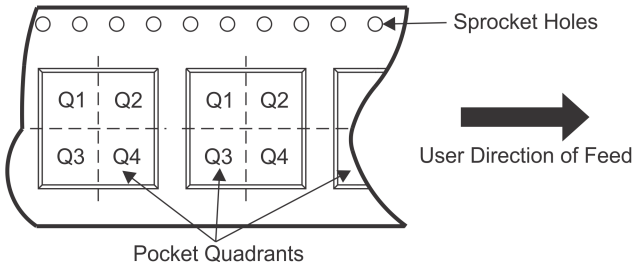


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

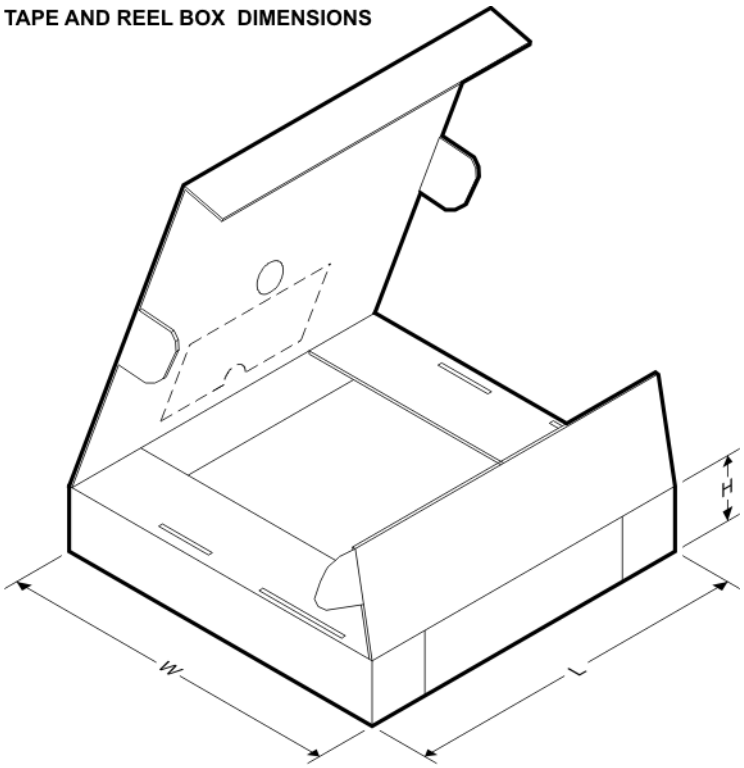
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP2021MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP2021MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2021MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2021MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2022MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP2022MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP2022MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP2022MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

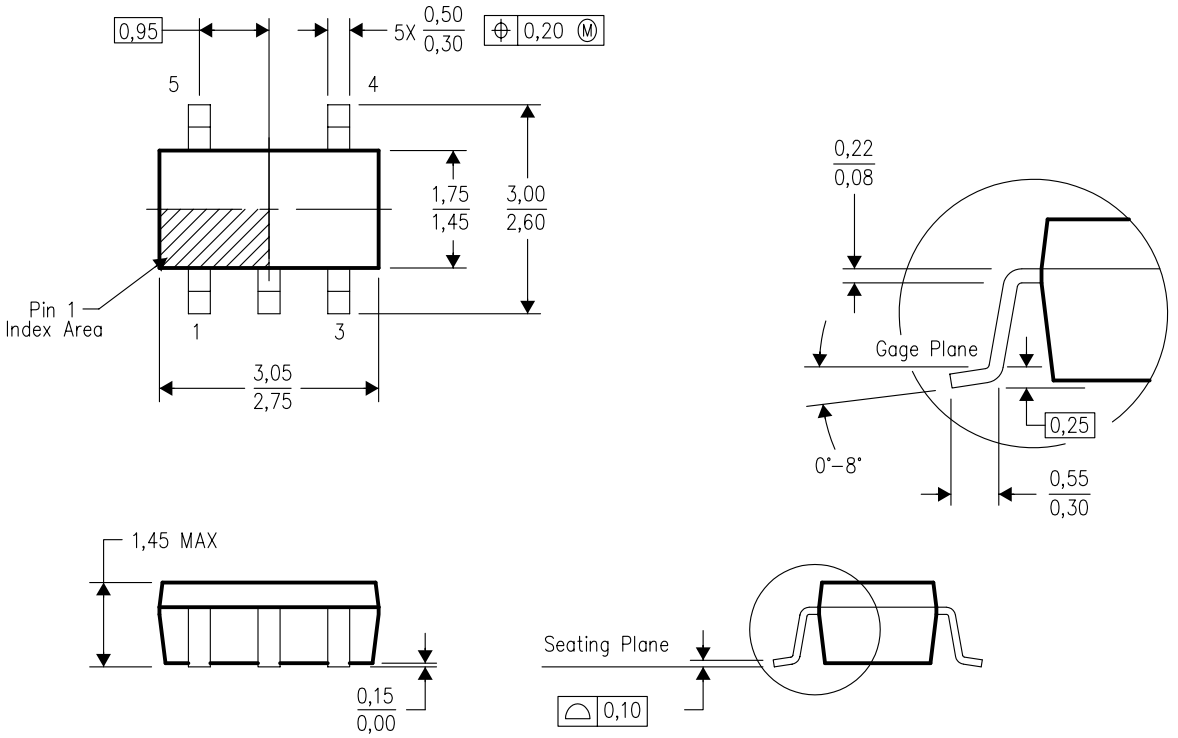
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP2021MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMP2021MF/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMP2021MFE/NOPB	SOT-23	DBV	5	250	203.0	190.0	41.0
LMP2021MFX/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMP2022MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMP2022MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMP2022MME/NOPB	VSSOP	DGK	8	250	203.0	190.0	41.0
LMP2022MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0

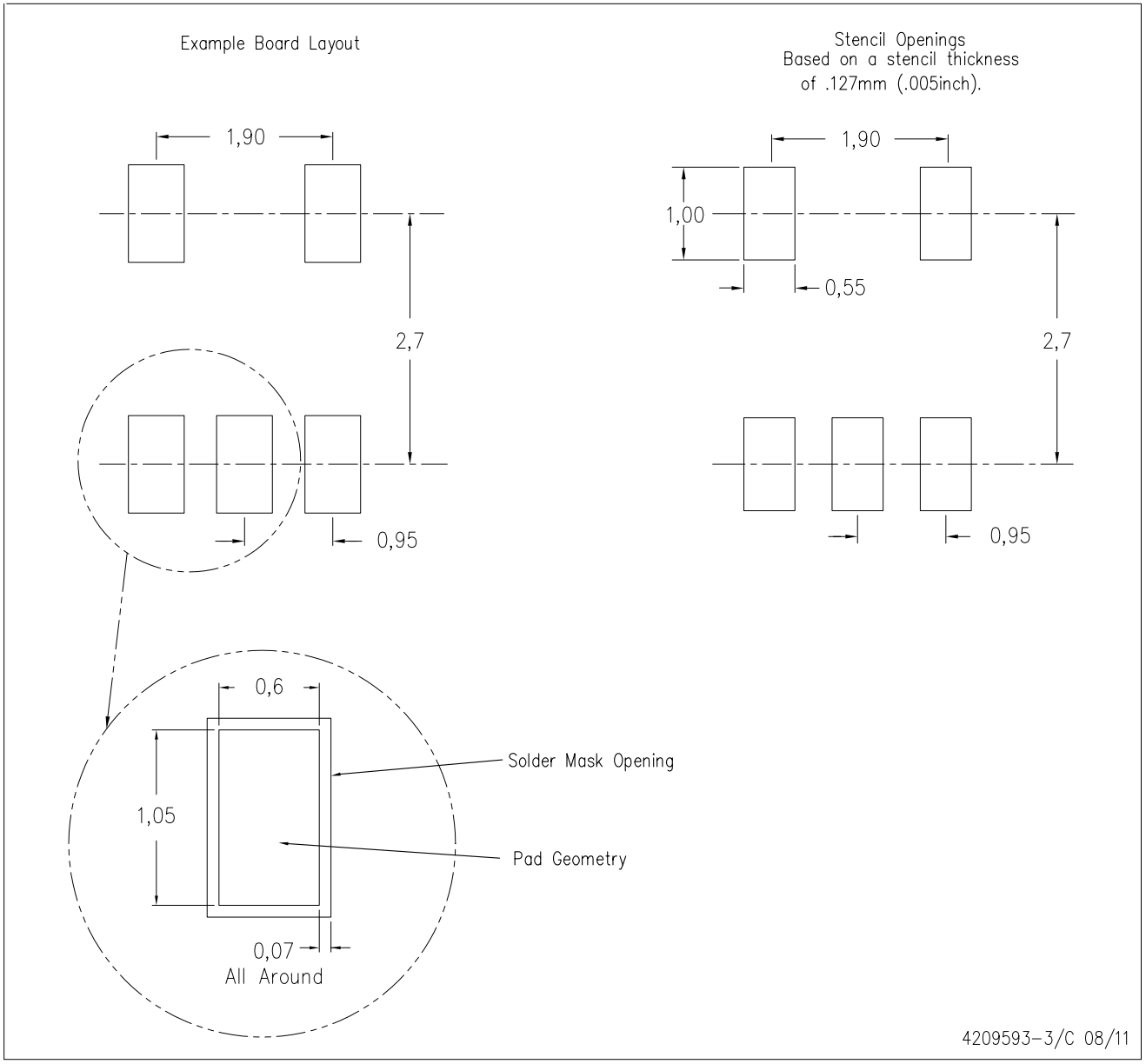
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

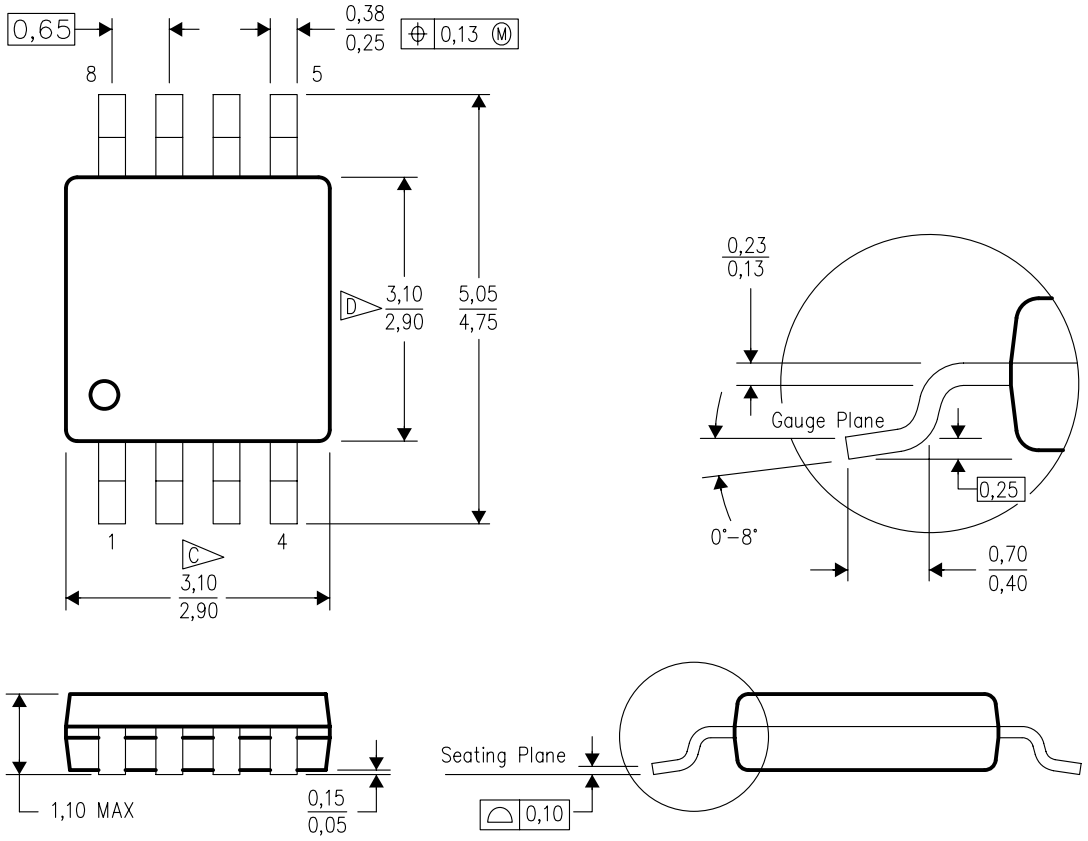
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

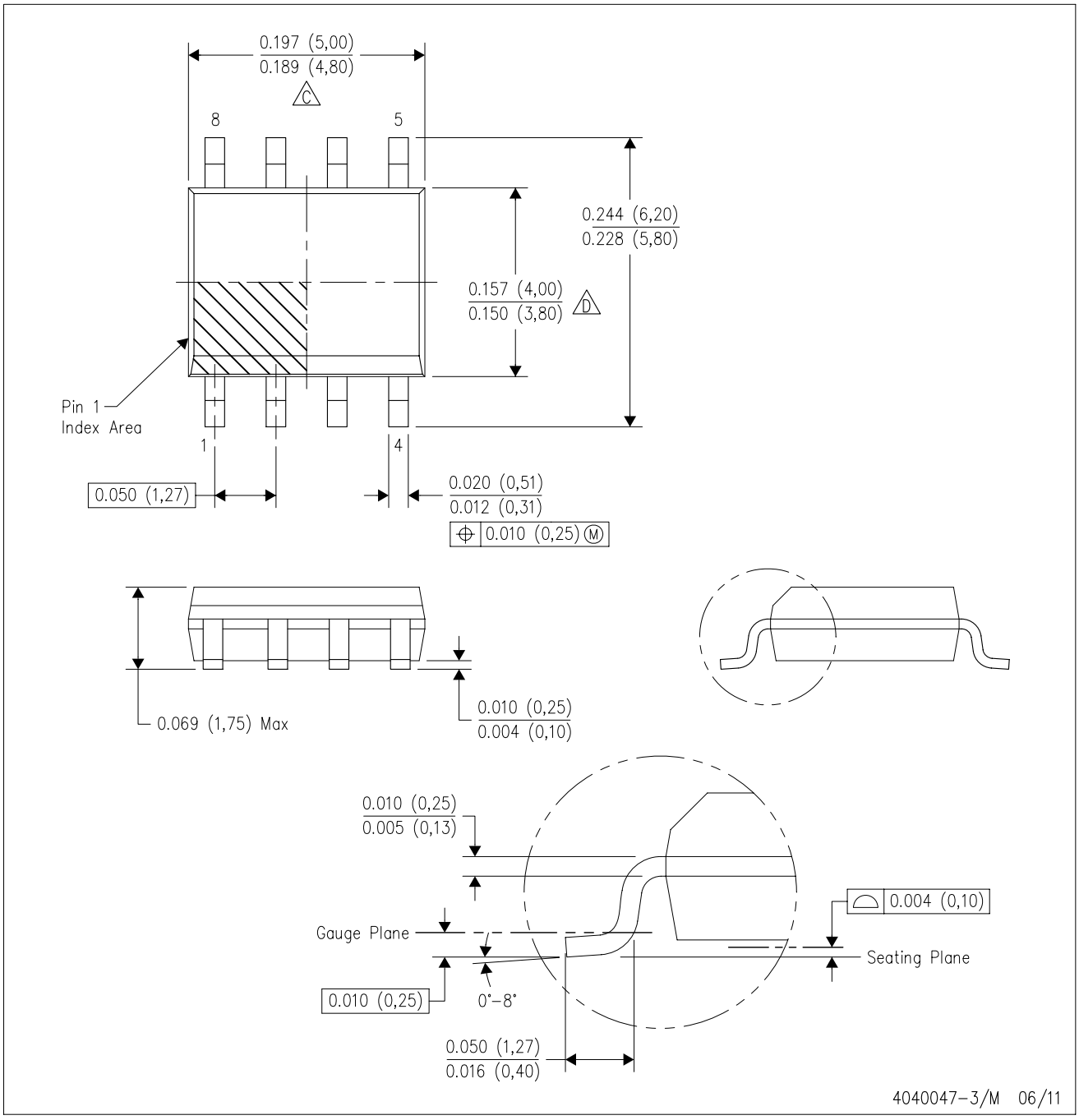
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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