LMP7721 3 Femtoampere Input Bias Current Precision Amplifier

Check for Samples: LMP7721

FEATURES

- Unless Otherwise Noted, Typical Values at T_A = 25°C, V_S = 5V.
- Input Bias Current (V_{CM} = 1V)
  - Max @ 25°C ±20 fA
  - Max @ 85°C ±900 fA
- Offset Voltage ±26 µV
- Offset Voltage Drift −1.5 µV/°C
- DC Open Loop Gain 120 dB
- DC CMRR 100 dB
- Input Voltage Noise (at f = 1 kHz) 6.5 nV/√Hz
- THD 0.0007%
- Supply Current 1.3 mA
- GBW 17 MHz
- Slew Rate (Falling Edge) 12.76 V/µs
- Supply Voltage 1.8V to 5.5V
- Operating Temperature Range −40°C to 125°C
- 8-Pin SOIC

APPLICATIONS

- Photodiode Amplifier
- High Impedance Sensor Amplifier
- Ion Chamber Amplifier
- Electrometer Amplifier
- pH Electrode Amplifier
- Transimpedance Amplifier

DESCRIPTION

The LMP7721 is the industry's lowest guaranteed input bias current precision amplifier. The ultra low input bias current is 3 fA, with a guaranteed limit of ±20 fA at 25°C and ±900 fA at 85°C. This is achieved with the latest patent pending technology of input bias current cancellation amplifier circuitry. This technology also maintains the ultra low input bias current over the entire input common mode voltage range of the amplifier.

Other outstanding features, such as low voltage noise (6.5 nV/√Hz), low DC offset voltage (±150 µV maximum at 25°C) and low offset voltage temperature coefficient (−1.5 µV/°C), improve system sensitivity and accuracy in high precision applications. With a supply voltage range of 1.8V to 5.5V, the LMP7721 is the ideal choice for battery operated portable applications. The LMP7721 is part of the LMP™ precision amplifier family.

As part of National's PowerWise™ products, the LMP7721 provides the remarkably wide gain bandwidth product (GBW) of 17 MHz while consuming only 1.3 mA of current. This wide GBW along with the high open loop gain of 120 dB enables accurate signal conditioning. With these specifications, the LMP7721 has the performance to excel in a wide variety of applications such as electrochemical cell amplifiers and sensor interface circuits.

The LMP7721 is offered in an 8-pin SOIC package with a special pinout that isolates the amplifier's input from the power supply and output pins. With proper board layout techniques, the unique pinout of the LMP7721 will prevent PCB leakage current from reaching the input pins. Thus system error will be further reduced.

Block Diagram of a Typical Application

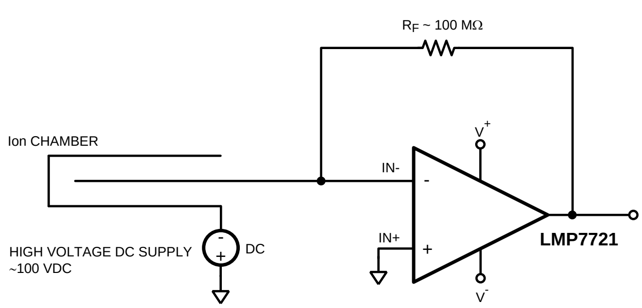


Figure 1. Ion Chamber: Current to Voltage Converter

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
V_{IN} Differential	±0.3V
Supply Voltage ($V_S = V^+ – V^−$) (4)	6.0V
Voltage on Input/Output Pins	V^+ +0.3V, $V^−$ −0.3V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (5)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The voltage on any pin should not exceed 6V relative to any other pins.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/θ_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings (1)

Temperature Range (2)	−40°C to 125°C
Supply Voltage ($V_S = V^+ – V^−$)	
0°C ≤ T_A ≤ 125°C	1.8V to 5.5V
−40°C ≤ T_A ≤ 125°C	2.0V to 5.5V
Package Thermal Resistance ($θ_{JA}$ (2))	
8-Pin SOIC	190°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/θ_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

2.5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 2.5V, $V^−$ = 0V, $V_{CM} = (V^+ + V^−)/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			±50	±180 **±480**	µV
TC V_{OS}	Input Offset Voltage Drift (3)			–1.5	–4	µV/°C

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.

2.5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 2.5V, V^- = 0V, V_{CM} = (V^+ + V^-)/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
I_{BIAS}	Input Bias Current	V_{CM} = 1V (4) (5)	25°C		±3	±20	fA
			−40°C to 85°C			±900	
			−40°C to 125°C			**±5**	pA
I_{OS}	Input Offset Current	V_{CM} = 1V (5)			6	40	fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.4V		83 **80**	100		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0		84 **80**	92		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB		−0.3 **–0.3**		1.5 **1.5**	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.15V to 2.2V R_L = 2 kΩ to V^+/2		88 **82**	107		dB
		V_O = 0.15V to 2.2V R_L = 10 kΩ to V^+/2		92 **88**	120		
V_O	Output Swing High	R_L = 2 kΩ to V^+/2		70 **77**	25		mV from V^+
		R_L = 10 kΩ to V^+/2		60 **66**	20		
	Output Swing Low	R_L = 2 kΩ to V^+/2			30	70 **73**	mV
		R_L = 10 kΩ to V^+/2			15	60 **62**	
I_O	Output Short Circuit Current	Sourcing to V^- V_{IN} = 200 mV (6)		36 **30**	46		mA
		Sinking to V^+ V_{IN} = −200 mV (6)		7.5 **5.0**	15		
I_S	Supply Current				1.1	1.5 **1.75**	mA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)			9.3		V/μs
		A_V = +1, Falling (90% to 10%)			10.8		
GBW	Gain Bandwidth Product				15		MHz
e_n	Input-Referred Voltage Noise	f = 400 Hz			8		$nV/\sqrt{Hz}$
		f = 1 kHz			7		
i_n	Input-Referred Current Noise	f = 1 kHz			0.01		$pA/\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 2, R_L = 100 kΩ V_O = 0.9 V_{PP}			0.003		%
		f = 1 kHz, A_V = 2, R_L = 600Ω V_O = 0.9 V_{PP}			0.003		

(4) Positive current corresponds to current flowing into the device.
(5) This parameter is guaranteed by design and/or characterization and is not tested in production.
(6) The short circuit test is a momentary open loop test.

5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = (V^+ + V^-)/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage				±26	±150 **±450**	μV
TC V_{OS}	Input Offset Average Drift (3)				–1.5	–4	μV/°C
I_{BIAS}	Input Bias Current	V_{CM} = 1V (4) (5)	25°C		±3	±20	fA
			−40°C to 85°C			±900	
			−40°C to 125°C			**±5**	pA
I_{OS}	Input Offset Current	(5)			6	40	fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.7V		84 **82**	100		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0		84 **80**	96		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB		−0.3 **–0.3**		4 **4**	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.3V to 4.7V R_L = 2 kΩ to V^+/2		88 **82**	111		dB
		V_O = 0.3V to 4.7V R_L = 10 kΩ to V^+/2		92 **88**	120		
V_O	Output Swing High	R_L = 2 kΩ to V^+/2		70 **77**	30		mV from V^+
		R_L = 10 kΩ to V^+/2		60 **66**	20		
	Output Swing Low	R_L = 2 kΩ to V^+/2			31	70 **73**	mV
		R_L = 10 kΩ to V^+/2			20	60 **62**	
I_O	Output Short Circuit Current	Sourcing to V^- V_{IN} = 200 mV (6)		46 **38**	60		mA
		Sinking to V^+ V_{IN} = −200 mV (6)		10.5 **6.5**	22		
I_S	Supply Current				1.3	1.7 **1.95**	mA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)			10.43		V/μs
		A_V = +1, Falling (90% to 10%)			12.76		
GBW	Gain Bandwidth Product				17		MHz
e_n	Input-Referred Voltage Noise	f = 400 Hz			7.5		nV/$\sqrt{Hz}$
		f = 1 kHz			6.5		
i_n	Input-Referred Current Noise	f = 1 kHz			0.01		pA/$\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 2, R_L = 100 kΩ V_O = 4 V_{PP}			0.0007		%
		f = 1 kHz, A_V = 2, R_L = 600Ω V_O = 4 V_{PP}			0.0007		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is guaranteed by design and/or characterization and is not tested in production.
(6) The short circuit test is a momentary open loop test.

CONNECTION DIAGRAM

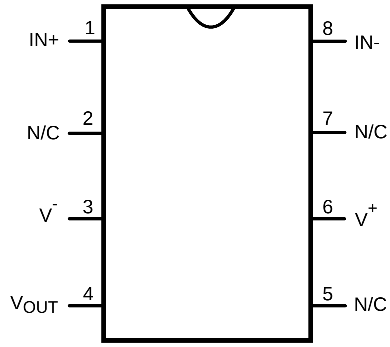


Figure 2. 8-Pin SOIC
Top View

Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

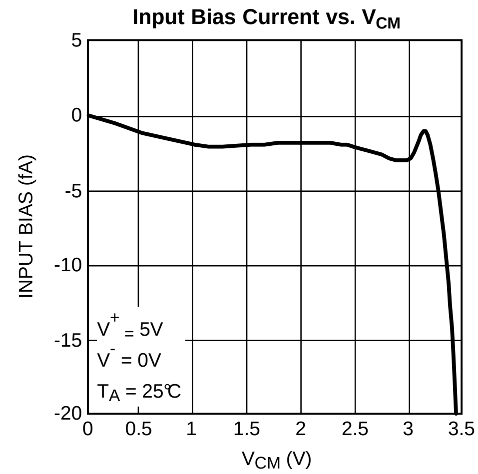


Figure 3.

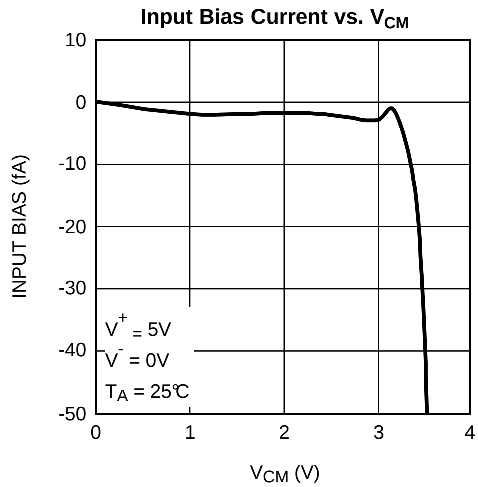


Figure 4.

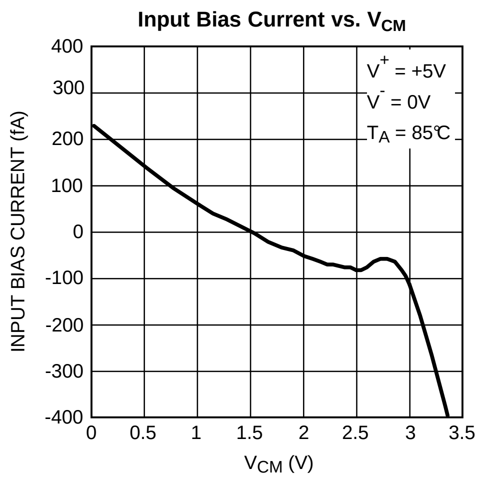
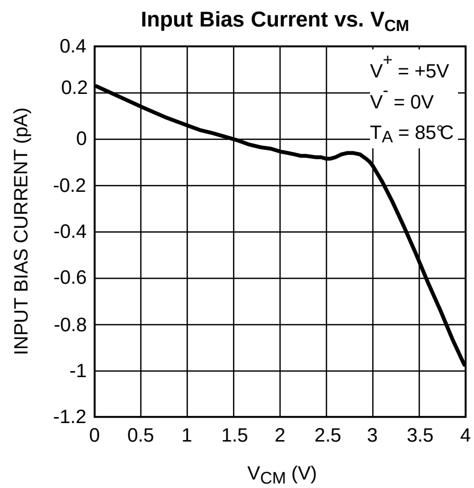


Figure 5.



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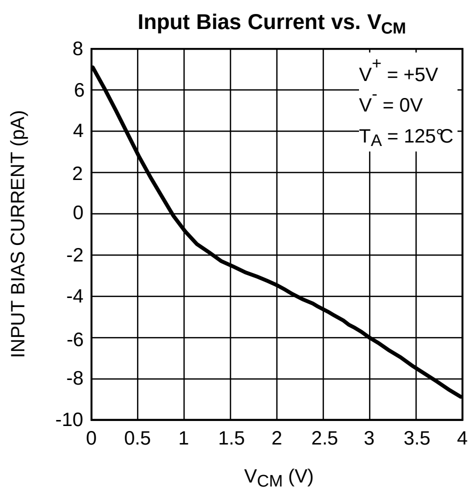


Figure 7.

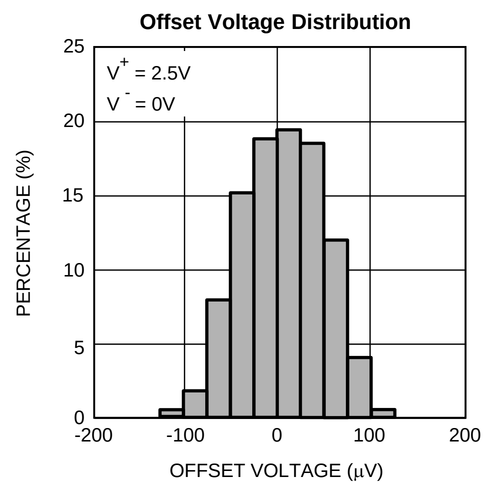


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

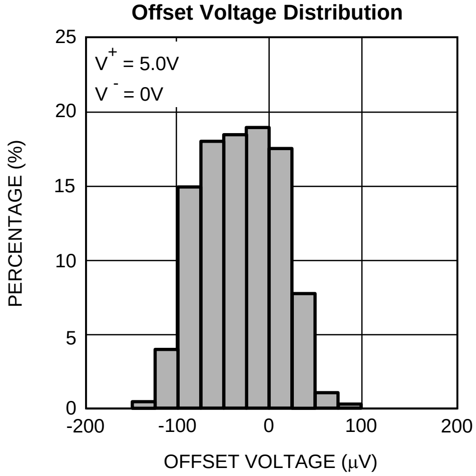


Figure 9.

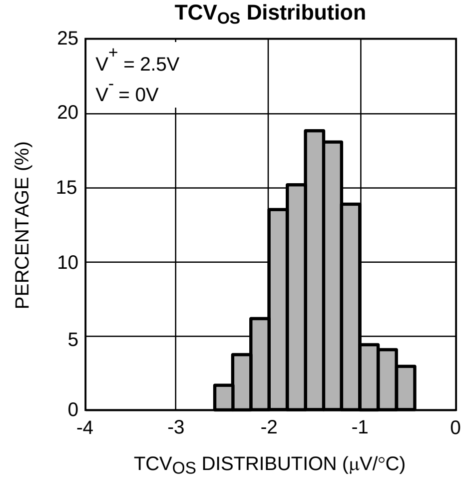
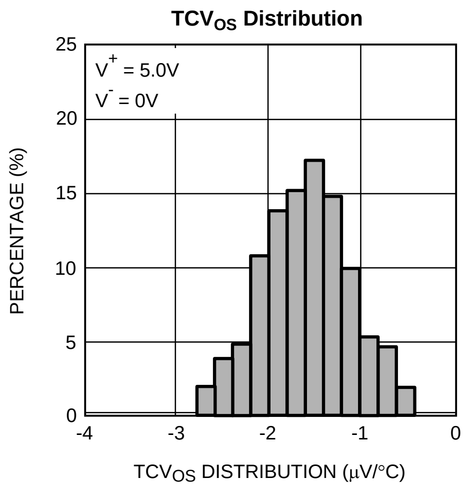


Figure 10.



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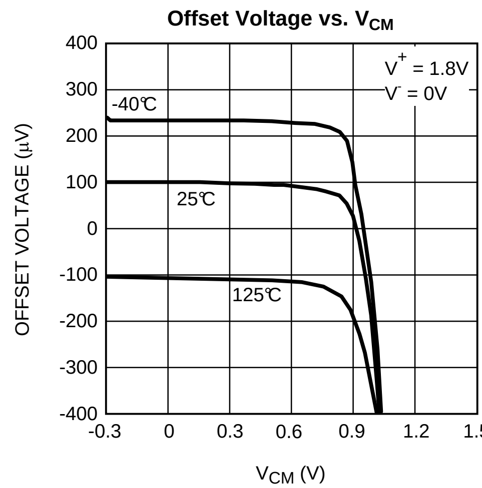

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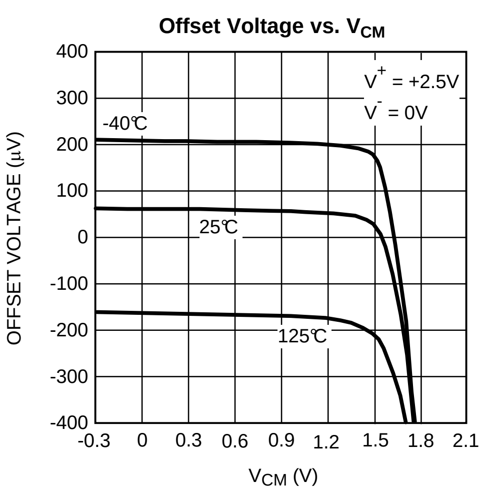


Figure 13.

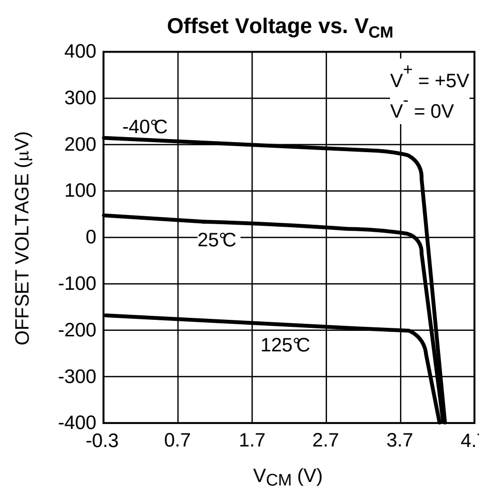


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

Offset Voltage vs. Supply Voltage

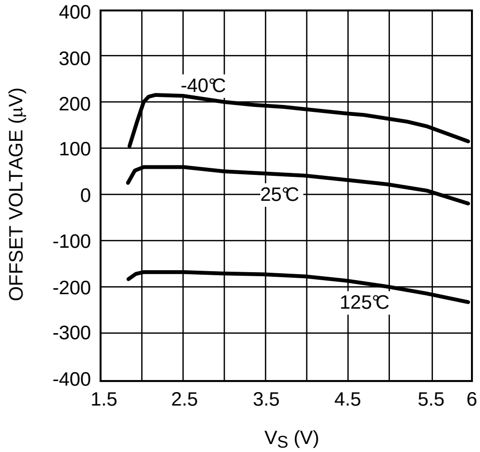


Figure 15.

Offset Voltage vs. Temperature

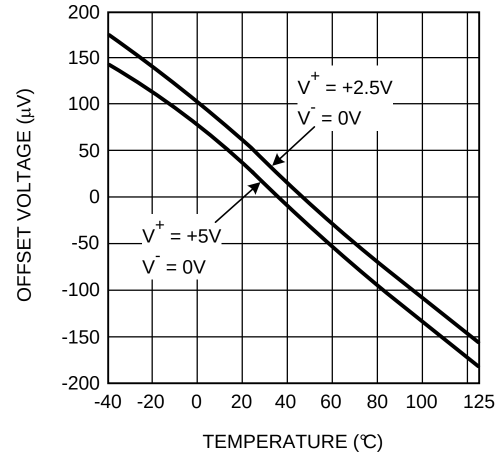


Figure 16.

Supply Current vs. Supply Voltage

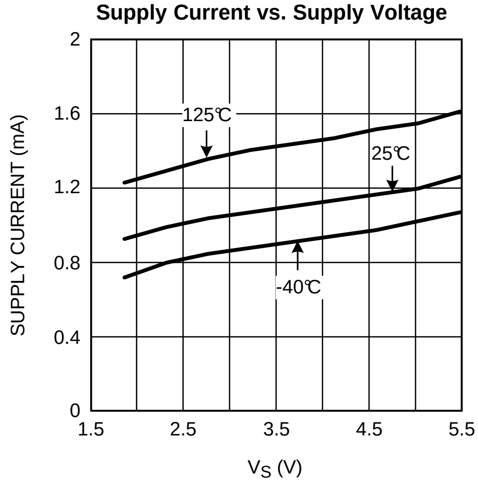


Figure 17.

Open Loop Frequency Response Gain and Phase

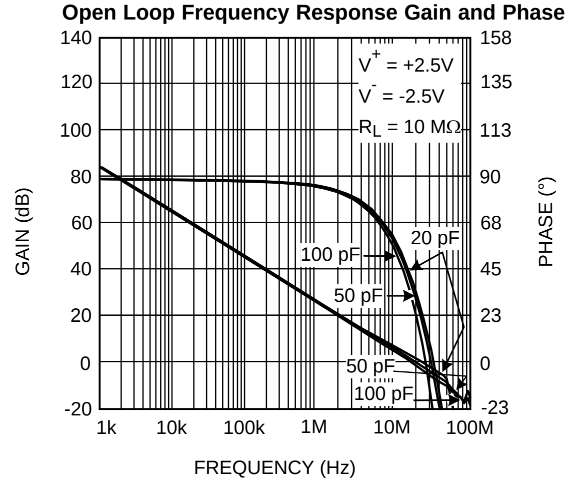


Figure 18.

Open Loop Frequency Response Gain and Phase

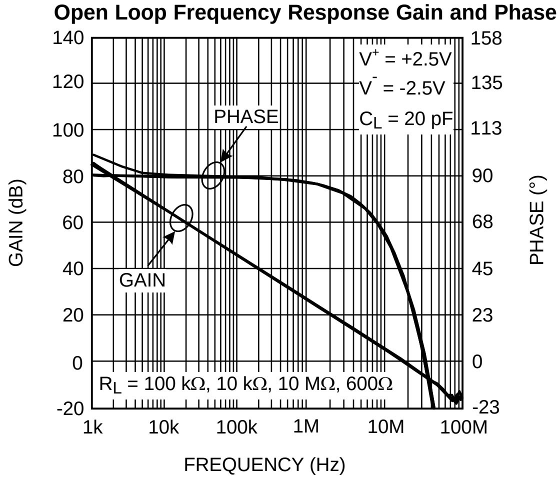


Figure 19.

Phase Margin vs. Capacitive Load

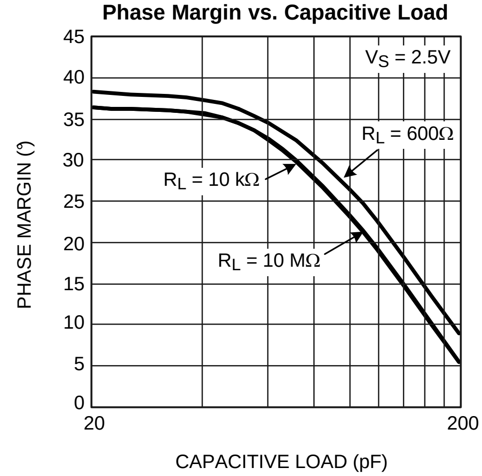


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

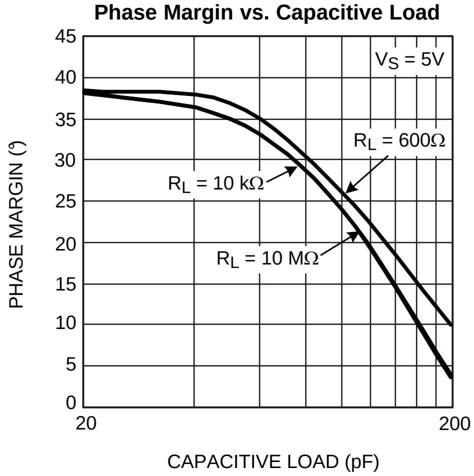
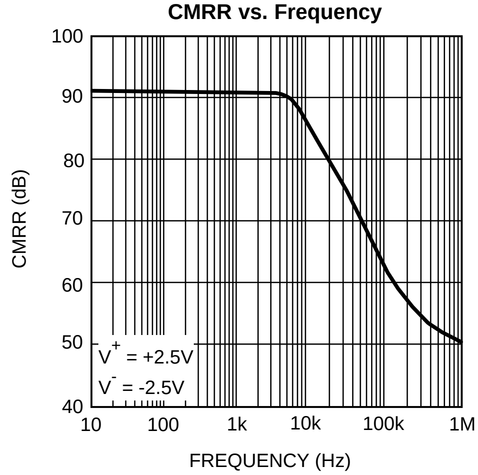


Figure 21.



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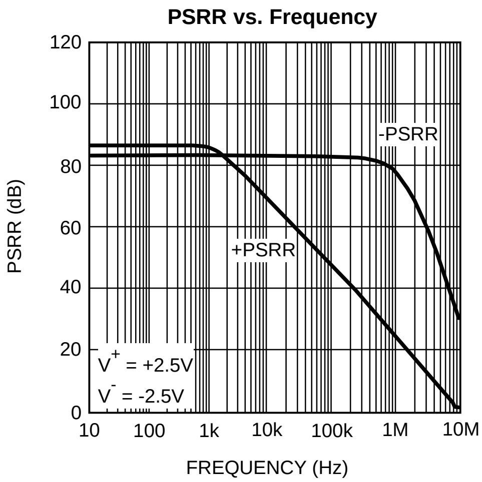


Figure 23.

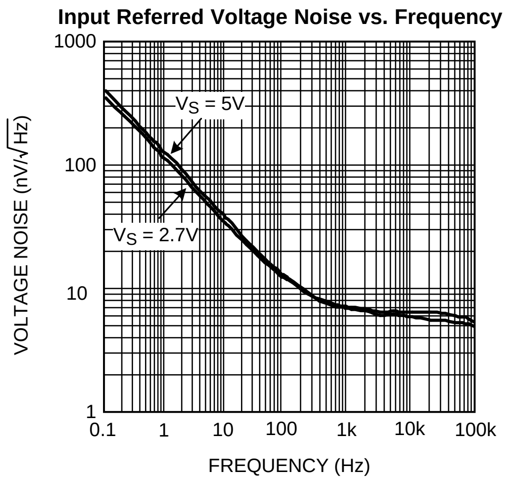
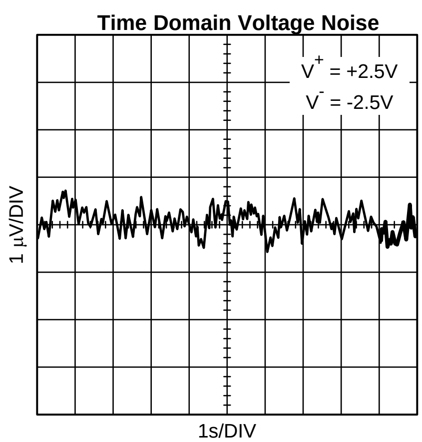


Figure 24.



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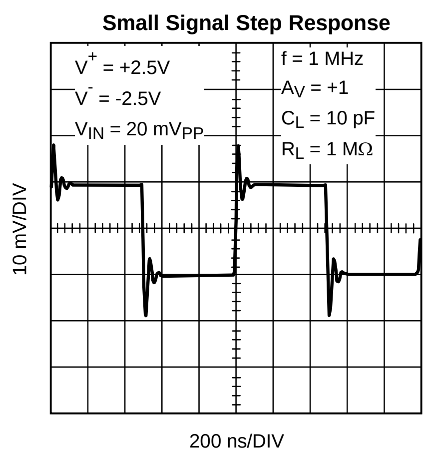


Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

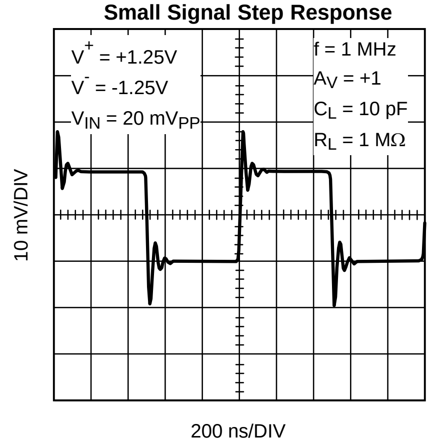


Figure 27.

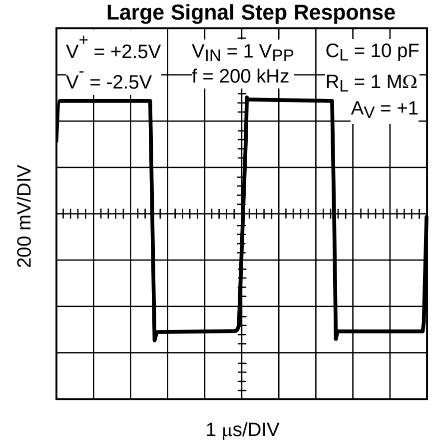
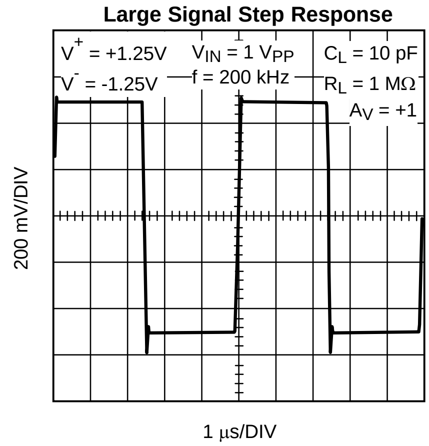


Figure 28.



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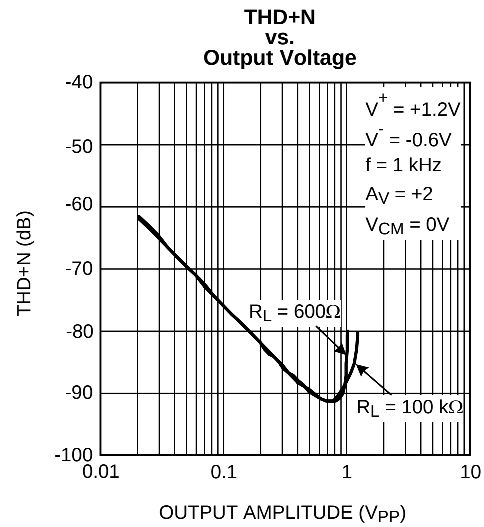
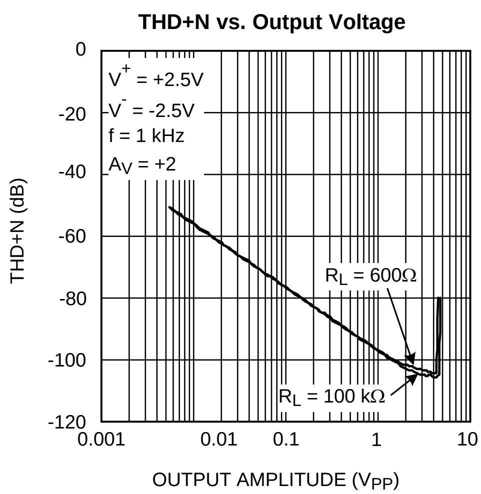


Figure 30.



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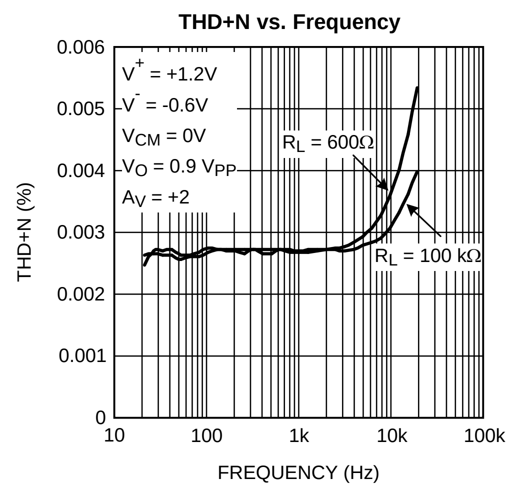


Figure 32.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, $V_{CM} = (V^+ + V^-)/2$.

THD+N vs. Frequency

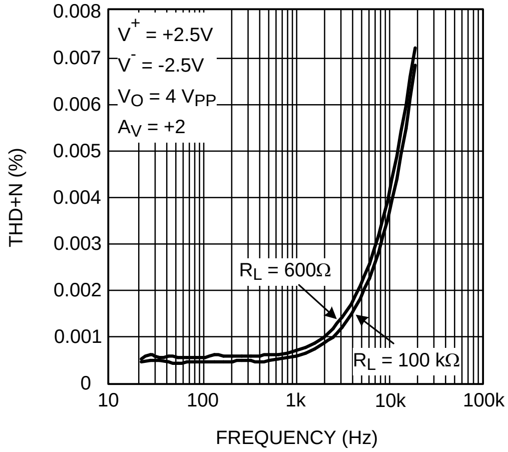


Figure 33.

Sourcing Current vs. Supply Voltage

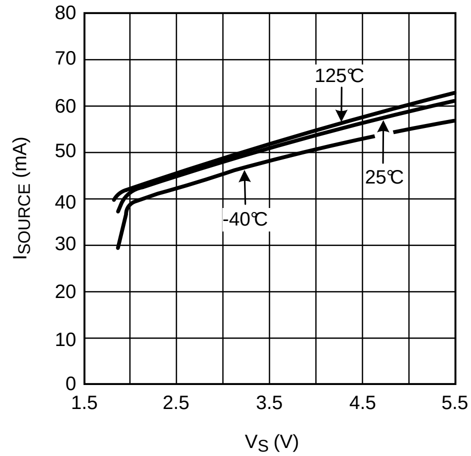


Figure 34.

Sinking Current vs. Supply Voltage

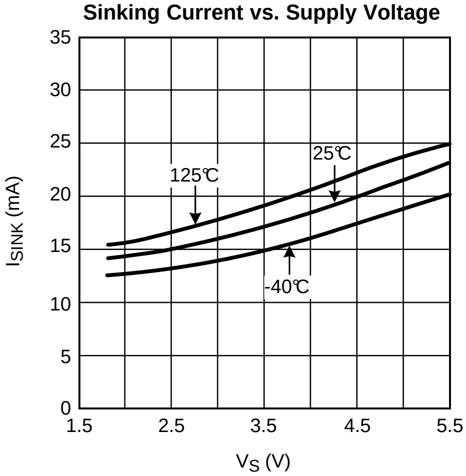


Figure 35.

Sourcing Current vs. Output Voltage

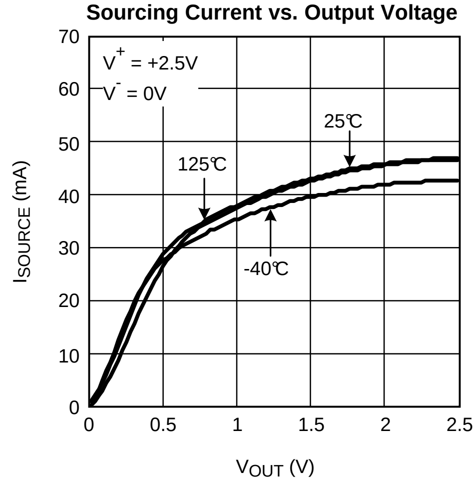


Figure 36.

Sourcing Current vs. Output Voltage

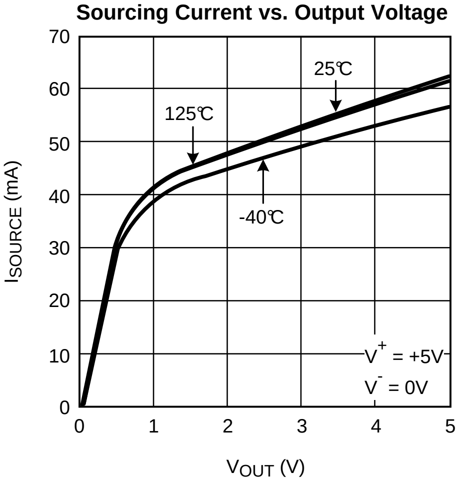


Figure 37.

Sinking Current vs. Output Voltage

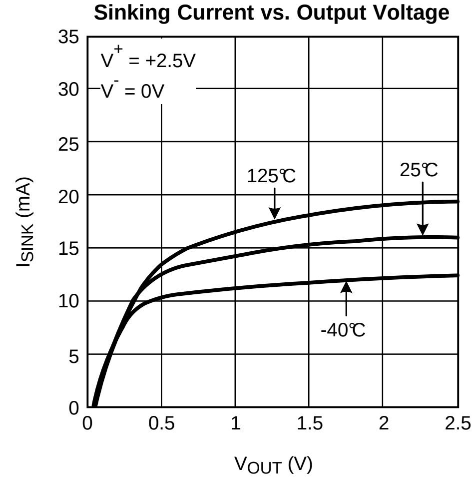


Figure 38.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

Sinking Current vs. Output Voltage

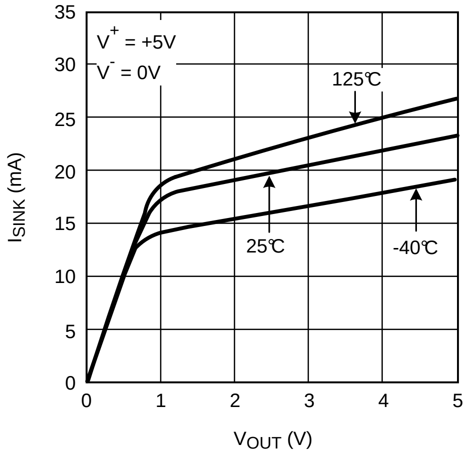


Figure 39.

Output Swing High vs. Supply Voltage

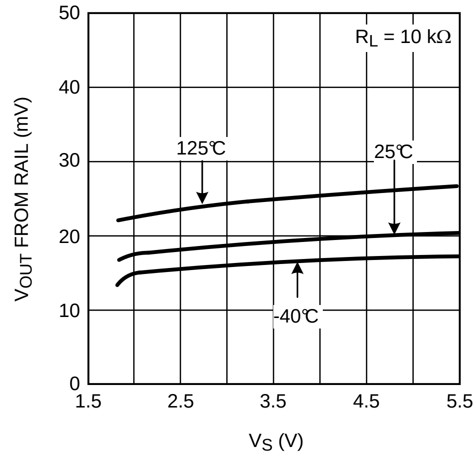


Figure 40.

Output Swing Low vs. Supply Voltage

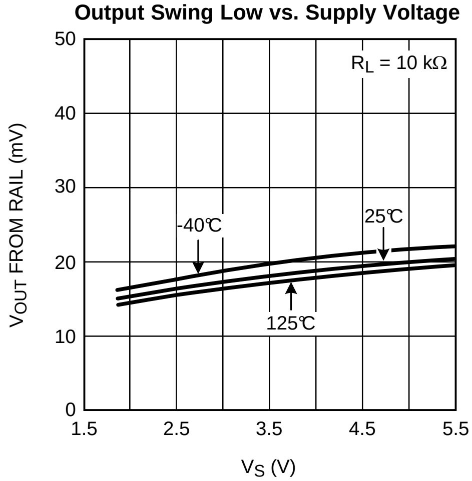


Figure 41.

Output Swing High vs. Supply Voltage

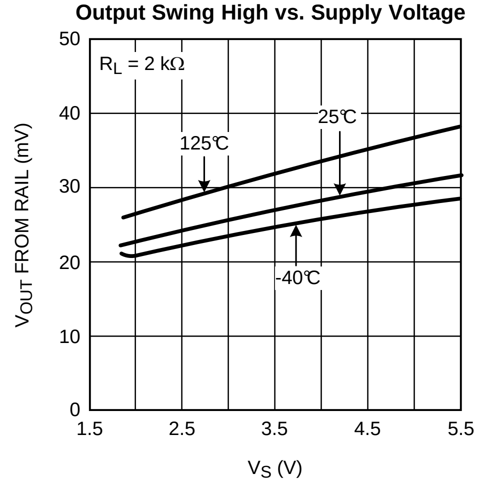


Figure 42.

Output Swing Low vs. Supply Voltage

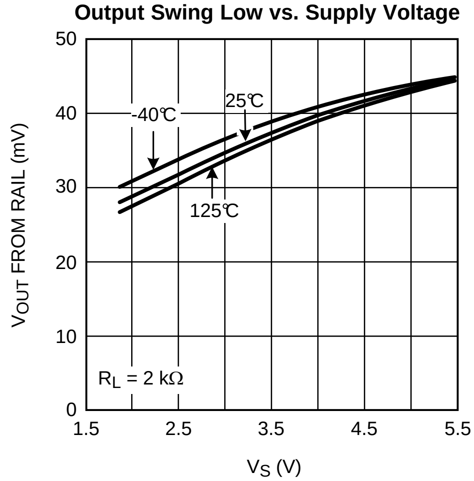


Figure 43.

Output Swing High vs. Supply Voltage

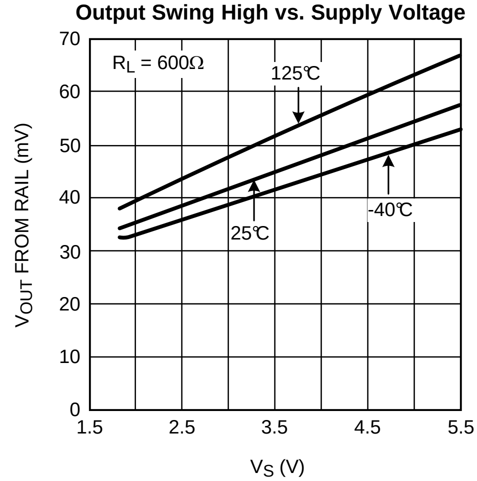


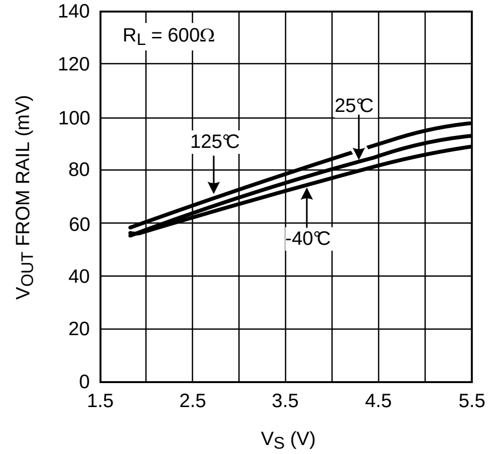
Figure 44.

Figure 45.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

Output Swing Low vs. Supply Voltage



APPLICATION INFORMATION

ADVANTAGES OF THE LMP7721

Ultra Low Input Bias Current

The LMP7721 has the industry's lowest guaranteed input bias current. The ultra low input bias current is typically 3 fA, with a guaranteed limit of ±20 fA at 25°C, ±900 fA at 85°C and ±5 pA at 125°C when V_{CM} = 1V with a 5V or a 2.5V power supply.

Wide Bandwidth at Low Supply Current

The LMP7721 is a high performance amplifier that provides a 17 MHz unity gain bandwidth while drawing only 1.3 mA of current. This makes the LMP7721 ideal for wideband amplification in portable applications.

Low Input Referred Noise

The LMP7721 has a low input referred voltage noise density (6.5 nV$\sqrt{Hz}$ at 1 kHz with 5V supply). Its MOS input stage ensures a very low input referred current noise density (0.01 pA/$\sqrt{Hz}$).

The low input referred noise and the ultra low input bias current make the LMP7721 stand out in maintaining signal fidelity. This quality makes the LMP7721 a suitable candidate for sensor based applications.

Low Supply Voltage

The LMP7721 has performance guaranteed at 2.5V and 5V power supplies. The LMP7721 is guaranteed to be functional at all supply voltages between 2.0V to 5.5V, for ambient temperatures ranging from −40°C to 125°C. This means that the LMP7721 has a long operational span over the battery's lifetime. The LMP7721 is also guaranteed to be functional at 1.8V supply voltage, for ambient temperatures ranging from 0°C to 125°C. This makes the LMP7721 ideal for use in low voltage commercial applications.

RRO and Ground Sensing

Rail-to-rail output swing provides the maximum possible output dynamic range. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is created to boost the LMP7721's output current drive capability. This allows the LMP7721 to source 30 mA to 40 mA of current at 1.8V power supply.

The LMP7721's input common mode range includes the negative supply rail which makes direct sensing at ground possible in single supply operation.

Unique Pinout

The LMP7721 has been designed with the IN+ and IN−, V^+ and V^- pins on opposite sides of the package. There are isolation pins between IN+ and V^-, IN− and V+. This unique pinout makes it easy to guard the LMP7721's input. This pinout design reduces the input bias current's dependence on common mode or supply bias.

The SOIC package features low leakage and it has large pin spacing. This lowers the probability of dust particles settling down between two pins thus reducing the resistance between the pins which can be a problem.

Input Protection

The LMP7721 input stage is protected from seeing excessive differential input voltage by a pair of back-to-back diodes attached between the inputs. This limits the differential voltage and hence prevents phase inversion as well as any performance drift. These diodes can conduct current when the input signal has a really fast edge, and, if necessary, should be isolated (using a resistor or a current follower) in such cases.

SYSTEM DESIGN TECHNIQUES WITH THE LMP7721

In order to take full advantage of the LMP7721's ultra low input bias current, a triaxial cable/connector is recommended when designing application systems.

A triaxial cable/connector is similar to a coaxial cable/connector and is often referred to as "triax". Figure 46 shows the structure of the triax.

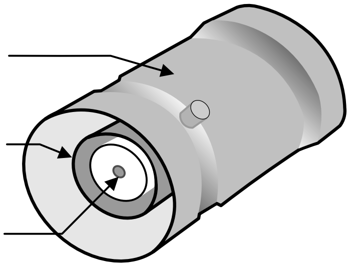


Figure 46. The Structure of a Triax

The signal conductor and the guard of the triax should be kept at the same potential; therefore, the leakage current between them is practically zero. Since triax has an extra layer of insulation and a second conducting sheath, it offers greater rejection of interference than coaxial cable/connector.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMP7721 allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the General Operational Amplifier circuit, Figure 47 the frequency of this pole is

$$f_p = \frac{1}{2\pi C_S R_P} \quad (1)$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. The typical input capacitance of the LMP7721 is about 10pF. This formula, as well as all formulas derived below, apply to inverting and non-inverting op amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 15 pF. If the frequency of the feedback pole is much higher than the “ideal” closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the “ideal” −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier’s low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S} \quad (2)$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right) \quad (3)$$

is the amplifier’s low-frequency noise gain and GBW is the amplifier’s gain bandwidth product. An amplifier’s low frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \tag{4}$$

regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \geq 2\sqrt{GBW \times R_F \times C_S} \tag{5}$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1 \right)} \tag{6}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1 \right) < 2\sqrt{GBW \times R_F \times C_S} \tag{7}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}} \tag{8}$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F} \tag{9}$$

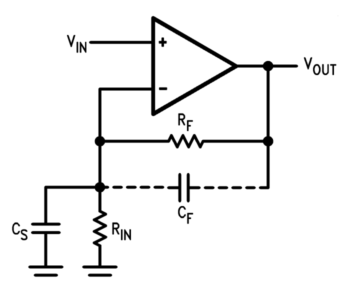


Figure 47. General Operational Amplifier Circuit

NOTE

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

TRANSIMPEDANCE AMPLIFIER EXAMPLE (INVERTING CONFIGURATION)

A transimpedance amplifier converts a small amount of current into voltage. The transfer function of a transimpedance amplifier is $V_{out} = -I_{in} * R_F$. Figure 48 shows a typical transimpedance amplifier.

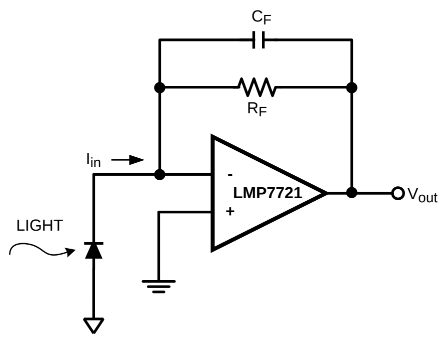


Figure 48. Photodiode Transimpedance Amplifier

The current is generated by a photodiode. The amount of the current is so small that it requires a large gain from the transimpedance amplifier in order to transform the miniscule current into easily detectable voltages. The larger the gain, the larger the value of R_F needed. When R_F is larger, the error caused by I_{bias}*R_F increases. For example, if R_F is 1000 MΩ, and an op amp with 3 nA of I_{bias} is used, the I_{bias}*R_F error at the output will be 3V! This error can be dramatically reduced to 3 µV by using the LMP7721.

Photodiodes are high impedance sensors which require careful design of the associated signal conditioning circuitry in order to meet the system challenges. CMOS input op amps are often used in transimpedance applications as they have extremely high input impedance. A triaxial cable is recommended for its very low noise pick-up.

A MOS input stage with ultra low input bias current, negligible input current noise, and low input voltage noise allows the LMP7721 to provide high fidelity amplification. In addition, the LMP7721 has a 17 MHz gain bandwidth product, which enables high gain at wide bandwidth. A rail-to-rail output swing at 5.5V power supply allows detection and amplification of a wide range of input currents. These properties make the LMP7721 ideal for transimpedance amplification.

Figure 49 is an example of the LMP7721 used as a transimpedance amplifier.

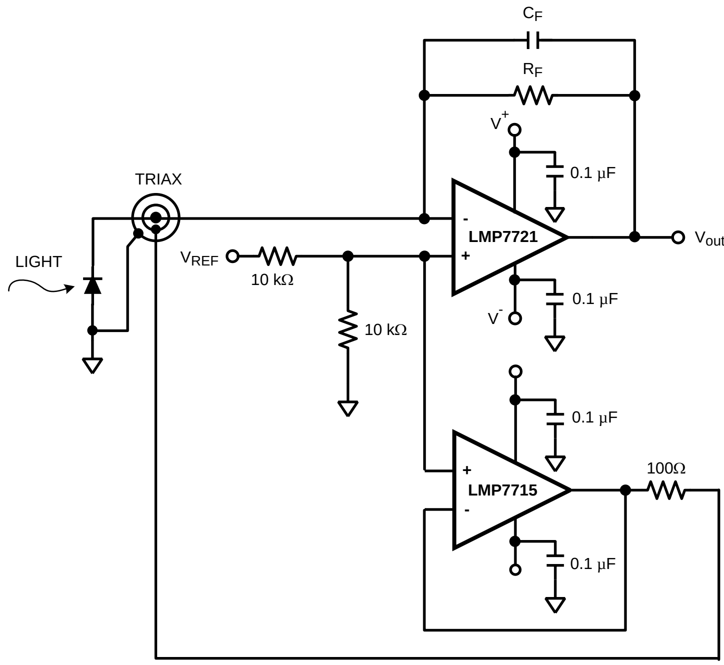


Figure 49. LMP7721 as Transimpedance Amplifier

The current generated by the photodiode is fed to the signal conductor of the triax and then sent to the inverting input of the LMP7721. The LMP7721's non-inverting input is biased at $V_{REF}/2$ for level shifting purposes. In this application, the non-inverting input is a low impedance node and hence is used to drive the LMP7715 which acts as a guard driver. The output of the guard driver is connected to the guard of the triax via a 100Ω isolation resistor. Ideally, the inverting and the non-inverting inputs of the amplifier are kept at the same potential through the operation of the amplifier. By connecting the signal conductor to the inverting input and letting the non-inverting input drive the guard, the signal conductor and the guard are kept at the same potential which prevents leakage from the signal source.

pH ELECTRODE AMPLIFIER EXAMPLE (NON-INVERTING CONFIGURATION)

The output of a pH electrode ranges from 415 mV to −415 mV as the pH changes from 0 to 14 at 25°C. The output impedance of a pH electrode is extremely high, ranging from 10 MΩ to 1000 MΩ. The ultra low input bias current of the LMP7721 allows the voltage error produced by the input bias current and electrode resistance to be minimal. For example, the output impedance of the pH electrode used is 10 MΩ, if an op amp with 3 nA of I_{bias} is used, the error caused due to this amplifier's input bias current and the source resistance of the pH electrode is 30 mV! This error can be greatly reduced to 30 nV by using the LMP7721.

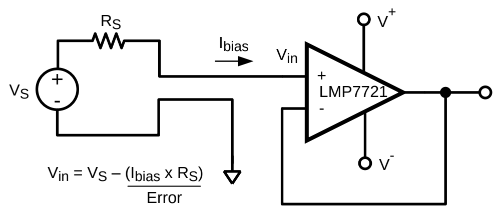


Figure 50. Error Caused by Amplifier's Input Bias Current and Sensor Source Impedance

Figure 51 is an example of the LMP7721 used as a pH sensor amplifier.

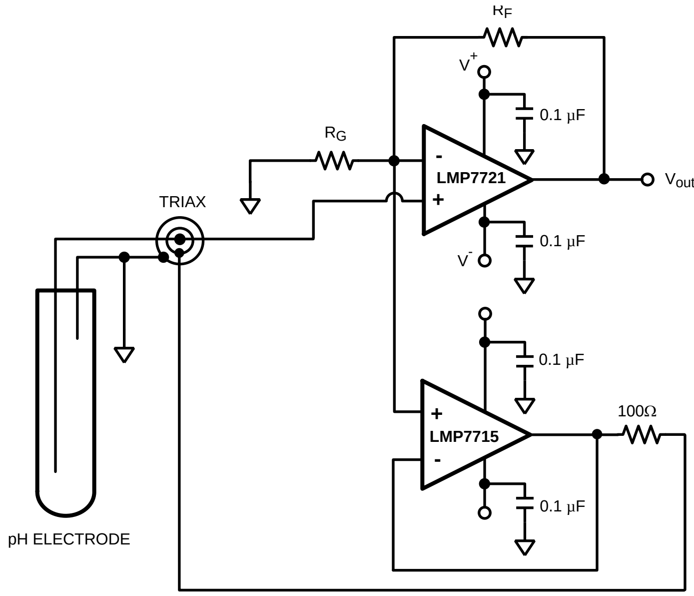


Figure 51. LMP7721 as pH Electrode Amplifier

The output voltage from the pH electrode is fed to the signal conductor of the triax and then sent to the non-inverting input of the LMP7721. In this application, the inverting input is a low impedance node and hence is used to drive the LMP7715 which acts as a guard driver. The output of the guard driver is connected to the guard of the triax via a 100Ω isolation resistor. Ideally, the inverting and the non-inverting inputs of the amplifier are kept at the same potential through the operation of the amplifier. By connecting the signal conductor to the non-inverting input and letting the inverting input drive the guard, the signal conductor and the guard are kept at the same potential which prevents leakage from the signal source.

LAYOUT AND ASSEMBLY CONSIDERATIONS

In order to capitalize on the LMP7721's ultra low input bias current, careful circuit layout and assembly are required. Guarding techniques are highly recommended to reduce parasitic leakage current by isolating the LMP7721's input from large voltage gradients across the PC board. A guard is a low impedance conductor that surrounds an input line and its potential is raised to the input line's voltage. The input pins should be fully guarded as shown in Figure 52. The guard traces should completely encircle the input connections. In addition, they should be located on both sides of the PCB and be connected together.

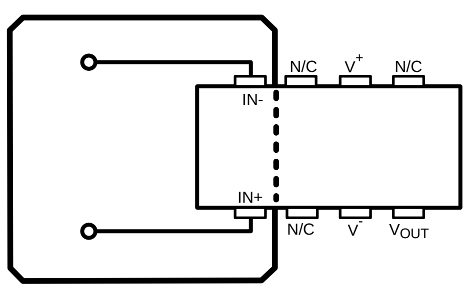


Figure 52. Circuit Board Guard Layout

Solder mask should not cover the input and the guard area including guard traces on either side of the PCB.

Sockets are not recommended as they can be a significant leakage source. After assembly, a thorough cleaning using commercial solvent is necessary.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP7721MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP77 21MA	Samples
LMP7721MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP77 21MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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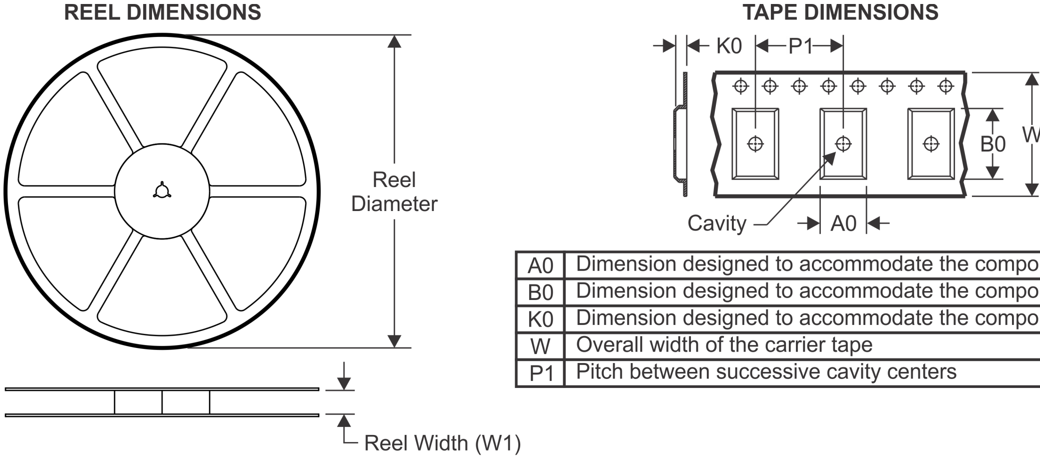
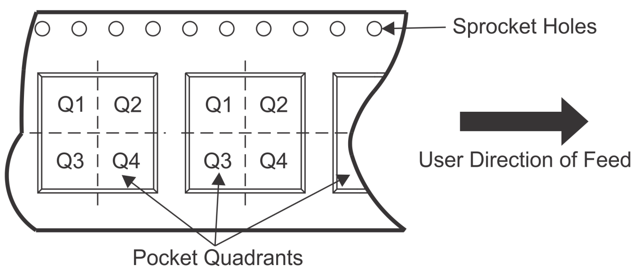
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

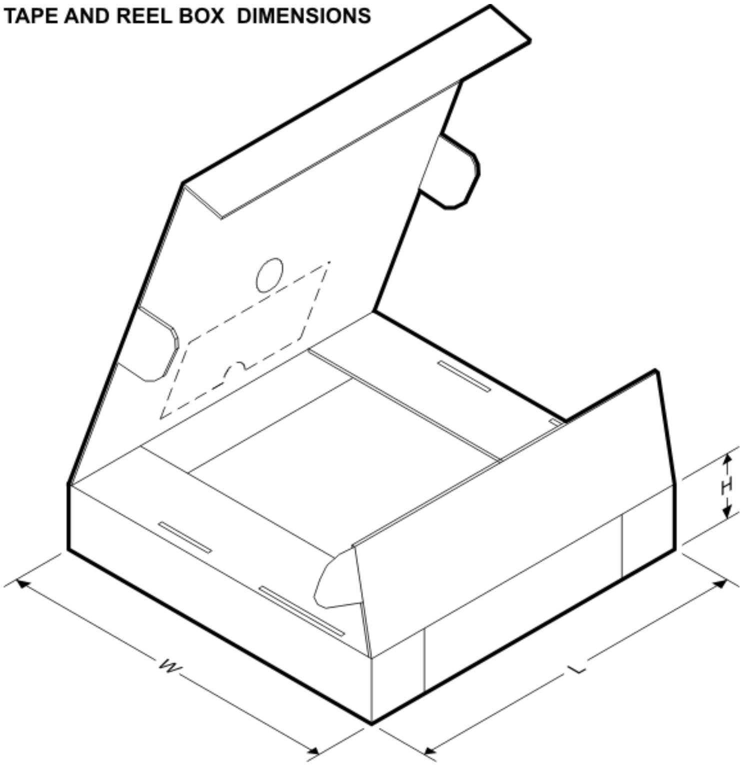
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7721MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

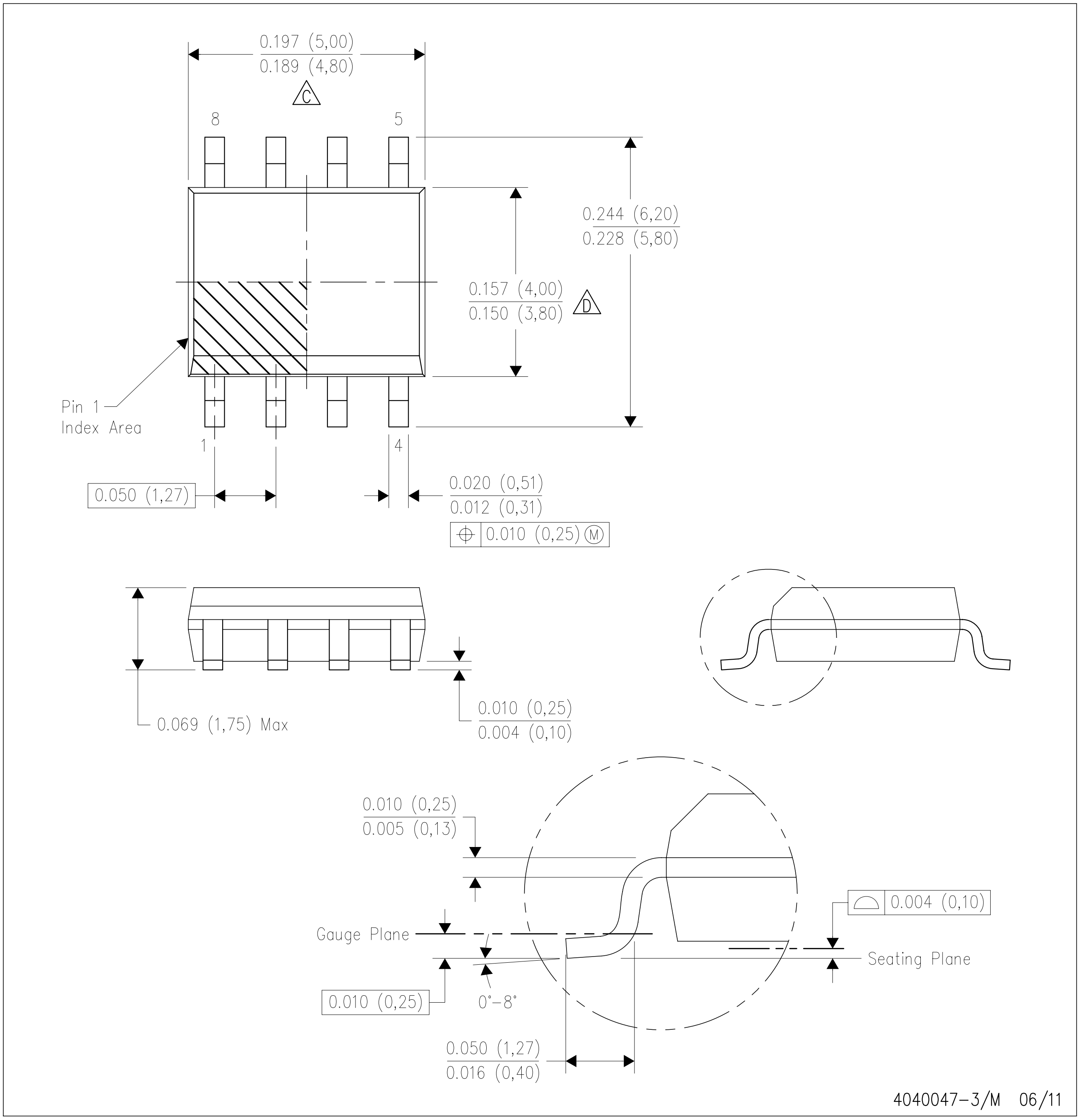
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7721MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.