LMP91002 Sensor AFE System: Configurable AFE Potentiostat for Low-Power Chemical Sensing Applications

Check for Samples: LMP91002

FEATURES

- **Typical Values, T_A = 25°C**
- **Supply Voltage 2.7 V to 3.6 V**
- **Supply Current (Average Over Time) <10 µA**
- **Cell Conditioning Current Up to 10 mA**
- **Reference Electrode Bias Current (85°C) 900pA (Max)**
- **Output Drive Current 750µA**
- **Complete Potentiostat Circuit to Interface to Most Not Biased Gas Sensors**
- **Low Bias Voltage Drift**
- **Programmable TIA Gain 2.75kΩ to 350kΩ**
- **I^2C Compatible Digital Interface**
- **Ambient Operating Temperature -40°C to 85°C**
- **Package 14 pin WSON**
- **Supported by Webench Sensor AFE Designer**

APPLICATIONS

- **Gas Detector**
- **Amperometric Applications**
- **Electrochemical Blood Glucose Meter**

DESCRIPTION

The LMP91002 is a programmable Analog Front End (AFE) for use in micro-power electrochemical sensing applications. It provides a complete signal path solution between a not biased gas sensor and a microcontroller generating an output voltage proportional to the cell current. The LMP91002's programmability enables it support not biased electro-chemical gas sensor with a single design. The LMP91002 supports gas sensitivities over a range of 0.5 nA/ppm to 9500 nA/ppm. It also allows for an easy conversion of current ranges from 5µA to 750µA full scale. The LMP91002's transimpedance amplifier (TIA) gain is programmable through the I2C interface. The I2C interface can also be used for sensor diagnostics. The LMP91002 is optimized for micro-power applications and operates over a voltage range of 2.7V to 3.6V. The total current consumption can be less than 10µA. Further power savings are possible by switching off the TIA amplifier and shorting the reference electrode to the working electrode with an internal switch.

Typical Application

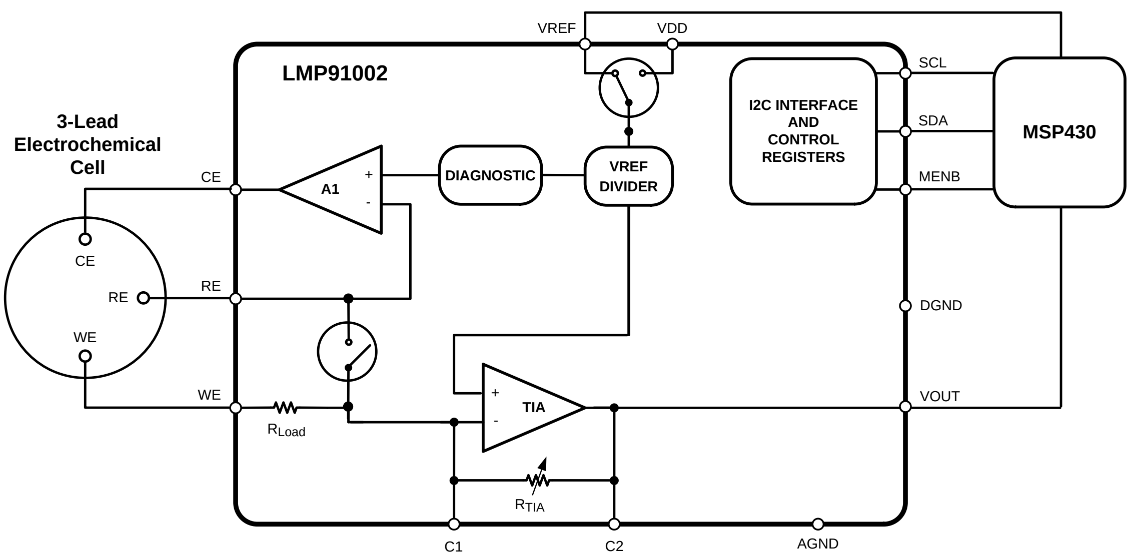


Figure 1. AFE Gas Detector

Connection Diagram

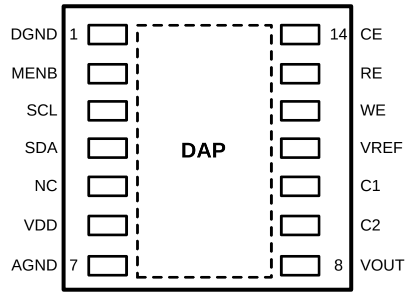


Figure 2. 14–Pin WSON – Top View
See Package Number NHL0014B

PIN DESCRIPTIONS

Pin	Name	Description
1	DGND	Connect to ground
2	MENB	Module Enable, Active Low
3	SCL	Clock signal for I^2C compatible interface
4	SDA	Data for I^2C compatible interface
5	NC	Not Internally Connected
6	VDD	Supply Voltage
7	AGND	Ground
8	VOUT	Analog Output
9	C2	External filter connector (Filter between C1 and C2)
10	C1	External filter connector (Filter between C1 and C2)
11	VREF	Voltage Reference input
12	WE	Working Electrode. Output to drive the Working Electrode of the chemical sensor
13	RE	Reference Electrode. Input to drive Counter Electrode of the chemical sensor
14	CE	Counter Electrode. Output to drive Counter Electrode of the chemical sensor
	DAP	Connect to AGND

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

ESD Tolerance[4]	Human Body Model	2kV
	Charge-Device Model	1kV
	Machine Model	200V
Voltage between any two pins		6.0V
Current through VDD or VSS		50mA
Current sunk and sourced by CE pin		10mA
Current out of other pins[5]		5mA
Storage Temperature Range		-65°C to 150°C
Junction Temperature[6]		150°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) For soldering specifications, see www.ti.com/lit/SNOA549.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field- Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(5) All non-power pins of this device are protected against ESD by snapback devices. Voltage at such pins will rise beyond absmax if current is forced into pin.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ All numbers apply for packages soldered directly onto a PC board.

Operating Ratings[1]

Supply Voltage V_S = (VDD - AGND)		2.7V to 3.6V
Temperature Range[2]		-40°C to 85°C
Package Thermal Resistance[2]	14-Pin WSON (θ_{JA})	44 °C/W

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ All numbers apply for packages soldered directly onto a PC board.

Electrical Characteristics (1)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_S= (V_{DD} – AGND), V_S= 3.3V and AGND = DGND = 0V, V_{REF} = 2.5V, Internal Zero = 20% V_{REF}. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
Power Supply Specification						
I_S	Supply Current	3-lead amperometric cell mode MODECN = 0x03		10	**15** 13.5	µA
		Standby mode MODECN = 0x02		6.5	**10** 8	
		Deep Sleep mode MODECN = 0x00		0.6	**1** 0.85	
Potentiostat						
I_{RE}	Input bias current at RE pin	VDD=2.7V; Internal Zero 50% VDD	-90 **-800**		90 **800**	pA
		VDD=3.6V; Internal Zero 50% VDD	-90 **-900**		90 **900**	
I_{CE}	Minimum operating current capability	sink		750		µA
		source		750		
	Minimum charging capability (4)	sink		10		mA
		source		10		
AOL_A1	Open loop voltage gain of control loop op amp (A1)	300mV≤VCE≤Vs-300mV, -750µA≤ICE≤750µA	**104**	120		dB
en_RW	Low Frequency integrated noise between RE pin and WE pin	0.1Hz to 10Hz (5)		3.4		µVpp
V_{OS_RW}	WE Voltage Offset referred to RE	0% VREF, Internal Zero=20% VREF	**-550**		**550**	µV
		0% VREF, Internal Zero=50% VREF				
		0% VREF, Internal Zero=67% VREF				
TcV_{OS_RW}	WE Voltage Offset Drift referred to RE from -40°C to 85°C (6)	0% VREF, Internal Zero=20% VREF	-4		4	µV/°C
		0% VREF, Internal Zero=50% VREF				
		0% VREF, Internal Zero=67% VREF				
TIA_GAIN	Transimpedance gain accuracy			5		%
	Linearity			±0.05		%
	Programmable TIA Gains	7 programmable gain resistors		2.75 3.5 7 14 35 120 350		kΩ
		Maximum external gain resistor		350		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) At such currents no accuracy of the output voltage can be expected.
(5) This parameter includes both A1 and TIA's noise contribution.
(6) Offset voltage temperature drift is determined by dividing the change in VOS at the temperature extremes by the total temperature change.Starting from the measured voltage offset at temperature T1 (V_{OS_RW}(T1)), the voltage offset at temperature T2 (V_{OS_RW}(T2)) is calculated according the following formula: $V_{OS\_RW}(T2)=V_{OS\_RW}(T1)+ABS(T2–T1)* TcV_{OS\_RW}$.

Electrical Characteristics(1) (continued)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_S= (V_{DD} – AGND), V_S= 3.3V and AGND = DGND = 0V, V_{REF} = 2.5V, Internal Zero = 20% V_{REF}. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min(2)	Typ(3)	Max(2)	Units
TIA_ZV	Internal zero voltage	3 programmable percentages of VREF			20 50 67		%
		3 programmable percentages of VDD			20 50 67		%
	Internal zero voltage Accuracy				±0.04		%
RL	Load Resistor				10		Ω
	Load accuracy				5		%
PSRR	Power Supply Rejection Ratio at RE pin	2.7 ≤VDD≤5.25V	Internal zero 20% VREF	80	110		dB
			Internal zero 50% VREF				
			Internal zero 67% VREF				
External reference specification(7)							
VREF	External Voltage reference range			1.5		VDD	V
	Input impedance				10		MΩ

(7) In case of external reference connected, the noise of the reference has to be added.

I²C Interface(1)

Unless otherwise specified, all limits guaranteed for at T_A = 25°C, V_S=(VDD – AGND), 2.7V <V_S< 3.6V and AGND = DGND =0V, VREF= 2.5V. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
V_{IH}	Input High Voltage		**0.7*VDD**			V
V_{IL}	Input Low Voltage				**0.3*VDD**	V
V_{OL}	Output Low Voltage	I_{OUT}=3mA			**0.4**	V
	Hysteresis(4)		**0.1*VDD**			V
C_{IN}	Input Capacitance on all digital pins			**0.5**		pF

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) This parameter is guaranteed by design or characterization.

Timing Characteristics[1]

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_S= (VDD – AGND), V_S= 3.3V and AGND = DGND = 0V, VREF = 2.5V, Internal Zero= 20% VREF. **Boldface** limits apply at the temperature extremes. Refer to timing diagram in Figure 3.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	Clock Frequency		**10**		**100**	kHz
t_{LOW}	Clock Low Time		**4.7**			µs
t_{HIGH}	Clock High Time		**4.0**			µs
$t_{HD;STA}$	Data valid	After this period, the first clock pulse is generated	**4.0**			µs
$t_{SU;STA}$	Set-up time for a repeated START condition		**4.7**			µs
$t_{HD;DAT}$	Data hold time[2]		**0**			ns
$t_{SU;DAT}$	Data Setup time		**250**			ns
t_f	SDA fall time[3]	IL ≤ 3mA, CL ≤ 400pF			**250**	ns
$t_{SU;STO}$	Set-up time for STOP condition		**4.0**			µs
t_{BUF}	Bus free time between a STOP and START condition		**4.7**			µs
$t_{VD;DAT}$	Data valid time				**3.45**	µs
$t_{VD;ACK}$	Data valid acknowledge time				**3.45**	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter[3]				**50**	ns
t_timeout	SCL and SDA Timeout		**25**		**100**	ms
$t_{EN;START}$	I^2C Interface Enabling		**600**			ns
$t_{EN;STOP}$	I^2C Interface Disabling		**600**			ns
$t_{EN;HIGH}$	time between consecutive I^2C interface enabling and disabling		**600**			ns

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) LMP91002 provides an internal 300ns minimum hold time to bridge the undefined region of the falling edge of SCL.
(3) This parameter is guaranteed by design or characterization.

Timing Diagram

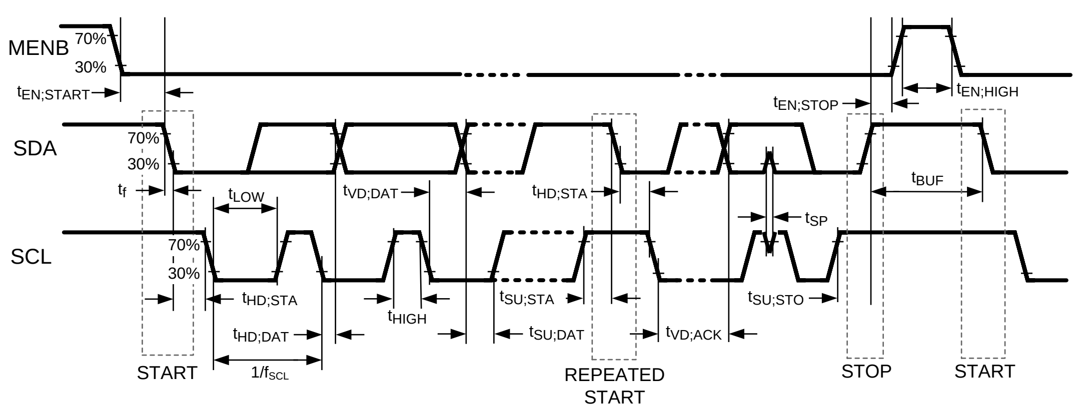


Figure 3. I^2C Interface Timing Diagram

Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V_S=(VDD – AGND), 2.7V <V_S< 3.6V and AGND = DGND =0V, VREF= 2.5V.

Input V_{OS_RW} vs. temperature

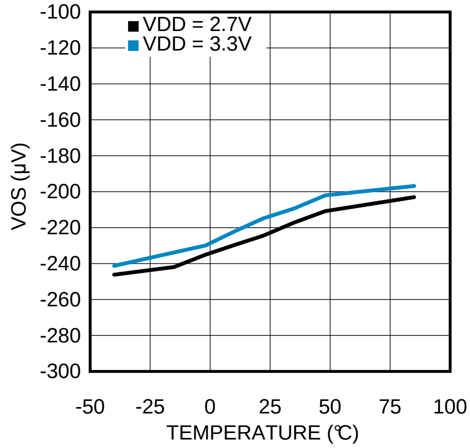


Figure 4.

Input V_{OS_RW} vs. VDD

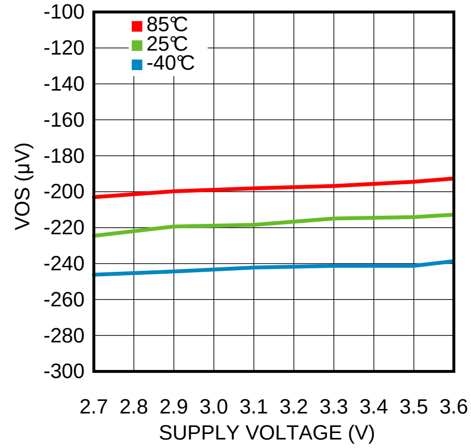


Figure 5.

I_{WE} Step current response (rise)

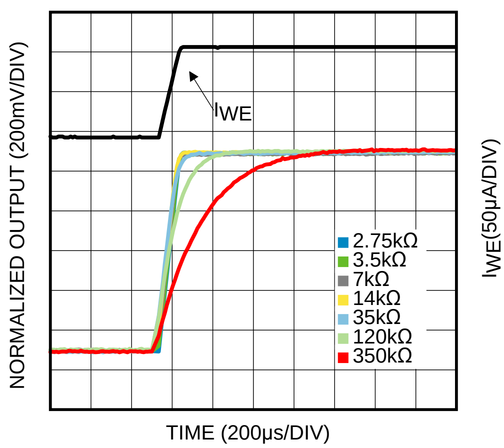


Figure 6.

I_{WE} Step current response (fall)

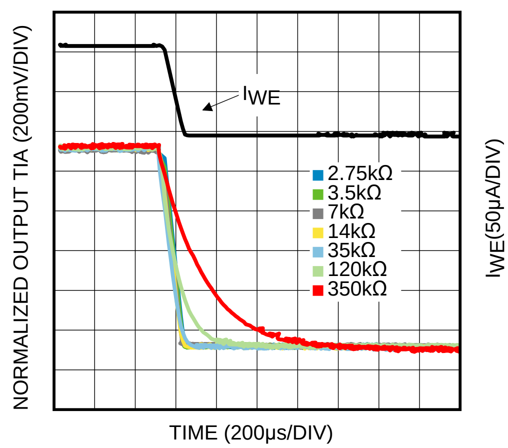


Figure 7.

AC PSRR vs. Frequency

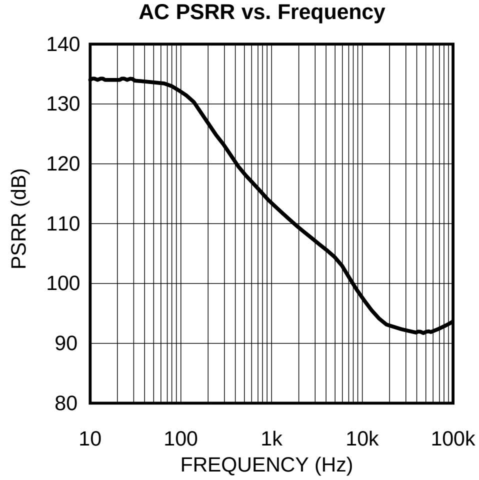


Figure 8.

Supply current vs. temperature (Deep Sleep Mode)

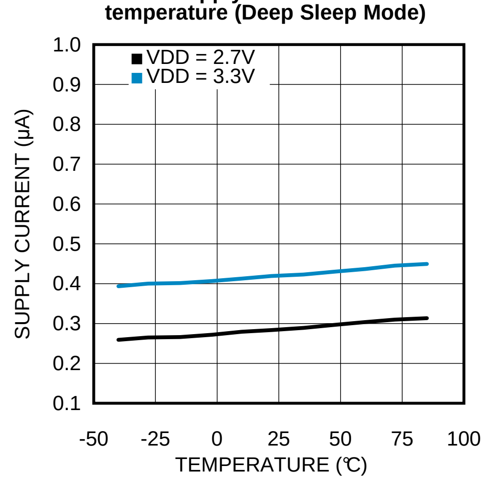


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_S=(VDD – AGND), 2.7V <V_S< 3.6V and AGND = DGND =0V, VREF= 2.5V.

Supply current vs.
VDD (Deep Sleep Mode)

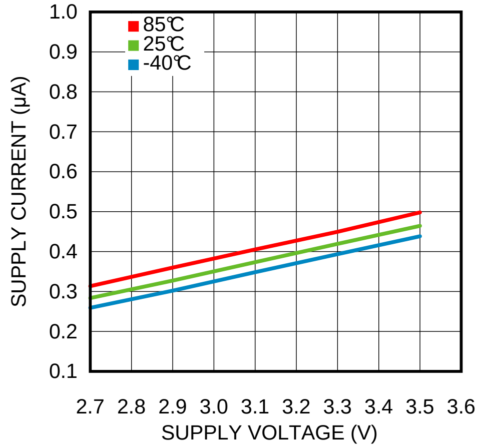


Figure 10.

Supply current vs.
temperature (Standby Mode)

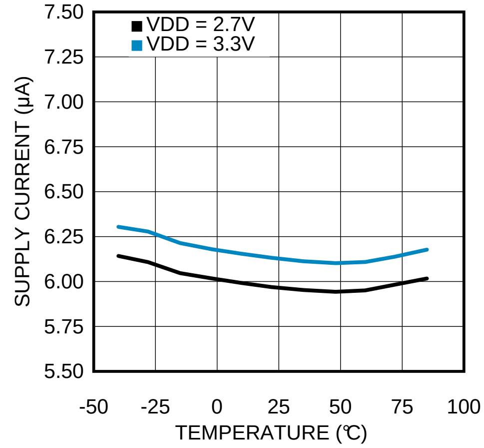


Figure 11.

Supply current vs.
VDD (Standby Mode)

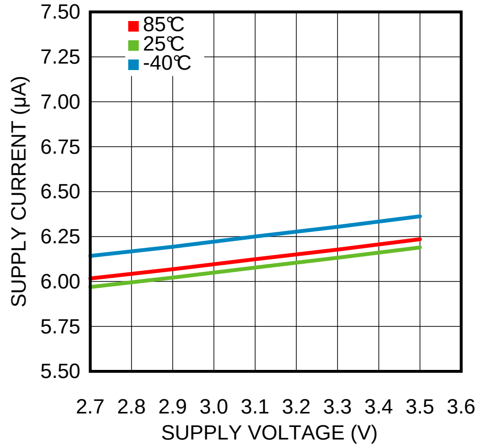


Figure 12.

Supply current vs.
temperature (3-lead amperometric Mode)

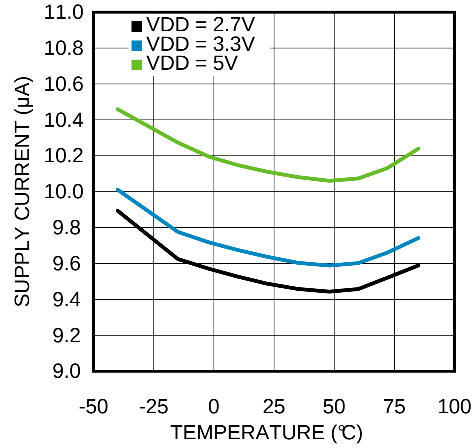


Figure 13.

Supply current vs.
VDD (3-lead amperometric Mode)

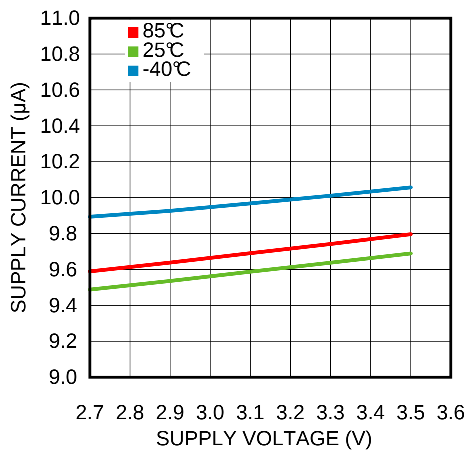


Figure 14.

0.1Hz to 10Hz noise

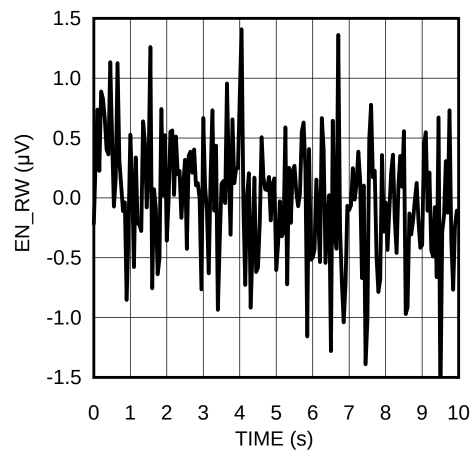


Figure 15.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_S=(VDD – AGND), 2.7V <V_S< 3.6V and AGND = DGND =0V, VREF= 2.5V.

A VOUT step response 100 ppm to 400 ppm CO (CO gas sensor connected to LMP91002)

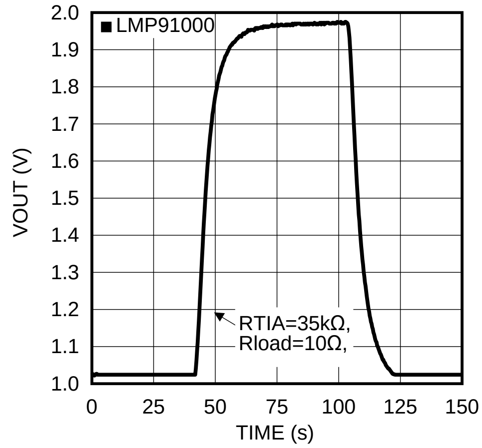


Figure 16.

Function Description

GENERAL

The LMP91002 is a programmable AFE for use in micropower chemical sensing applications. The LMP91002 is designed for 3-lead not biased gas sensors and for 2 leads galvanic cell. This device provides all of the functionality for detecting changes in gas concentration based on a delta current at the working electrode. The LMP91002 generates an output voltage proportional to the cell current. Transimpedance gain is user programmable through an I^2C compatible interface from 2.75kΩ to 350kΩ making it easy to convert current ranges from 5µA to 750µA full scale. Optimized for micro-power applications, the LMP91002 AFE works over a voltage range of 2.7V to 3.6 V. The cell voltage is user selectable using the on board programmability. In addition, it is possible to connect an external transimpedance gain resistor. Depending on the configuration, total current consumption for the device can be less than 10µA. For power savings, the transimpedance amplifier can be turned off and instead a load impedance equivalent to the TIA's inputs impedance is switched in.

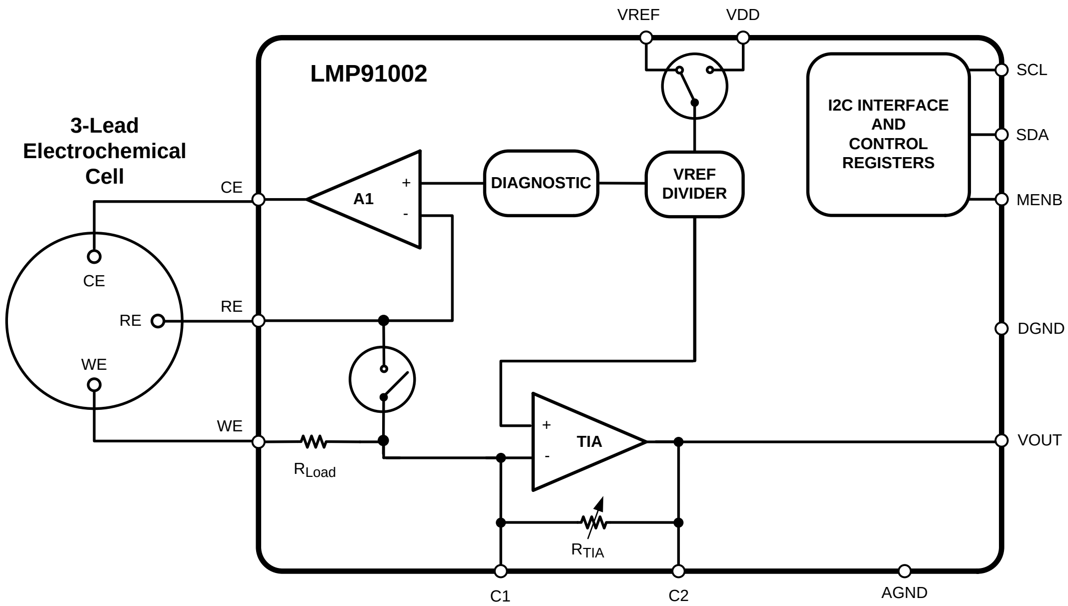


Figure 17. System Block Diagram

POTENTIOSTAT CIRCUITRY

The core of the LMP91002 is a potentiostat circuit. It consists of a differential input amplifier used to compare the potential between the working and reference electrodes to a zero bias potential.. The error signal is amplified and applied to the counter electrode (through the **Control Amplifier** - **A1**). Any changes in the impedance between the working and reference electrodes will cause a change in the voltage applied to the counter electrode, in order to maintain the constant voltage between working and reference electrodes. A **Transimpedance Amplifier** connected to the working electrode, is used to provide an output voltage that is proportional to the cell current. The working electrode is held at virtual ground (**Internal ground**) by the transimpedance amplifier. The potentiostat will compare the reference voltage to the desired bias potential and adjust the voltage at the counter electrode to maintain the proper working-to-reference voltage.

Transimpedance amplifier

The transimpedance amplifier (TIA in Figure 17) has 7 programmable internal gain resistors. This accommodates the full scale ranges of most existing sensors. Moreover an external gain resistor can be connected to the LMP91002 between C1 and C2 pins. The gain is set through the I^2C interface.

Control amplifier

The control amplifier (A1 op amp in Figure 17) provides initial charge to the sensor. A1 has the capability to drive up to 10mA into the sensor in order to to provide a fast initial conditioning. A1 is able to sink and source current according to the connected gas sensor (reducing or oxidizing gas sensor). It can be powered down to reduce system power consumption. However powering down A1 is not recommended, as it may take a long time for the sensor to recover from this situation.

Internal zero

The internal Zero is the voltage at the non-inverting pin of the TIA. The internal zero can be programmed to be either 67%, 50% or 20%, of the supply, or the external reference voltage. This provides both sufficient headroom for the counter electrode of the sensor to swing, in case of sudden changes in the gas concentration, and best use of the ADC’s full scale input range.

The Internal zero is provided through an internal voltage divider (Vref divider box in Figure 17). The divider is programmed through the I^2C interface.

I^2C INTERFACE

The I^2C compatible interface operates in Standard mode (100kHz). Pull-up resistors or current sources are required on the SCL and SDA pins to pull them high when they are not being driven low. A logic zero is transmitted by driving the output low. A logic high is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The LMP91002 comes with a 7 bit bus fixed address: 1001 000.

WRITE AND READ OPERATION

In order to start any read or write operation with the LMP91002, MENB needs to be set low during the whole communication. Then the master generates a start condition by driving SDA from high to low while SCL is high. The start condition is always followed by a 7-bit slave address and a Read/Write bit. After these 8 bits have been transmitted by the master, SDA is released by the master and the LMP91002 either ACKs or NACKs the address. If the slave address matches, the LMP91002 ACKs the master. If the address doesn't match, the LMP91002 NACKs the master. For a write operation, the master follows the ACK by sending the 8-bit register address pointer. Then the LMP91002 ACKs the transfer by driving SDA low. Next, the master sends the 8-bit data to the LMP91002. Then the LMP91002 ACKs the transfer by driving SDA low. At this point the master should generate a stop condition and optionally set the MENB at logic high level (refer to Figure 20).

A read operation requires the LMP91002 address pointer to be set first, also in this case the master needs setting at low logic level the MENB, then the master needs to write to the device and set the address pointer before reading from the desired register. This type of read requires a start, the slave address, a write bit, the address pointer, a Repeated Start (if appropriate), the slave address, and a read bit (refer to Figure 20). Following this sequence, the LMP91002 sends out the 8-bit data of the register.

When just one LMP91002 is present on the I^2C bus the MENB can be tied to ground (low logic level).

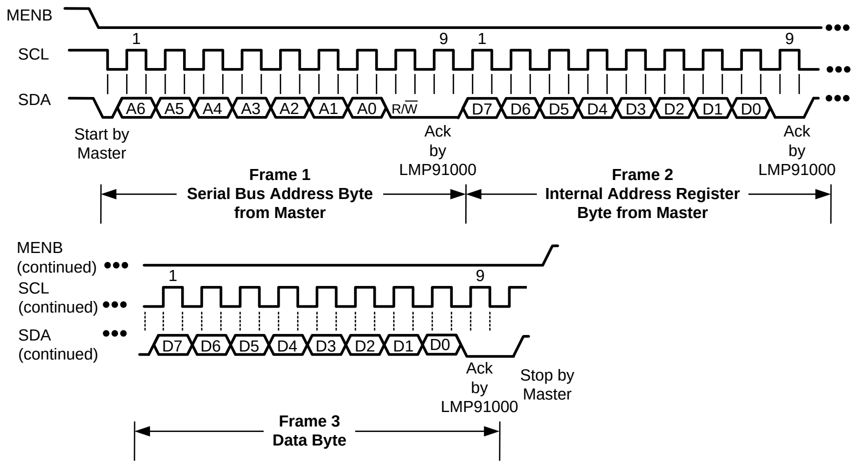


Figure 18. (a) Register write transaction

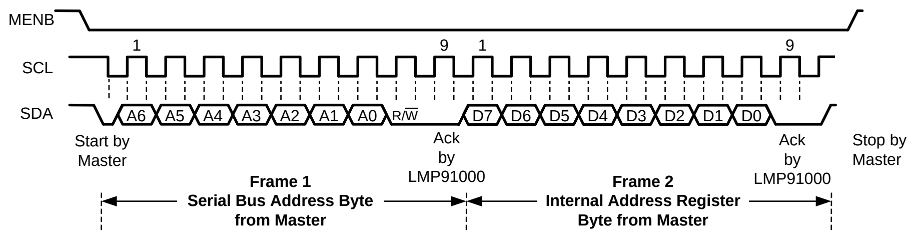
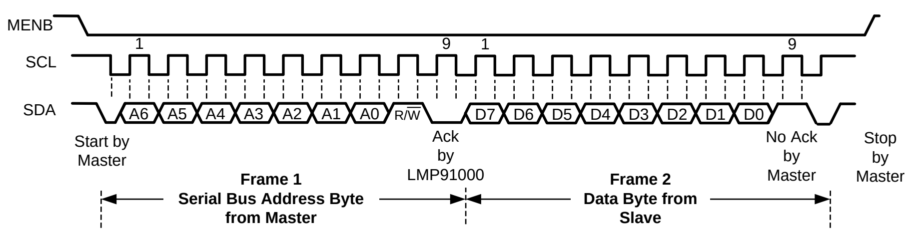


Figure 19. (b) Pointer set transaction



(c) Register read transaction

Figure 20. READ and WRITE transaction

TIMEOUT FEATURE

The timeout is a safety feature to avoid bus lockup situation. If SCL is stuck low for a time exceeding t_timeout, the LMP91002 will automatically reset its I^{2}C interface. Also, in the case the LMP91002 hangs the SDA for a time exceeding t_timeout, the LMP91002's I^{2}C interface will be reset so that the SDA line will be released. Since the SDA is an open-drain with an external resistor pull-up, this also avoids high power consumption when LMP91002 is driving the bus and the SCL is stopped.

REGISTERS

The registers are used to configure the LMP91002.

If writing to a reserved bit, user must write only 0. Readback value is unspecified and should be discarded.

Table 1. Register Map

Address	Name	Power on default	Access	Lockable?
0x00	STATUS	0x00	Read only	N
0x01	LOCK	0x01	R/W	N
0x02 through 0x09	RESERVED			
0x10	TIACN	0x03	R/W	Y
0x11	REFCN	0x20	R/W	Y
0x12	MODECN	0x00	R/W	N
0x13 through 0xFF	RESERVED			

STATUS -- Status Register (address 0x00)

The status bit is an indication of the LMP91002's power-on status. If its readback is “0”, the LMP91002 is not ready to accept other I^2C commands.

Bit	Name	Function
[7:1]	RESERVED	
0	STATUS	Status of Device **0 Not Ready (default)** 1 Ready

LOCK -- Protection Register (address 0x01)

The lock bit enables and disables the writing of the TIACN and the REFCN registers. In order to change the content of the TIACN and the REFCN registers the lock bit needs to be set to “0”.

Bit	Name	Function
[7:1]	RESERVED	
0	LOCK	Write protection 0 Registers 0x10, 0x11 in write mode **1 Registers 0x10, 0x11 in read only mode (default)**

TIACN -- TIA Control Register (address 0x10)

The parameters in the TIA control register allow the configuration of the transimpedance gain (R_{TIA}).

Bit	Name	Function
[7:5]	RESERVED	RESERVED
[4:2]	TIA_GAIN	TIA feedback resistance selection **000 External resistance (default)** 001 2.75kΩ 010 3.5kΩ 011 7kΩ 100 14kΩ 101 35kΩ 110 120kΩ 111 350kΩ
[1:0]	RESERVED	RESERVED

REFCN -- Reference Control Register (address 0x11)

The parameters in the Reference control register allow the configuration of the Internal zero, and Reference source. When the Reference source is external, the reference is provided by a reference voltage connected to the VREF pin. In this condition the Internal Zero is defined as a percentage of VREF voltage instead of the supply voltage.

Bit	Name	Function
7	REF_SOURCE	Reference voltage source selection **0 Internal (default)** 1 external
[6:5]	INT_Z	Internal zero selection (Percentage of the source reference) 00 20% **01 50% (default)** 10 67%
[4]	RESERVED	RESERVED
[3:0]	DIAGNOSTIC	Diagnostic step (Percentage of the source reference) **0000 0% (default)** 0001 1%

MODECN -- Mode Control Register (address 0x12)

The Parameters in the Mode register allow the configuration of the Operation Mode of the LMP91002.

Bit	Name	Function
7	FET_SHORT	Shorting FET feature **0 Disabled (default)** 1 Enabled
[6:3]	RESERVED	RESERVED
[2:0]	OP_MODE	Mode of Operation selection **000 Deep Sleep (default)** 010 Standby 011 3-lead amperometric cell

GAS SENSOR INTERFACE

The LMP91002 supports both 3-lead and 2-lead gas sensors. Most of the toxic gas sensors are amperometric cells with 3 leads (Counter, Worker and Reference). These leads should be connected to the LMP91002 in the potentiostat topology.

3-lead Amperometric Cell In Potentiostat Configuration

Most of the amperometric cell have 3 leads (Counter, Reference and Working electrodes). The interface of the 3-lead gas sensor to the LMP91002 is straightforward, the leads of the gas sensor need to be connected to the namesake pins of the LMP91002.

The LMP91002 is then configured in 3-lead amperometric cell mode; in this configuration the Control Amplifier (A1) is ON and provides the internal zero voltage and bias in case of biased gas sensor. The transimpedance amplifier (TIA) is ON, it converts the current generated by the gas sensor in a voltage, according to the transimpedance gain:

Gain = R_{TIA}

If different gains are required, an external resistor can be connected between the pins C1 and C2. In this case the internal feedback resistor should be programmed to “external”. The R_{Load} together with the output capacitance of the gas sensor acts as a low pass filter.

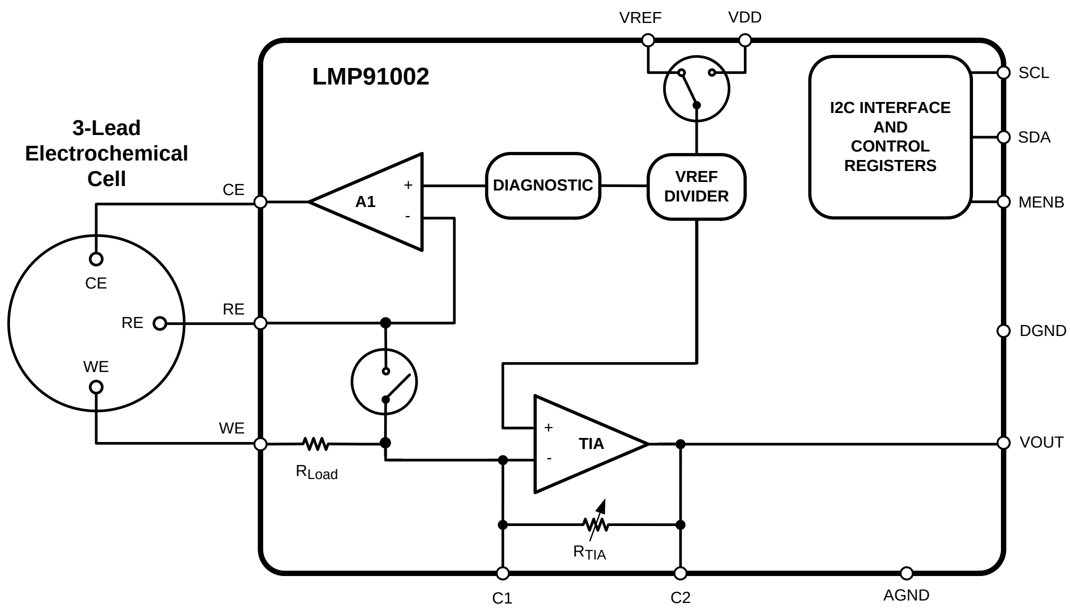


Figure 21. 3-Lead Amperometric Cell

2-lead Galvanic Cell in Potentiostat Configuration

When the LMP91002 is interfaced to a galvanic cell (for instance to an Oxygen gas sensor) referred to a reference, the Counter and the Reference pin of the LMP91002 are shorted together and connected to negative electrode of the galvanic cell. The positive electrode of the galvanic cell is then connected to the Working pin of the LMP91002.

The LMP91002 is then configured in 3-lead amperometric cell mode (as for amperometric cell). In this configuration the Control Amplifier (A1) is ON and provides the internal zero voltage. The transimpedance amplifier (TIA) is also ON, it converts the current generated by the gas sensor in a voltage, according to the transimpedance gain:

Gain= R_{TIA}

If different gains are required, an external resistor can be connected between the pins C1 and C2. In this case the internal feedback resistor should be programmed to “external”.

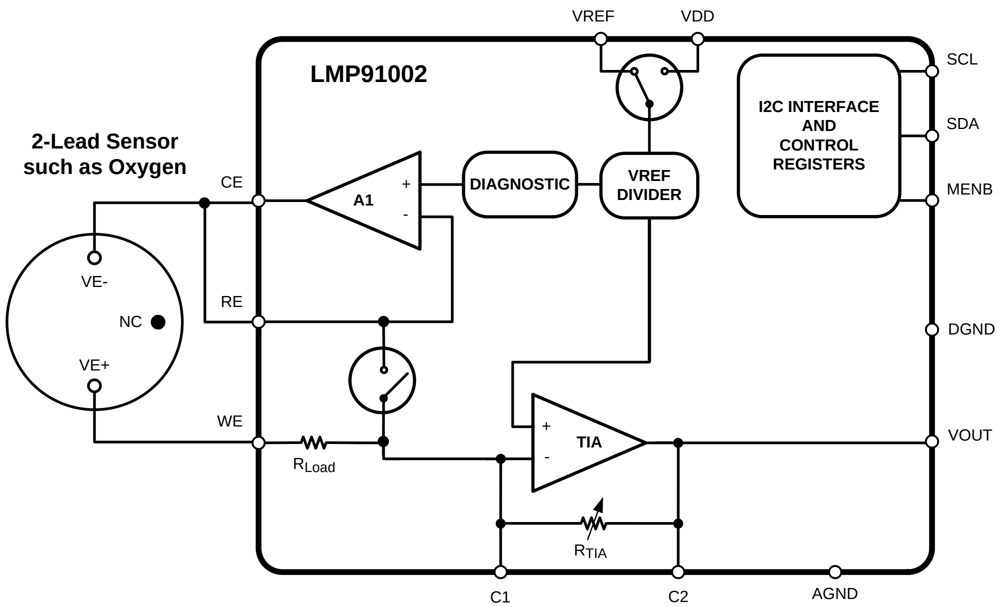


Figure 22.

APPLICATION INFORMATION

CONNECTION OF MORE THAN ONE LMP91002 TO THE I²C BUS

The LMP91002 comes out with a unique and fixed I²C slave address. It is still possible to connect more than one LMP91002 to an I²C bus and select each device using the MENB pin. The MENB simply enables/disables the I²C communication of the LMP91002. When the MENB is at logic level low all the I²C communication is enabled, it is disabled when MENB is at high logic level.

In a system based on a µcontroller and more than one LMP91002 connected to the I²C bus, the I²C lines (SDA and SCL) are shared, while the MENB of each LMP91002 is connected to a dedicate GPIO port of the µcontroller.

The µcontroller starts communication asserting one out of N MENB signals where N is the total number of LMP91002s connected to the I²C bus. Only the enabled device will acknowledge the I²C commands. After finishing communicating with this particular LMP91002, the microcontroller de-asserts the corresponding MENB and repeats the procedure for other LMP91002s. Figure 23 shows the typical connection when more than one LMP91002 is connected to the I²C bus.

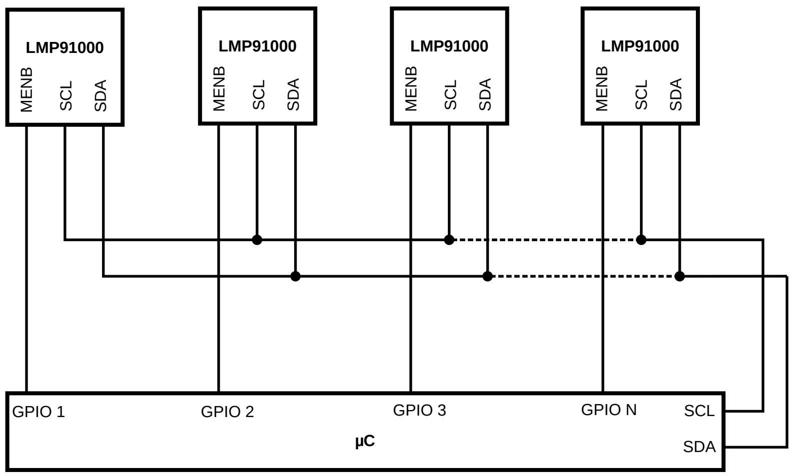


Figure 23. More than one LMP91002 on I²C bus

SMART GAS SENSOR ANALOG FRONT END

The LMP91002 together with an external EEPROM represents the core of a SMART GAS SENSOR AFE. In the EEPROM it is possible to store the information related to the GAS sensor type, calibration and LMP91002's configuration (content of registers 10h, 11h, 12h). At startup the microcontroller reads the EEPROM's content and configures the LMP91002. A typical smart gas sensor AFE is shown in Figure 24. The connection of MENB to the hardware address pin A0 of the EEPROM allows the microcontroller to select the LMP91002 and its corresponding EEPROM when more than one smart gas sensor AFE is present on the I²C bus. Note: only EEPROM I²C addresses with A0=0 should be used in this configuration.

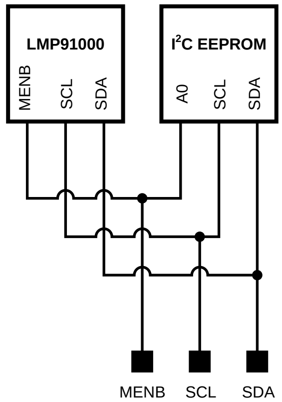


Figure 24. SMART GAS SENSOR AFE

SMART GAS SENSOR AFES ON I^2C BUS

The connection of Smart gas sensor AFEs on the I^2C bus is the natural extension of the previous concepts. Also in this case the microcontroller starts communication asserting 1 out of N MENB signals where N is the total number of smart gas sensor AFE connected to the I^2C bus. Only one of the devices (either LMP91002 or its corresponding EEPROM) in the smart gas sensor AFE enabled will acknowledge the I^2C commands. When the communication with this particular module ends, the microcontroller de-asserts the corresponding MENB and repeats the procedure for other modules. Figure 25 shows the typical connection when several smart gas sensor AFEs are connected to the I^2C bus.

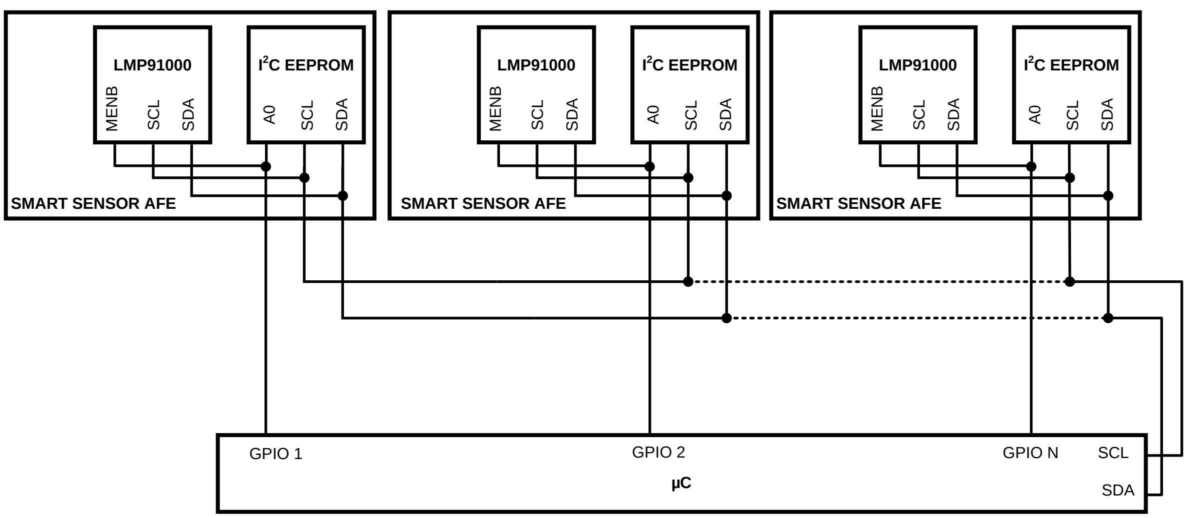


Figure 25. SMART GAS SENSOR AFEs on I^2C bus

POWER CONSUMPTION

The LMP91002 is intended for use in portable devices, so the power consumption is as low as possible in order to guarantee a long battery life. The total power consumption for the LMP91002 is below 10µA @ 3.3v average over time, (this excludes any current drawn from any pin). A typical usage of the LMP91002 is in a portable gas detector and its power consumption is summarized in Table 2. This has the following assumptions:

-Power On only happens a few times over life, so its power consumption can be ignored

-Deep Sleep mode is not used

-The system is used about 8 hours a day, and 16 hours a day it is in Standby mode.

This results in an average power consumption of approximately 7.8 µA. This can potentially be further reduced, by using the Standby mode between gas measurements. It may even be possible, depending on the sensor used, to go into deep sleep for some time between measurements, further reducing the average power consumption.

Table 2. Power Consumption Scenario

	Deep Sleep	StandBy	3-Lead Amperometric Cell	Total
Current consumption (µA) typical value	0.6	6.5	10	
Time ON (%)	0	60	39	
Average (µA)	0	3.9	3.9	7.8
Notes				
A1	OFF	ON	ON	
TIA	OFF	OFF	ON	
I^2C interface	ON	ON	ON	

SENSOR TEST PROCEDURE

The LMP91002 has all the hardware and programmability features to implement some test procedures. The purpose of the test procedure is to:

a) test proper function of the sensor (status of health)

b) test proper connection of the sensor to the LMP91002

The test procedure is very easy. The diagnostic block is user programmable through the digital interface. A step voltage can be applied by the end user to the positive input of A1. As a consequence a transient current will start flowing into the sensor (to charge its internal capacitance) and it will be detected by the TIA. If the current transient is not detected, either a sensor fault or a connection problem is present. The slope and the aspect of the transient response can also be used to detect sensor aging (for example, a cell that is drying and no longer efficiently conducts the current). After it is verified that the sensor is working properly, the LMP91002 needs to be reset to its original configuration. It is not required to observe the full transient in order to contain the testing time. All the needed information are included in the transient slopes (both edges). Figure 26 shows an example test procedure, a Carbon Monoxide sensor is connected to the LMP91002, a 25mVpp pulse is applied between Reference and Working pin.

The following procedure shows how to implement the sensor test. Preliminary conditions:

The LMP91002 is unlocked and it is in 3-Lead Amperometric Cell Mode

1. Put in the [3:0] bit of the register REFCN (0x11) the 0001b value, leaving the other bit unchanged. This operation will apply a potential (V_{RW}) between RE and WE pin ($V_{RE} > V_{WE}$), V_{RW}= 1% Source reference
2. Put in the [3:0] bit of the register REFCN (0x11) the 0000b value, leaving the other bit unchanged. This operation will remove the potential (V_{RW}) between RE and WE pin ($V_{RE} > V_{WE}$), V_{RW}= 0V.

The width of the pulse is simply the time between the two writing operation.

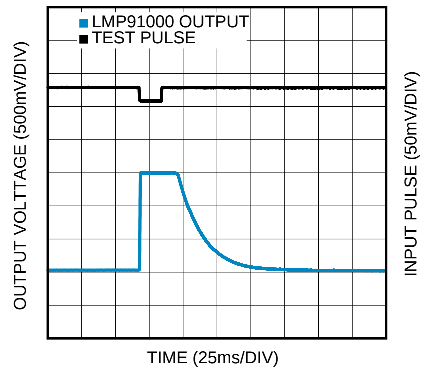


Figure 26. TEST PROCEDURE EXAMPLE

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP91002SD/NOPB	ACTIVE	WSON	NHL	14	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L91002	Samples
LMP91002SDE/NOPB	ACTIVE	WSON	NHL	14	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L91002	Samples
LMP91002SDX/NOPB	ACTIVE	WSON	NHL	14	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L91002	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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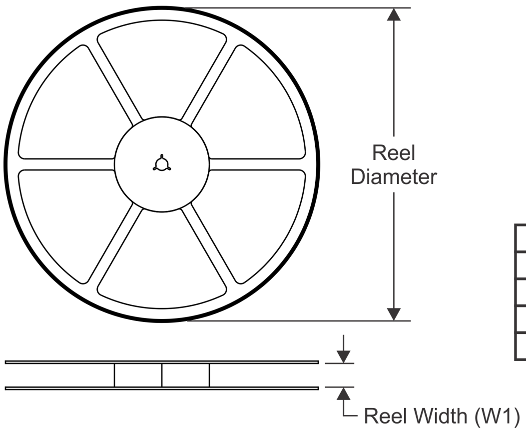
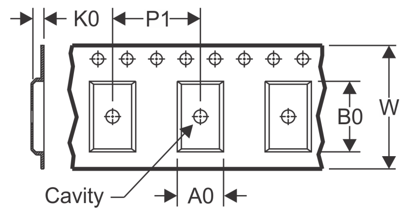
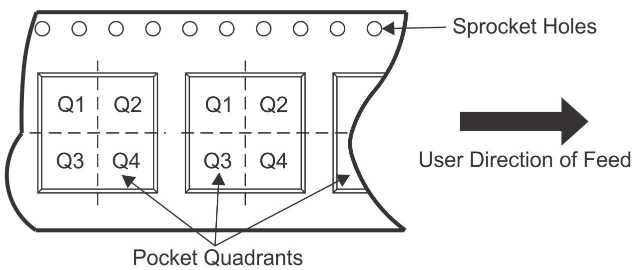
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

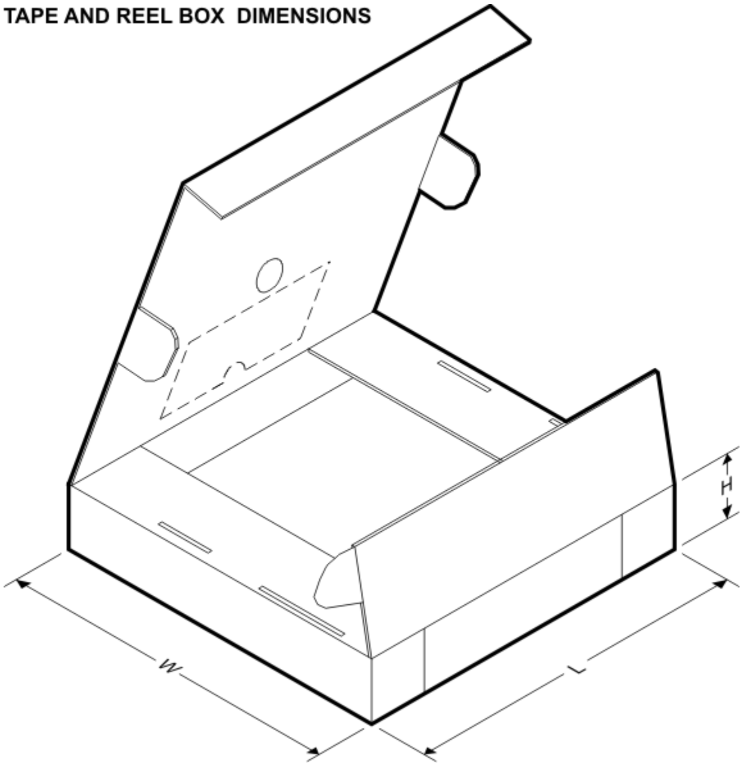
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP91002SD/NOPB	WSON	NHL	14	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMP91002SDE/NOPB	WSON	NHL	14	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMP91002SDX/NOPB	WSON	NHL	14	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

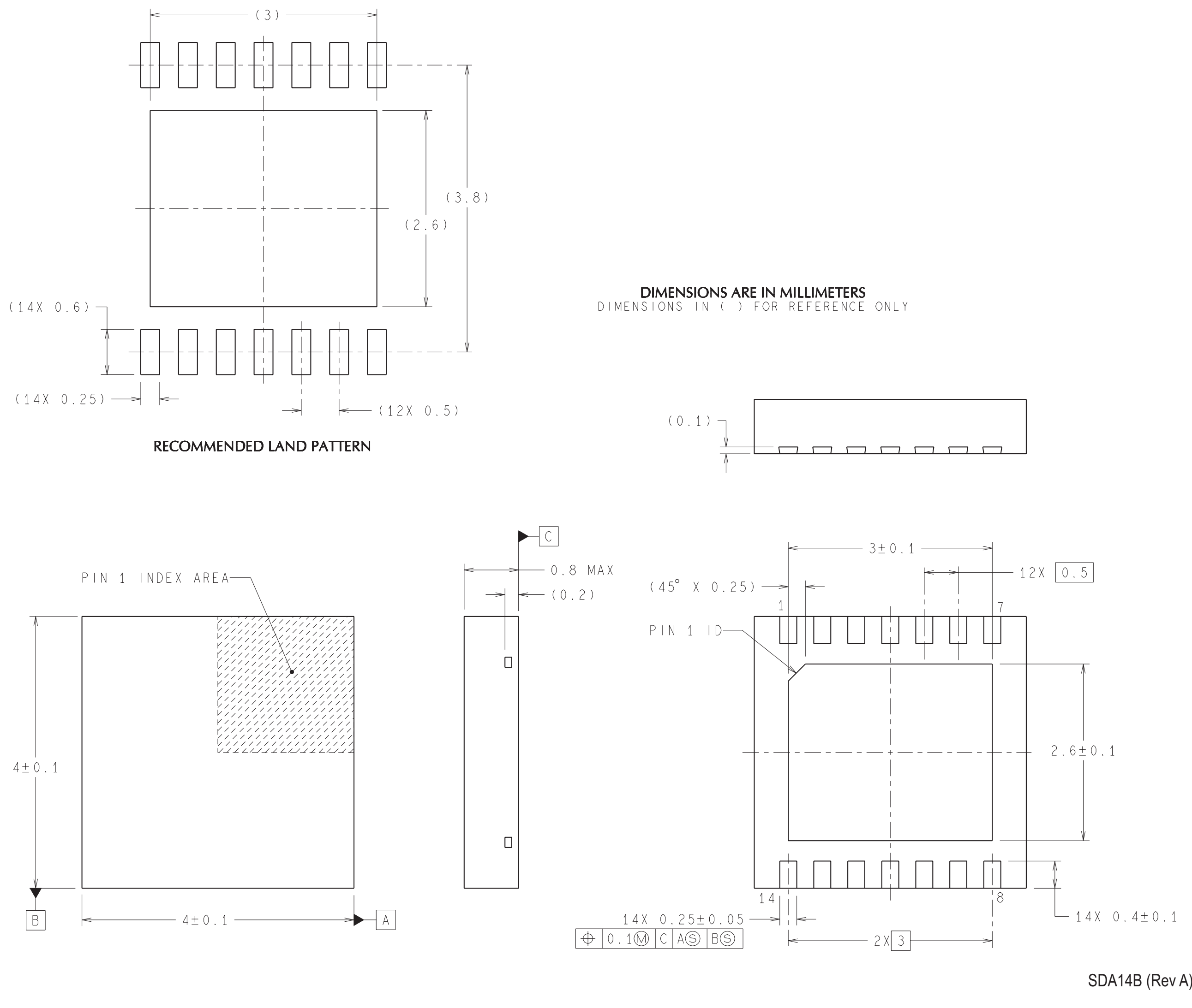
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP91002SD/NOPB	WSON	NHL	14	1000	203.0	190.0	41.0
LMP91002SDE/NOPB	WSON	NHL	14	250	203.0	190.0	41.0
LMP91002SDX/NOPB	WSON	NHL	14	4500	358.0	343.0	63.0

NHL0014B


(3)
(3.8)
(2.6)
(14X 0.6)
(14X 0.25)
(12X 0.5)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
C
0.8 MAX
(0.2)
PIN 1 INDEX AREA
4±0.1
B
4±0.1
A
3±0.1
12X 0.5
(45° X 0.25)
1
7
PIN 1 ID
2.6±0.1
14
8
14X 0.4±0.1
14X 0.25±0.05
0.1 M C A S B S
2X 3
SDA14B (Rev A)

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