LMS202E 15KV ESD Rated, 5V Single Supply TIA/EIA-232 Dual Transceivers

Check for Samples: LMS202E

FEATURES

- **ESD Protection for RS-232 I/O Pins**
- **±15kV-IEC1000 4-2 (EN61000-4-2) Contact Discharge**
- **±8kV-IEC1000 4-2 (EN61000-4-2) Air-Gap Discharge**
- **±15kV Human Body Model**
- **Single +5V Power Supply**
- **230 Kbps Data Rate**
- **On-Board DC-to-DC Converter**
- **0.1µF Charge Pump Capacitors**
- **Drop-In Replacement to Maxim's MAX202E**

APPLICATIONS

- **POS Equipment (Bar code reader)**
- **Hand-Held Equipment**
- **General Purpose RS-232 Communication**

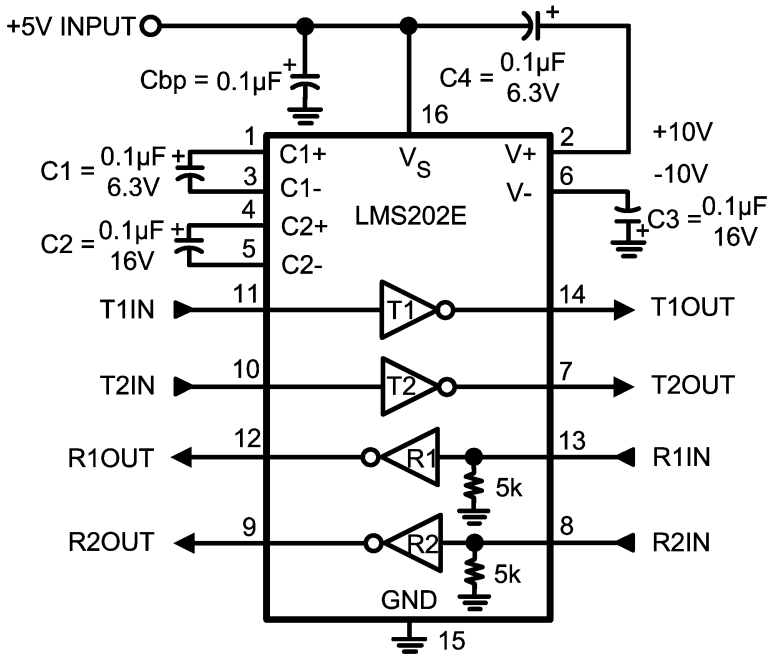
DESCRIPTION

The LMS202E features two transmitters and two receivers for RS-232 communication. It has a DC-to-DC converter that permits the device to operate with only a single +5V power supply. The on-chip DC-to-DC converter which utilizes four external 0.1µF capacitors to generate dual internal power supplies for RS-232 compatible output levels.

The device meet EIA/TIA-232E and CCITT V.28 specifications up to 230kbits/sec. The LMS202E is available in a 16 pin narrow and wide SOIC package.

The transmitter outputs and receiver inputs have ±15kV electrostatic discharge (ESD) protection. The LMS202E survives a ± 15kV ESD event to the RS-232 input and output pins when subjected according to Human Body Model or IEC 1000-4-2 (EN61000-4-2), air-gap specification. It survives a ±8kV discharge when subjected to IEC 1000-4-2 (EN61000-4-2), contact specification. This device is designed for use in harsh environments where ESD is a concern.

CONNECTION DIAGRAM AND TYPICAL CIRCUIT



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PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Function
1, 3	C1+, C1−	External capacitor connection pins. Recommended external capacitor C1 = 0.1µF (6.3V)
2	V+	Positive supply for TIA/EIA-232E drivers. Recommended external capacitor C4 = 0.1µF (6.3V)
4, 5	C2+, C2−	External capacitor connection pins. Recommended external capacitor C2 = 0.1µF (16V)
6	V−	Negative supply for TIA/EIA-232E drivers. Recommended external capacitor C3 = 0.1µF (16V)
7, 14	T1out, T2out	Transmitter output pins conform to TIA/EIA-232E levels. The typical transmitter output swing is ±8V when loaded 3kΩ load to ground. The open-circuit output voltage swings from (V+ − 0.6V) to V−
8,13	R1in, R2in	Receiver inputs accept TIA/EIA-232
9, 12	R1out and R2out	Receiver output pins are TTL/CMOS compatible
10, 11	Tin1, Tin2	Transmitter input pins are TTL/CMOS compatible. Inputs of transmitter do not have pull-up resistors. Connect all unused transmitter inputs to ground
15	GND	Ground pin
16	V_S	Power supply pin for the device, +5V (±10%)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

V_S			−0.3V to 6V
V+			(V_S − 0.3V) to + 14V
V−			+0.3V to −14V
Driver Input Voltage, T_{IN}			−0.3V to (V+ +0.3V)
Receiver Input Voltage, R_{IN}			± 30V
Driver Output Voltage T_O			(V− −0.3V to (V+ + 0.3V)
Receiver Output Voltage R_O			−0.3 to (V_S + 0.3)
Short Circuit Duration, T_O			Continuous
ESD Rating	IEC 1000-4-2) (3)	See (4)	
	Air-Gap Discharge		15kV
	Contact Discharge		8kV
	Human Body Model (5)	See (4)	15kV
		See (6)	2kV
ESD Rating (MM)			200V (7)(6)
Soldering Information	Infrared or Convection (20sec.)		235°C
Junction Temperature			150°C
Storage Temperature Range			−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) IEC 1000-4-2, 330Ω in series with 150pF
(4) ESD rating applies to pins 7,8 13 and 14
(5) Human Body Model, 1.5kΩ in series with 100pF
(6) ESD rating applies to pins 1, 2, 3, 4, 5, 6, 9, 10, 11, 12, 15 and 16
(7) Machine model, 0Ω in series with 200pF

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OPERATING RATINGS

Supply Voltage V_S		4.5V to 5.5V
Ambient Temperature Range, T_A	Commercial (C)	0°C to +70°C
	Industrial (I)	−40°C to +85°C
Package Thermal Resistance (1)		
SO		71°C/W
WSO		55°C/W

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified
C1 = C2 = C3 = C4 = Cbp = 0.1µF

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
DC Characteristics						
I_S	Supply Current	No Load, T_A = 25°C		1	7	mA
Logic						
I_{INPUT}	Input Leakage Current	T_{IN} = 0V to V_S			±10	µA
V_{THL}	Input Logic Theshold Low	T_{IN}			0.8	V
V_{THH}	Input Logic Theshold High	T_{IN}	2.0			V
V_{OL}	TTL/CMOS Output Voltage Low	R_{OUT}, I_{OUT} = 3.2mA			0.4	V
V_{OH}	TTL/CMOS Output Voltage High	R_{OUT}, I_{OUT} = −1.0mA	3.5	V_S −0.1		V
RS-232 Receiver Inputs						
V_{RI}	Receiver Input Voltage Range		−30		+30	V
V_{RTHL}	Receiver Input Theshold Low	V_S = 5V, T_A = 25°C	0.8	1.4		V
V_{RTHH}	Receiver Input Theshold High	V_S = 5V, T_A = 25°C		2	2.4	V
V_{HYST}	Receiver Input Hysteresis	V_S = 5V	0.2	0.6	1.0	V
R_I	Receiver Input Resistance	V_S = 5V, T_A = 25°C	3	5	7	kΩ
RS-232 Transmitter Outputs						
V_O	Transmitter Output Voltage Swing	All transmitters loaded with 3kΩ to GND	±5	±8		V
R_O	Output Resistance	V_S = V+ = V− = 0V, V_O = ± 2V	300			Ω
I_{OS}	Output Short Circuit Current			±11	±60	mA
Timing Characteristics						
DR	Maximum Data Rate	C_L = 50pF to 1000pF, R_L = 3kΩ to 7kΩ	230			kbps
T_{RPLH} T_{RPHL}	Receiver Propagation Delay	C_L = 150pF		0.08	1	µs
T_{DPLH} T_{DPHL}	Transmitter Propagation Delay	R_L = 3kΩ, C_L = 2500pF All transmitters loaded		2.4		µs
V_{SLEW}	Transition Region Slew Rate	T_A = 25°C, V_S = 5V C_L = 50pF to 1000pF, R_L = 3kΩ to 7kΩ Measured from +3V to −3V or vice versa	3	6	30	V/µs
ESD Performance: Transmitter Outputs and Receiver Inputs						
ESD Rating		Human Body Model		±15		kV
		IEC 1000-4-2, Contact		±8		
		IEC 1000-4-2, Air-gap		±15		

(1) All limits are specified by testing or statistical analysis
(2) Typical Values represent the most likely parametric norm.

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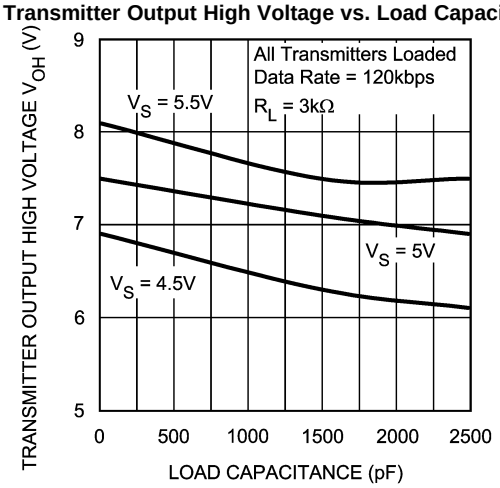
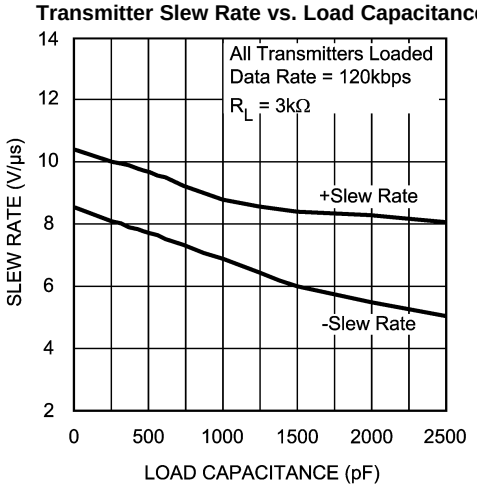
TYPICAL CHARACTERISTICS

Transmitter Output High Voltage vs. Load Capacitance



Transmitter Slew Rate vs. Load Capacitance



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APPLICATION INFORMATION

CAPACITOR SELECTION

The recommended capacitors are 0.1µF. However, larger capacitors for the charge pump may be used to minimized ripples on V+ and V− pins.

POWER SUPPLY DECOUPLING

In some applications that are sensitive to power supply noise from the charge pump, place a decoupling capacitor, Cbp, from V_S to GND. Use at least a 0.1µF capacitor or the same size as the charge pump capacitors (C1 − C4).

CHARGED PUMP

The dual internal charged-pump provides the ±10V to the to transmitters. Using capacitor C1, the charge pump converts +5V to +10V then stores the +10V in capacitor C3. The charge pump uses capacitor C2 to invert the +10V to −10V. The −10V is then stored in capacitor C4.

ELECTROSTATIC DISCHARGE PROTECTION

ESD protection has been placed at all pins to protect the device from ESD. All pins except for the transmitter output pins (pins 7 and 14) and receiver input pins (pins 8 and 13) have a ESD rating of 2kV Human Body Model (HBM) and 200V Machine Model (MM). The RS-232 bus pins (pins 7, 8, 13 and 14) have a more robust ESD protection. The RS-232 bus pins have a ESD rating of 15kV HBM and IEC 1000-4-2, air-gap. In addition the bus pins meet an ESD rating of 8kV with IEC 1000-4-2, contact. The ESD structures can withstand a high ESD event under the following conditions: powered-on, powered-off, and Input connected to high and low with outputs unloaded.

HUMAN BODY MODEL

The Human Body Model is an ESD testing standard, defined in Mil-STD-883C method 3015.7. It simulates a human discharging an ESD charge to the IC device. The rise time is approximately 10 ns and decay time is approximately 150 ns. The waveform is obtained by discharging 2kV volts capacitor through a resistor, R2 = 1.5 kΩ. The peak current is approximately 1.33A.

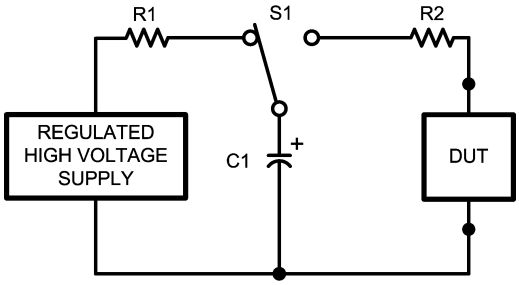

Figure 1. HBM ESD Test Model

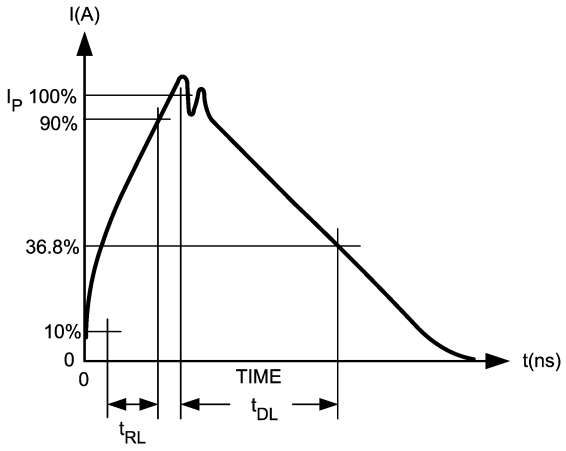

Figure 2. HBM Waveform

MACHINE MODEL

The Machine Model is the standard ESD test method in Japan and the automotive industry. It simulates a charge on large object discharging through the IC device. This takes place in automated test and handling systems. The equipment can accumulate static charge due to improper grounding, which is transmitted through the IC when it is picked and placed.

The waveform is obtained by discharging 400V volts capacitor to the device. Resistor, R2 = 0Ω.

The parasitic inductance, L, from the PCB affects the peak current and period of the waveform. For L = 0.5µF, the peak current is approximately 7A with a period of 60 ns. For L = 2.5µH, the peak current is reduced to 4A with a period of 140 ns.

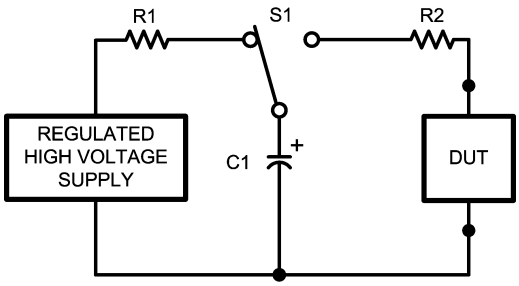

Figure 3. MM ESD Model

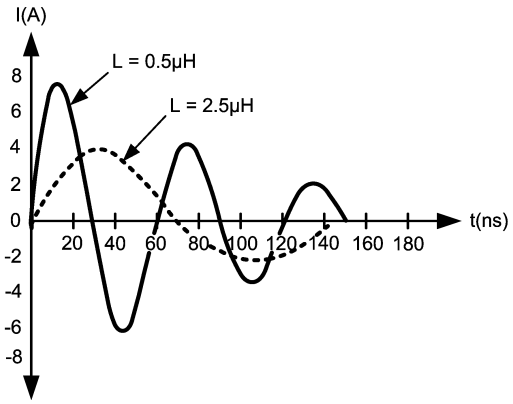

Figure 4. MM Waveform

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IEC 1000-4-2 (EN61000-4-2)

The European Union requires ESD immunity testing for all electronic products as a condition for EMC Mark before shipping to any member countries. This is not a IC requirement but an overall system requirement. IEC 1000-4-2 specifies ESD testing both by contact and air-gap discharge. ESD testing by contact are generally more repeatable than air-gap but is less realistic to actual ESD event. However, air-gap discharge is more realistic but ESD results may vary widely dependent on environmental conditions (temperature, humidity,....) The waveform is obtained by discharging 150pF capacitor through a resistor, R2 = 330Ω. A typical peak current may be high as 37A with 10kV.

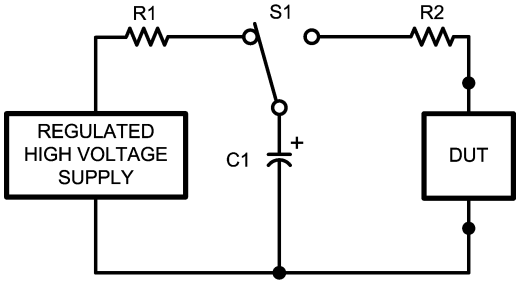

Figure 5. IEC ESD Model

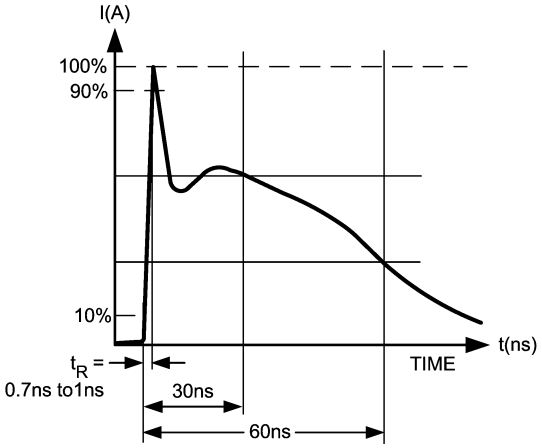

Figure 6. IEC Waveform

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMS202ECM	ACTIVE	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	LMS202ECM	Samples
LMS202ECM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMS202ECM	Samples
LMS202ECMX	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	LMS202ECM	Samples
LMS202ECMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMS202ECM	Samples
LMS202EIM	ACTIVE	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	LMS202EIM	Samples
LMS202EIM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMS202EIM	Samples
LMS202EIMX	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	LMS202EIM	Samples
LMS202EIMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMS202EIM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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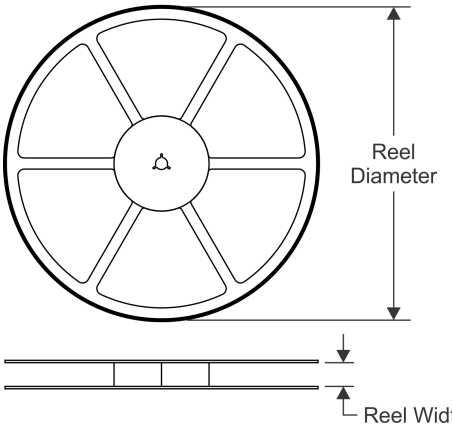
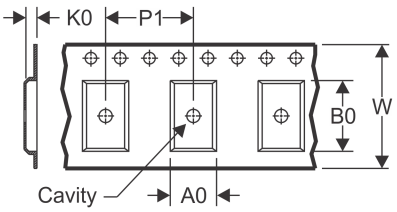
TAPE AND REEL INFORMATION

REEL DIMENSIONS

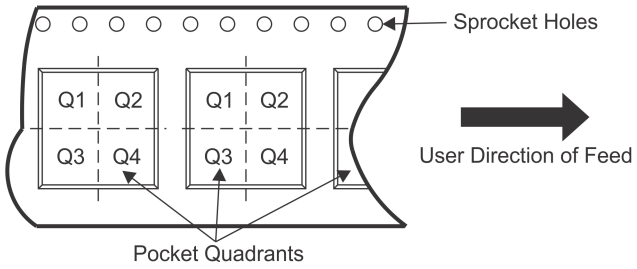


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

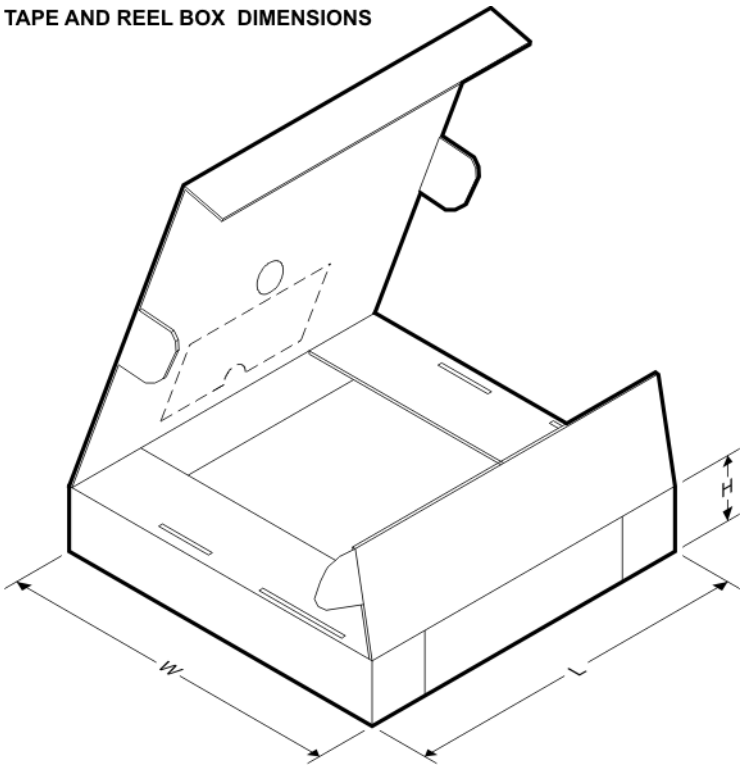
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMS202ECMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LMS202ECMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LMS202EIMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LMS202EIMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

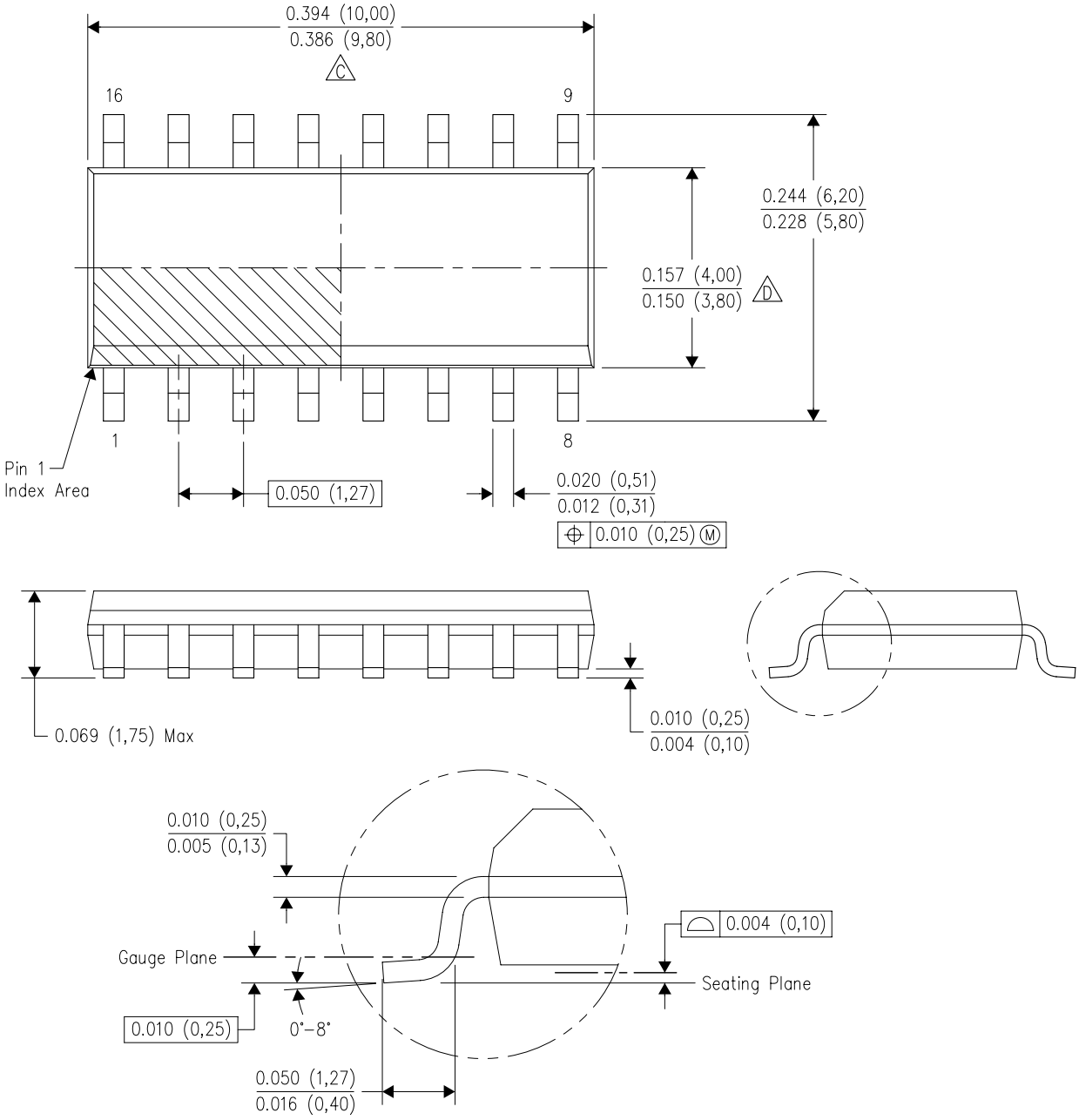
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMS202ECMX	SOIC	D	16	2500	349.0	337.0	45.0
LMS202ECMX/NOPB	SOIC	D	16	2500	349.0	337.0	45.0
LMS202EIMX	SOIC	D	16	2500	349.0	337.0	45.0
LMS202EIMX/NOPB	SOIC	D	16	2500	349.0	337.0	45.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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