LMS5213 80mA, μCap, Low Dropout Voltage Regulator in SOT

Check for Samples: LMS5213

FEATURES

- **Space Saving SOT Package**
- **Available in 2.8V, 3.0V, and 3.3V Fixed Voltages**
- **Ensured 80mA Output**
- **Low Quiescent Current**
- **Low Dropout Voltage**
- **Low Temperature Coefficient**
- **Current and Thermal Limiting**
- **Logic-Controlled Shutdown**
- **Stability With Low-ESR Ceramic Capacitors**
- **Pin-to-Pin Replacement for Mic™ 5213**

APPLICATIONS

- **Cellular Phones**
- **Battery-Powered Equipment**
- **Bar Code Scanner**
- **Laptop/Palmtop Computer**
- **High-Efficiency Linear Power Supplies**

DESCRIPTION

- The LMS5213 is a μCap, low dropout voltage regulator with very low quiescent current, 220μA typical, at 80mA load. It also has very low dropout voltage, typically 20mV at light load and 330mV at 80mA.

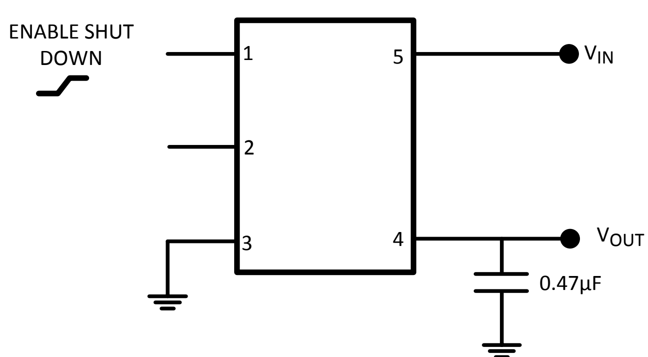
The LMS5213 provides up to 80mA and consumes a typical of 1μA in disable mode.

The LMS5213 is optimized to work with low value, low cost ceramic capacitors. The output typically require only 0.47μF of output capacitance for stability. The enable pin can be tied to V_{IN} for easy device layout.

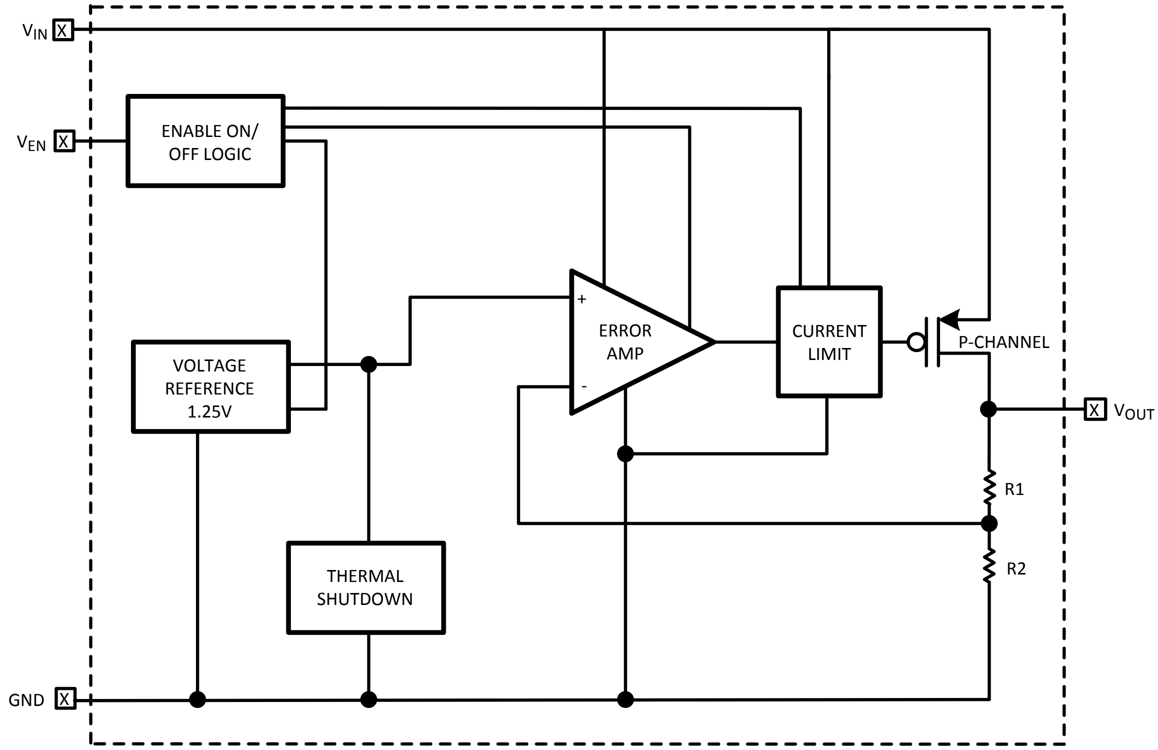
The LMS5213 is designed for portable, battery powered equipment applications with small space requirements.

The LMS5213 is available in a space saving 5-pin SOT package. Performance is specified for the −40°C to +125°C temperature range and is available in 2.8V, 3.0V and 3.3V fixed voltages. For other output voltage options, please contact Texas Instruments.

TYPICAL APPLICATION



SIMPLIFIED SCHEMATIC



PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Function
1	V_{EN}	Enable Input Logic, Logic High = Enabled Logic Low = Shutdown
2	NC	Not internally connected
3	GND	Ground
4	V_{OUT}	Output Voltage
5	V_{IN}	Input Voltage

CONNECTION DIAGRAM

SOT-5

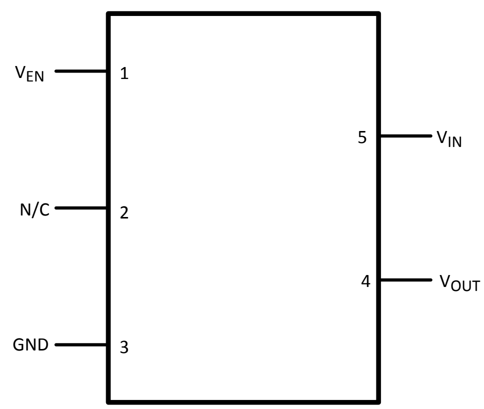


Figure 1. Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[1][2]

ESD Tolerance [3]	Human Body Model	2000V
Junction Temperature		150°C
V_{IN}, V_{OUT}, V_{EN}		−0.3 TO 6.5V
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering (10 sec)	260°C (lead temp)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.

OPERATING RATINGS

Supply Voltages	V_{IN}	2.7V to 6V
	V_{EN}	0V to V_{IN}
Junction Temp. Range [1]		−40°C to +125°C
Storage Temperature Range		−65°C to 150°C
Package Thermal Resistance	SOT-5	478°C/W

(1) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for T_J = 25°C, $V_{IN} = V_{OUT}$ + 1V, I_L = 1mA, C_L = 0.47µF, V_{EN} ≥ 2.0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
V_O	Output Voltage Accuracy		-3 -4		3 **4**	%
$\Delta V_O/\Delta T$	Output Voltage Temperature Coefficient	[3]		50	**200**	ppm/°C
$\Delta V_O/V_O$	Line Regulation	$V_{IN} = V_{OUT}$ +1V to 6V		0.008	0.3 **0.5**	%
$\Delta V_O/V_O$	Load Regulation	I_L = 0.1mA to 80mA [4]		0.08	0.3 **0.5**	%
V_{IN}-V_O	Dropout Voltage [5]	I_L = 100µA		20		mV
		I_L = 20mA		70	**350**	
		I_L = 50mA		180		
		I_L = 80mA		330	**600**	
I_Q	Quiescent Current	V_{EN} ≤ 0.4V (Shutdown)		1	10	µA
I_{GND}	Ground Pin Current	I_L = 100µA, V_{EN} ≥ 2.0V (active)		160		µA
		I_L = 20mA, V_{EN} ≥ 2.0V (active)		180	**750**	
		I_L = 50mA, V_{EN} ≥ 2.0V (active)		200		
		I_L = 80mA, V_{EN} ≥ 2.0V (active)		220	**3000**	

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) Output voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.
(4) Regulation is measured at constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
(5) Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V_{IN} = V_{OUT} + 1V, I_L = 1mA, C_L = 0.47µF, V_{EN} ≥ 2.0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{GNDDO}	Ground Pin Current at Dropout (6)	V_{IN} = $V_{OUT(NOMINAL)}$ –0.5V		200	**300**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V		180	**250**	mA
$\Delta V_O/\Delta P_D$	Thermal Regulation	(7)		0.05		%W
Enable Input						
V_{IL}	Enable Input Voltage Level	Logic Low (off)			**0.6**	V
V_{IH}		Logic High (on)	**2.0**			V
I_{IL}	Enable Input Current	V_{IL} ≤ 0.6V		0.01	**1**	µA
I_{IH}		V_{IH} ≥ 2.0V		15	**50**	µA

(6) Ground pin current is the regulator quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.
(7) Thermal regulation is defined as the change in output voltage at a time “t” after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for an 80mA load pulse at V_{IN} = 6V for t = 16ms.

TYPICAL CHARACTERISTICS

Unless otherwise specified, T_A = 25°C, V_{OUT} = 2.8V, C_L = 0.47µF

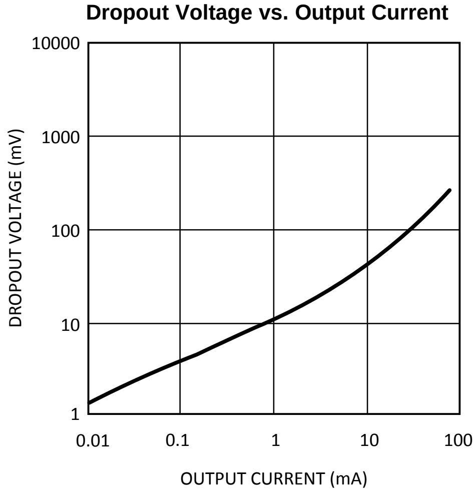


Figure 2.

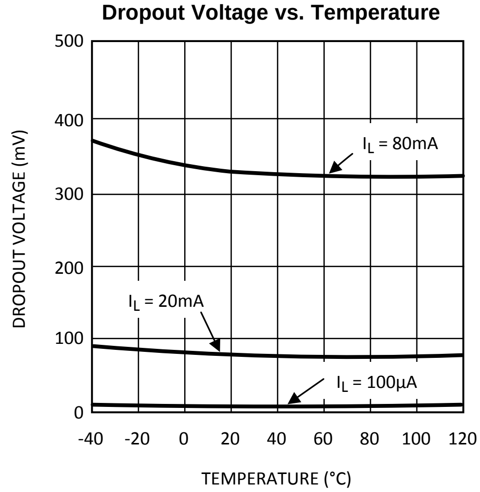


Figure 3.

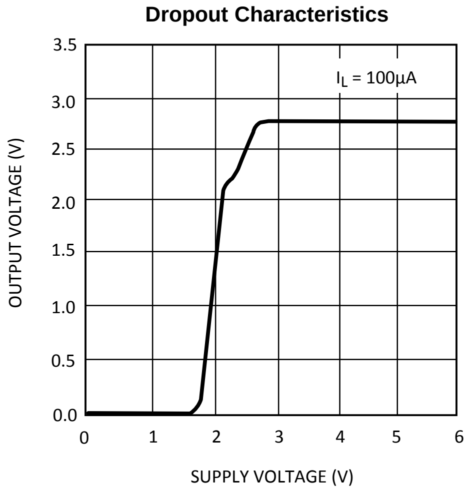


Figure 4.

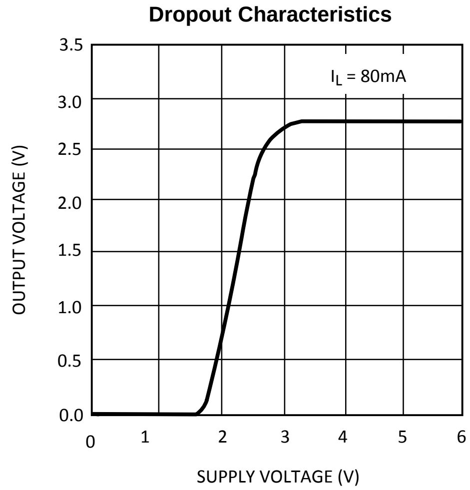


Figure 5.

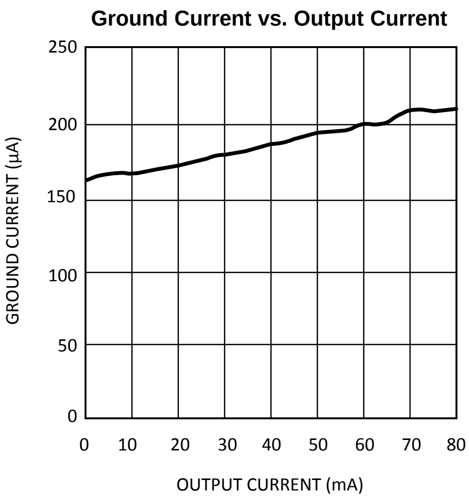


Figure 6.

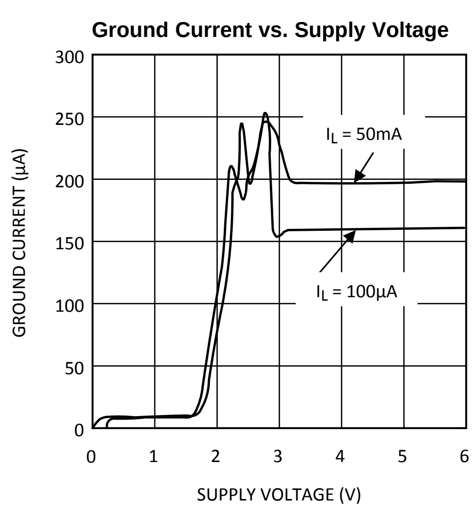


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V_{OUT} = 2.8V, C_L = 0.47µF

Ground Current vs. Temperature

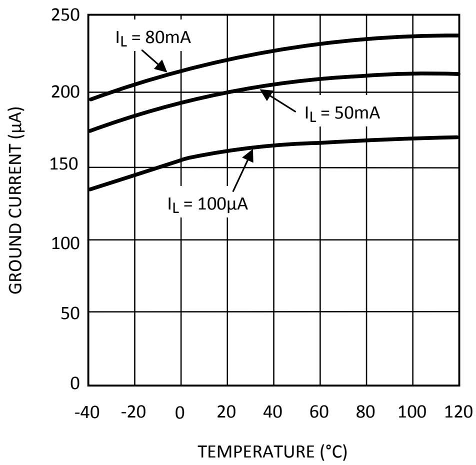


Figure 8.

Short Circuit Current vs. Input Voltage

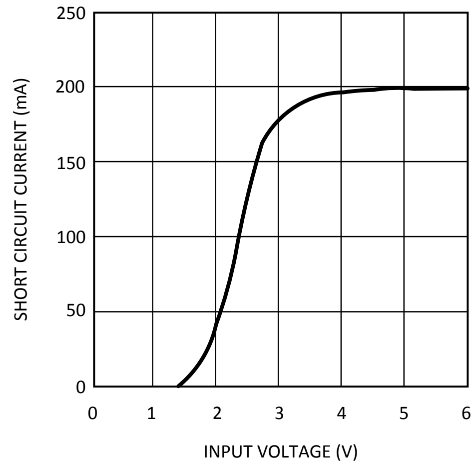


Figure 9.

Output Voltage vs. Temperature

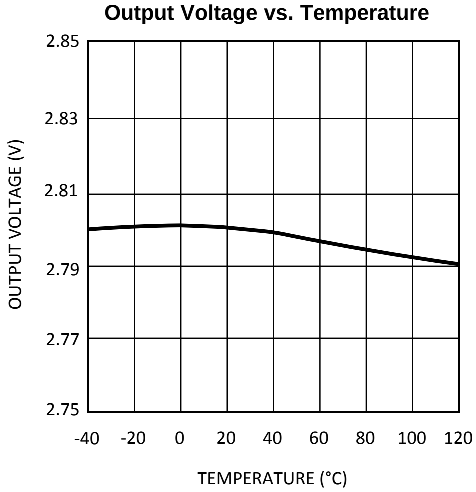


Figure 10.

Load Transient

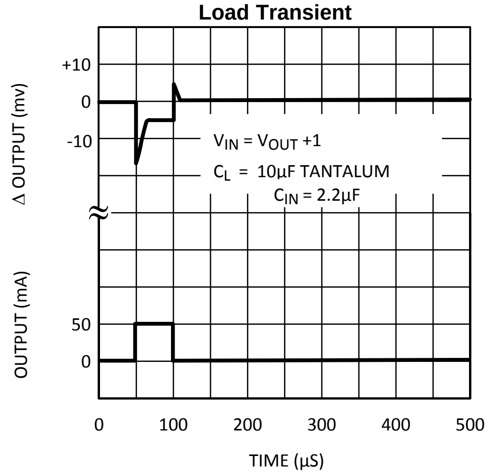


Figure 11.

Load Transient

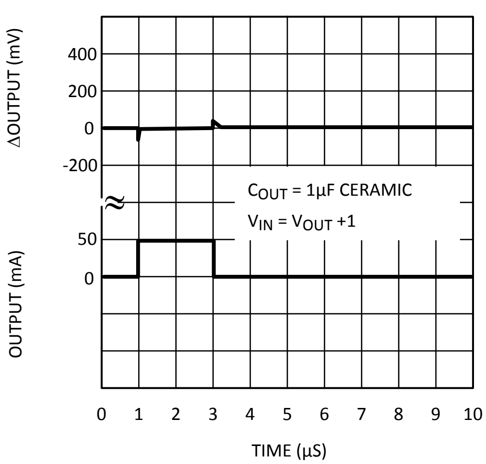


Figure 12.

Line Transient

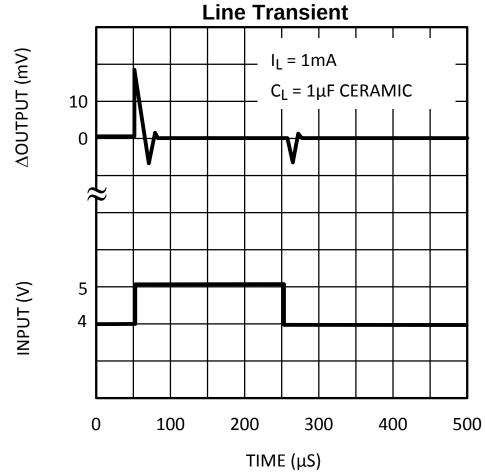


Figure 13.

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V_{OUT} = 2.8V, C_L = 0.47µF

Line Transient

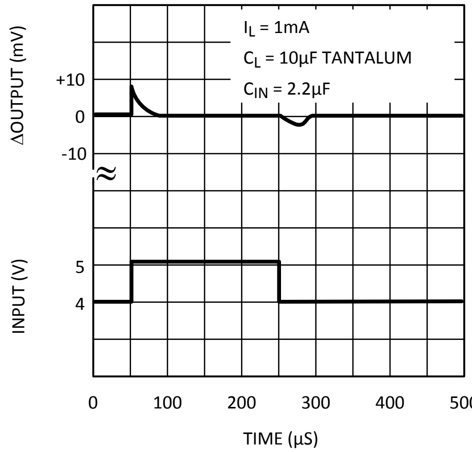


Figure 14.

Ripple Voltage vs. Frequency

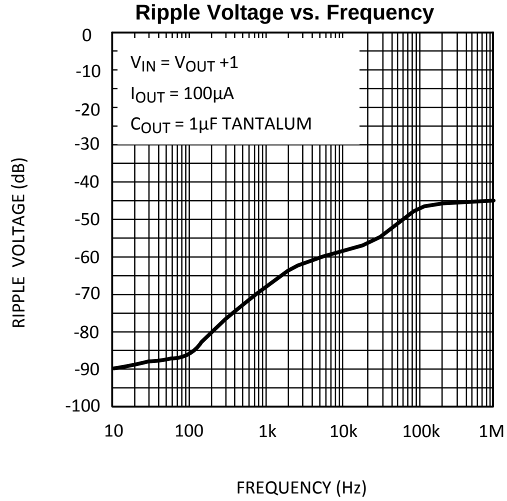


Figure 15.

Ripple Voltage vs. Frequency

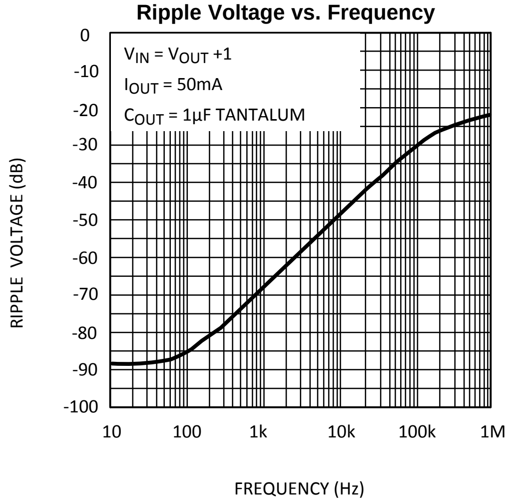


Figure 16.

Noise Characteristics

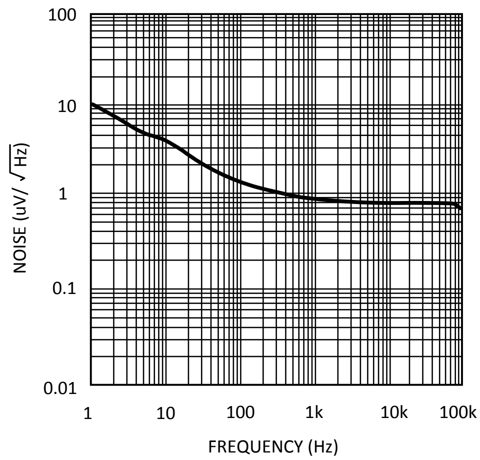


Figure 17.

Enable Characteristics (V_O = 3.3V)

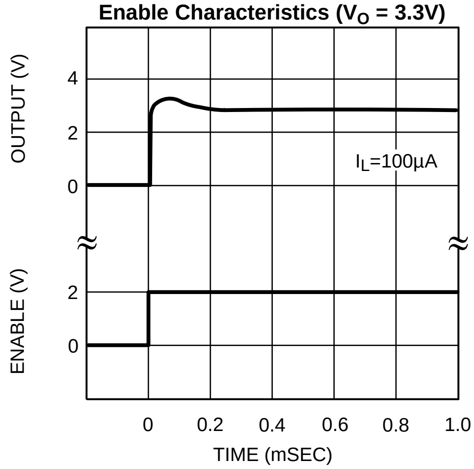


Figure 18.

Enable Characteristics (V_O = 3.3V)

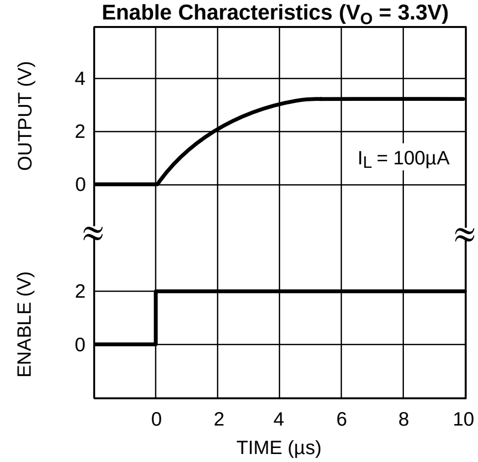


Figure 19.

APPLICATION INFORMATION

The LMS5213 is a low dropout, linear regulator designed primarily for battery-powered applications. The LMS5213 can be used with low cost ceramic capacitors, typical value of 0.47µF.

As illustrated in the simplified schematics, the LMS5213 consists of a 1.25V reference, error amplifier, P-channel pass transistor and internal feedback voltage divider. The 1.25V reference is connected to the input of the error amp. The error amp compares this reference with the feedback voltage. If the feedback voltage is lower than the reference, the pass transistor gate is pulled lower allowing more current to pass and increasing the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled up allowing less current to pass to the output. The output voltage is fedback through the resistor divider. Additional blocks include short circuit current protection and thermal protection.

The LMS5213 features an 80mA P-channel MOSFET transistor. This provides several advantages over similar designs using PNP pass transistors including longer battery life.

The P-channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable amounts of current in dropout when the pass transistor saturates. They also have high base drive currents under large loads. The LMS5213 does not suffer from these problems and consumes only the specified quiescent current under light and heavy loads.

External Capacitors

Like any low-dropout regulators, the LMS5213 requires external capacitors for regulator stability. The LMS5213 is specially designed for portable applications requiring minimum board space and the smallest components.

A 0.1µF capacitor should be placed from V_{IN} to GND if there is more than 10 inches of wire between the input and AC filter or when a battery is used as the input. This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground.

The LMS5213 is designed to work with small ceramic output capacitors. Ceramic capacitors ranging between 0.47µF to 4.7µF are the smallest and least expensive.

No-Load Stability

The LMS5213 will remain stable and in regulation with no-load (other than the internal voltage divider). This is especially important in CMOS RAM keep-alive applications.

Enable Input

The LMS5213 is shut off by pulling the V_{EN} pin below 0.6V; all internal circuitry is powered off and the quiescent current is typically 1µA. Pulling the V_{EN} high above 2V re-enables the device and allows operation. If the shut down feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on all the time.

Thermal Behavior

The LMS5213 regulator has internal thermal shutdown to protect the device from over heating. Under all operating conditions, the maximum junction temperature of the LMS5213 must be below 125°C. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. The maximum power dissipation is

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (1)$$

θ_{JA} is the junction-to-ambient thermal resistance, 478°C/W for the LMS5213 in the SOT package. T_A is the maximum ambient temperature $T_{J(MAX)}$ is the maximum junction temperature of the die, 125°C

When operating the LMS5213 at room temperature, the maximum power dissipation is 209 mW.

The actual power dissipated by the regulator is

$$P_D = (V_{IN}-V_{OUT})\, I_L + V_{IN}\, I_{GND} \quad (2)$$

The figure below shows the voltage and currents, which are present in the circuit.

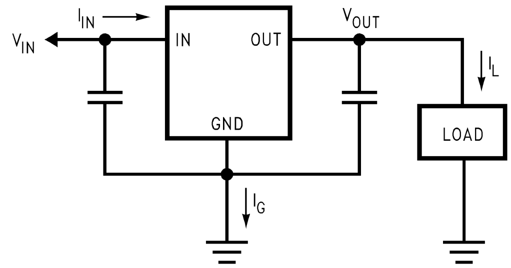


Figure 20. Power Dissipation Diagram

Substituting $P_{D(MAX)}$, determined above, for P_D and solving for the operating condition that are critical to the application will give the maximum operating conditions for the regulator circuit. To prevent the device from entering thermal shutdown, maximum power dissipation cannot be exceeded.

Fixed Voltage Regulator

The LMS5213 offers a smaller system solution that is ideal for general-purpose voltage regulation in any handheld device.

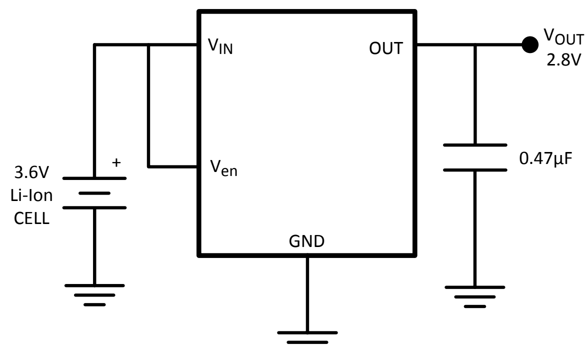


Figure 21. Single-Cell Regulator

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