150mA, µCap, Low Dropout Voltage Regulator with Power Good

Check for Samples: LMS5258

FEATURES

- **Power Good Indicator**
- **Stability With Low ESR Capacitors**
- **Low Ground Current: 120µA**
- **150mA Output Current**
- **"Zero" Shutdown Mode Current**
- **Fast Transient Response**
- **Auto Discharge**
- **Thermal Shutdown**
- **Current Limiting**
- **TTL-Logic-Controlled Enable Input**
- **Pin-to-Pin Replacement for MIC5258**

APPLICATIONS

- **Processor Power-Up Sequencing**
- **Laptop, Notebook and Palm Top Computer**
- **PCMCIA V_{CC} and V_{PP} Regulation Switching**

DESCRIPTION

The LMS5258 is a µCap, precise CMOS voltage regulator with power good output.

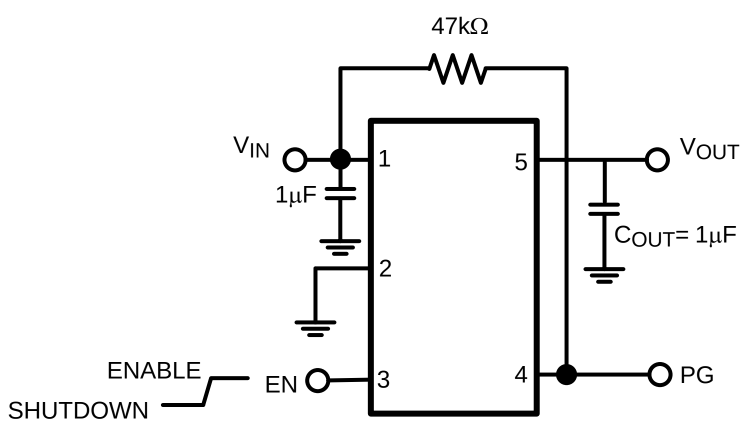
It provides up to 150mA and consumes a typical of 10nA in shutdown mode. The LMS5258 output stage is designed with a push pull output for faster transient response.

The LMS5258 is optimized to work with low value, low cost ceramic capacitors. The output typically require only 1µF of output capacitance for stability. The enable pin can be tied to V_{IN} for easy device layout.

The LMS5258 is designed for portable, battery powered equipment applications with small space requirements.

The LMS5258 is available in a 5-pin SOT package. Performance is specified for the −40°C to +125°C temperature range and is available in a fixed 1.2V. For other output voltage options, please contact Texas Instruments.

TYPICAL APPLICATION



PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Function
1	V_{IN}	Input Voltage
2	GND	Ground
3	EN	Enable Input Logic, Logic High = Enabled Logic Low = Shutdown (Do not leave open)
4	PG	Power Good Output
5	V_{OUT}	Output Voltage

CONNECTION DIAGRAM

SOT-5

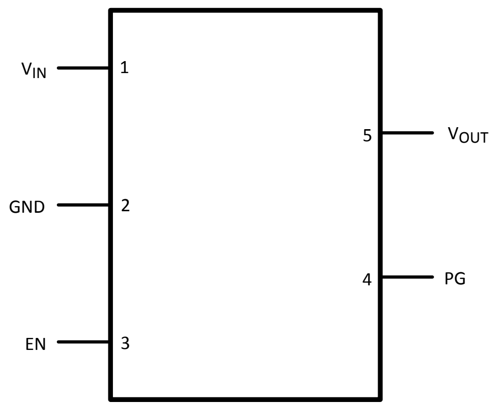


Figure 1. Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

ESD Tolerance (3)	Human Body Model	2000V
Junction Temperature		150°C
V_{IN}, V_{OUT}, V_{EN}		−0.3 TO 6.5V
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering (10 sec)	260°C (lead temp)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.

OPERATING RATINGS

Supply Voltages	V_{IN}	2.7V to 6V
	V_{EN}	0V to V_{IN}
Junction Temp. Range (1)		−40°C to +125°C
Storage Temperature Range		−65°C to 150°C
Package Themal Resistance	SOT-5	235°C/W

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

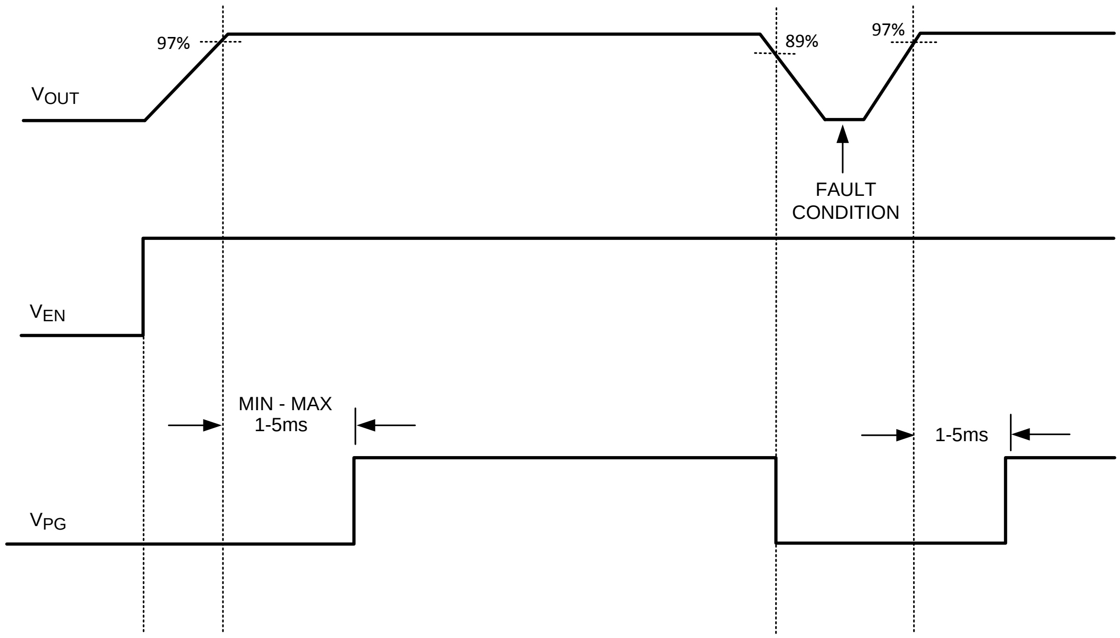
ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for T_J = 25°C, V_{IN} = 2.7V, I_L = 100µA, C_{OUT} = 1µF, V_{EN} ≥ 2.0V. **Boldface** limits apply over the entire operating temperature range, −40°C to 125°C.

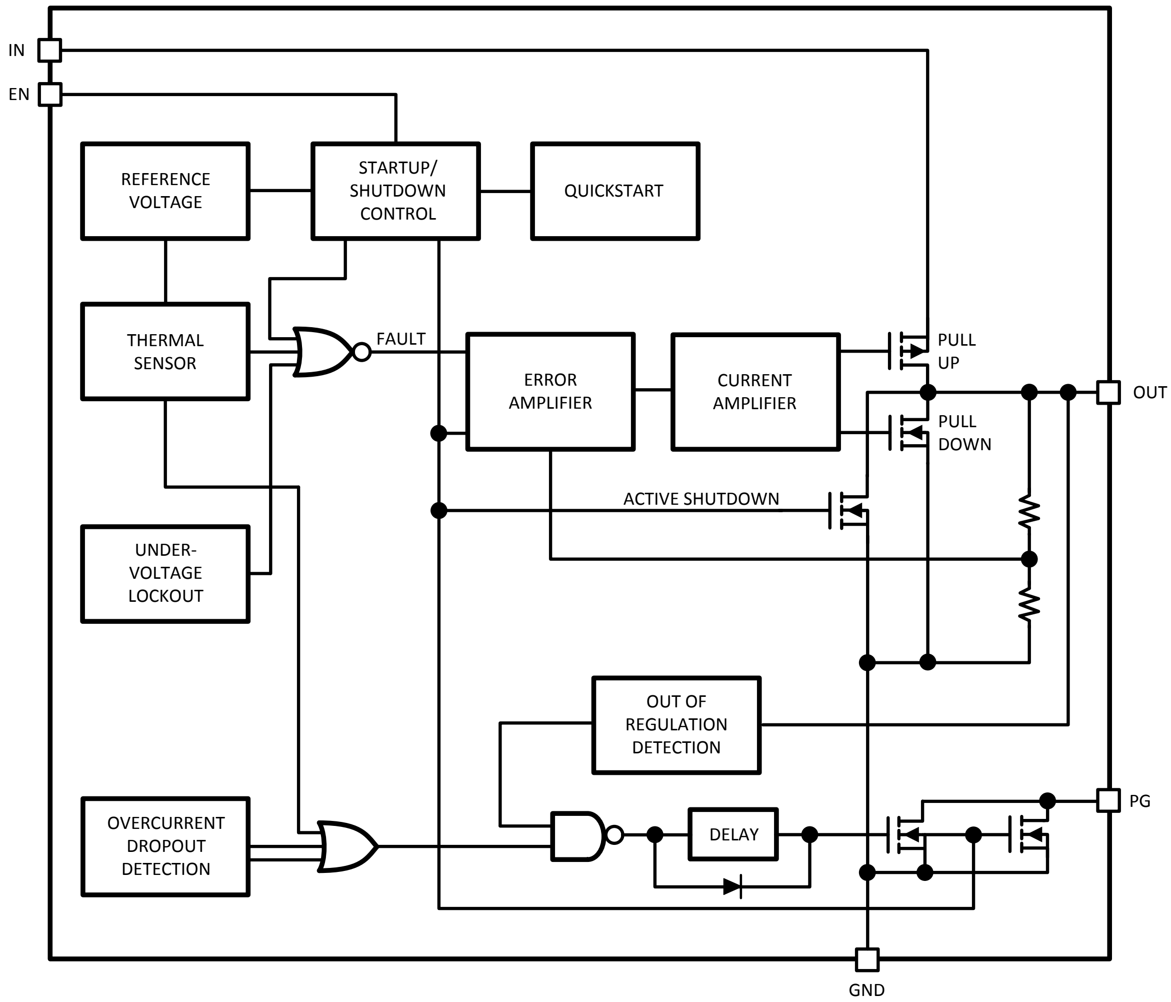
Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_O	Output Voltage Accuracy		-3 **-4**		3 **4**	%
$\Delta V_O/V_O$	Line Regulation	V_{IN} = 2.7V to 6V	**−0.3**		**0.3**	%
$\Delta V_O/V_O$	Load Regulation	I_L = 0.1mA to 150mA (3)		1	4	%
I_Q	Quiescent Current	V_{EN} ≤ 0.4V (Shutdown), PG = NC		.01	1	µA
I_{GND}	Ground Pin Current (1)	V_{EN} ≥ 2.0V (active), V_{IN} = 6V, I_L = 0mA		120	180	µA
		I_L = 150mA, V_{EN} ≥ 2.0V (active), V_{IN} = 6V		160	225	
PSRR	Power Supply Rejection	f = 120H_Z, C_{OUT} = 4.7µF, I_L= 150mA		62		dB
I_{LIMIT}	Current Limit	V_{OUT} = 0V	160	350		mA
Thermal Protection						
	Thermal Shutdown Temperature			150		°C
Enable Input						
V_{IL}	Enable Input Voltage Level	Logic Low (off), V_{IN} = 5.5V			**0.4**	V
V_{IH}		Logic High (on), V_{IN} = 5.5V	**2**			V
I_{IL}	Enable Input Current	V_{IL} ≤ 0.4V, V_{IN} = 5.5V		0.01		µA
I_{IH}		V_{IH} ≥ 2.0V, V_{IN} = 5.5V		0.01		µA
Power Good						
V_{PG}	Low Threshold	% of V_{OUT} (PG ON)	89			%
	High Threshold	% of V_{OUT} (PG OFF)			97	
V_{OL}	PG Output Logic-Low Voltage	Ipowergood = 100µA, Fault Condition		0.02	0.1	V
I_{PG}	Power Good Leakage Current	Power Good Off, V_{PG} = 5.5V		0.01		µA
V_{PG} Delay	Delay Time to Power Good	See Timing Diagram	1		5	ms

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) Regulation is measured at constant junction temperature using low duty cycle pulse testing.

TIMING DIAGRAM



BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, V_{IN} = 3.3V, C_{OUT} = 1µF, T_A = 25°C and powergood pull up resistor = 47kΩ.

Ground Current vs. Output Current

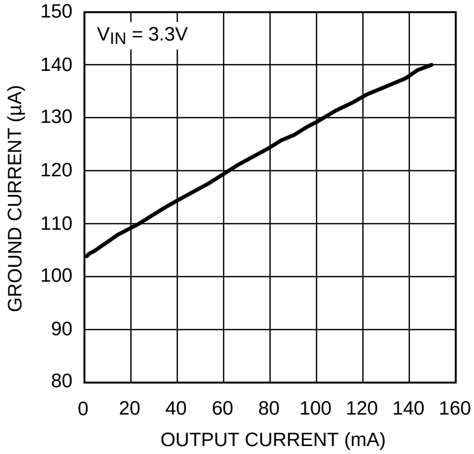


Figure 2.

Ground Current vs. Input Voltage

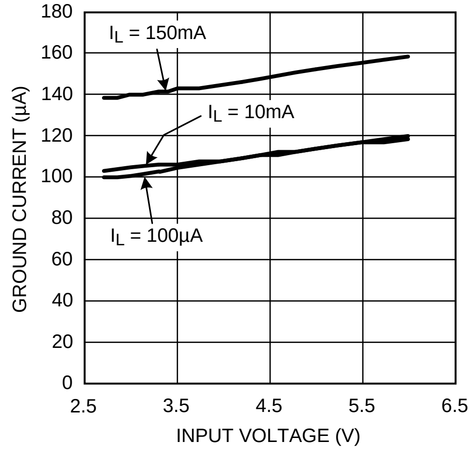


Figure 3.

Ground Current vs. Temperature

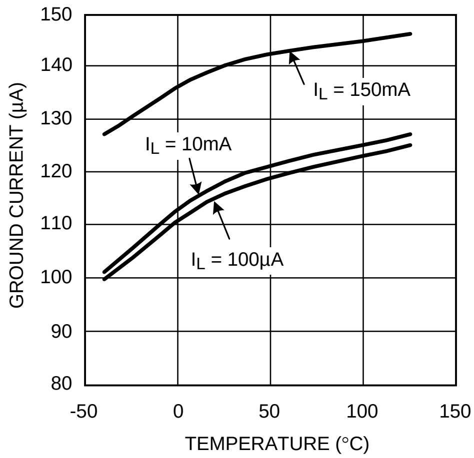


Figure 4.

Short Circuit Current vs. Temperature (V_{IN} = 3.3V)

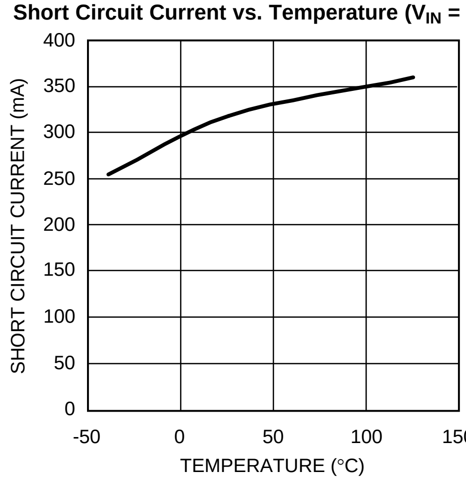


Figure 5.

Short Circuit Current vs. Input Voltage

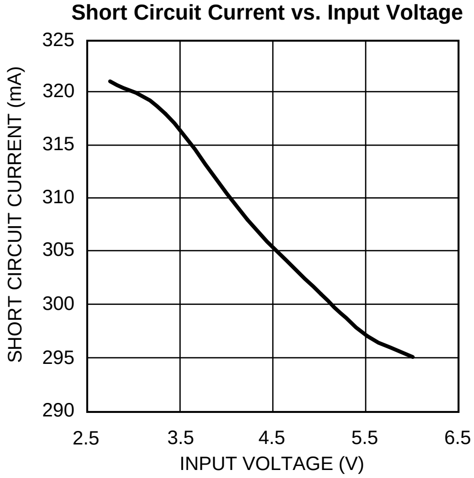


Figure 6.

Power Good Delay vs. Input Voltage (I_L = 100µA)

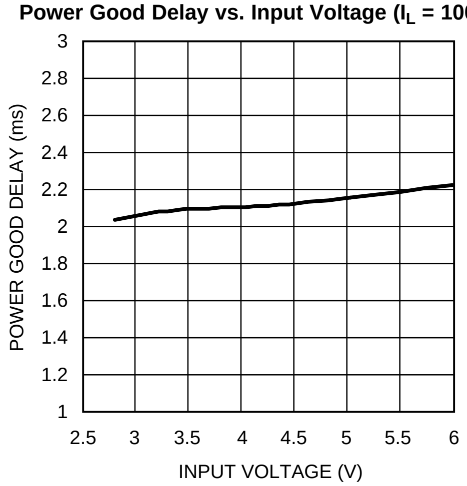


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 3.3V, C_{OUT} = 1µF, T_A = 25°C and powergood pull up resistor = 47kΩ.

Power Good Delay vs. Temperature (V_{IN} = 3.3V)

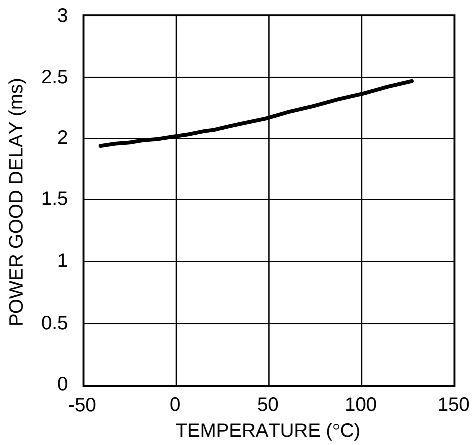


Figure 8.

Output Voltage vs. Temperature

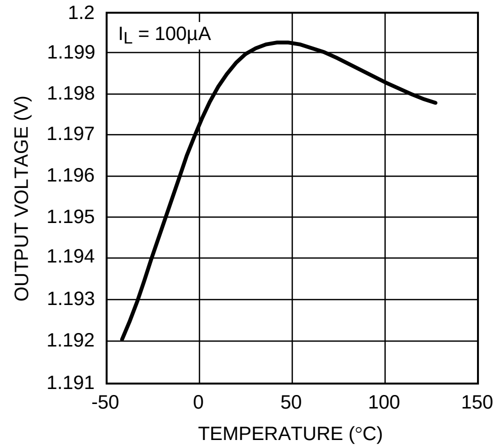


Figure 9.

Output Voltage vs. Input Voltage

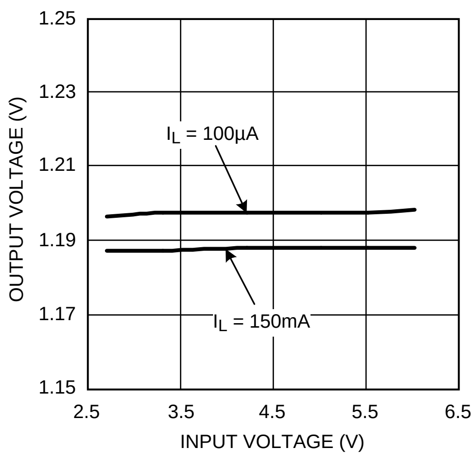


Figure 10.

Output Voltage vs. Output Current

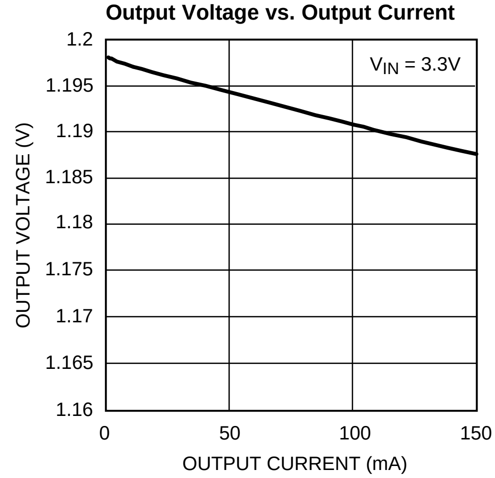


Figure 11.

Enable Voltage vs. Input Voltage

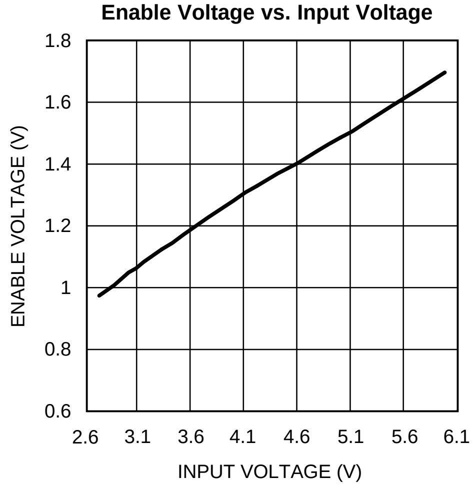


Figure 12.

Enable Voltage vs. Temperature

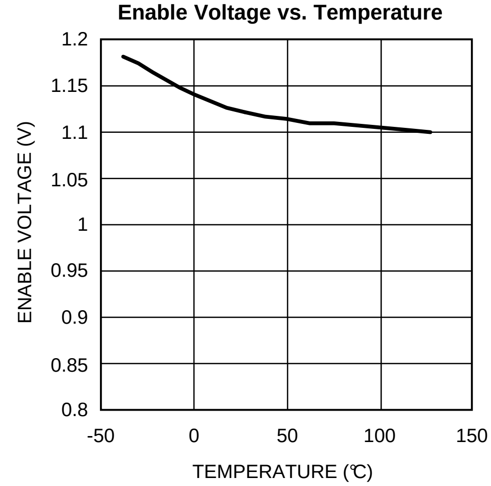


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 3.3V, C_{OUT} = 1μF, T_A = 25°C and powergood pull up resistor = 47kΩ.

Power Good Pull-Up Resistor vs. Power Good

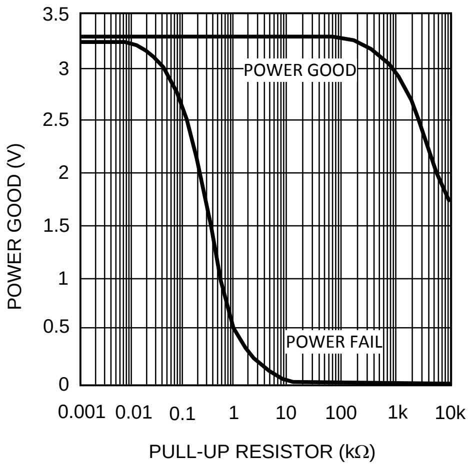


Figure 14.

Voltage Noise vs. Frequency

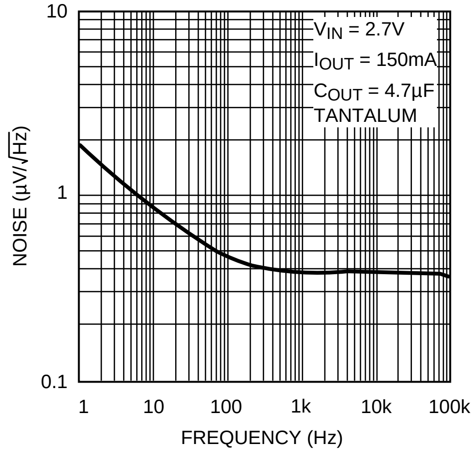


Figure 15.

PSRR vs. Frequency

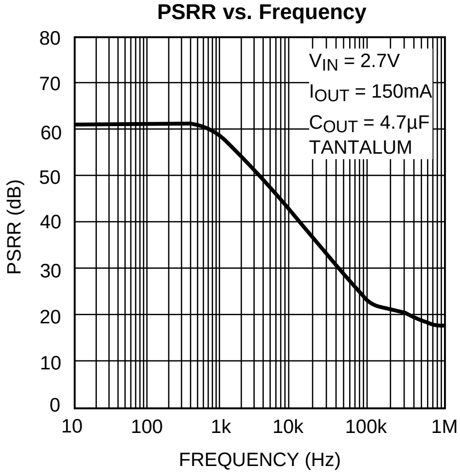


Figure 16.

Power On Reset Delay Time

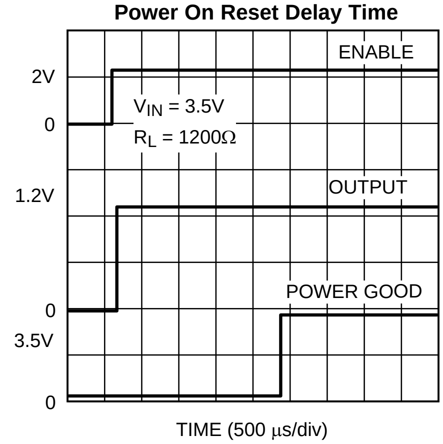


Figure 17.

APPLICATION NOTES

LMS5258 is a linear regulator designed to be used with a low ESR, low cost ceramic capacitors.

EXTERNAL CAPACITORS

The LMS5258 regulator requires an output capacitor to maintain stability. The capacitor must be at least 1µF or greater. The capacitor can be low-ESR ceramic chip capacitor, however for improved capacitance over temperature, tantalum capacitors can be used.

A 1µF input capacitor is recommended when the supply capacitance is more than 10 inches away from the device, or when the supply is a battery.

X7R dielectric ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much 50% and 60% respectively over their operating temperature range. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic or a tantalum capacitor to ensure the same minimum capacitance value over the operating temperature range. Tantalum capacitors have a very stable dielectric (10% over their operating temperature range) and can also be used with this device.

ENABLE/SHUTDOWN

The LMS5258 has an active high enable pin that allows the regulator to be disabled. Applying a Logic Level low (<0.4 V) to the Shutdown pin will cause the output to turn off, in this state current consumed by the regulator goes nearly to zero. Applying a logic level high (>2.0) enables the output voltage. The enable/shutdown pin can't be left floating; a floating enable pin may cause an indeterminate state on the output.

ACTIVE SHUTDOWN

The LMS5258 designed with a N-channel MOSFET that acts as a shutdown clamp. The N-channel turns on when the device is disabled to allow the output capacitor and load to discharge.

POWER GOOD

The power good output is an open-drain output. It is designed essentially to work as a power-on reset generator once the regulated voltage was up and/ or a fault condition. When a fault condition and an undervoltage detection occur, the output of the power good pin goes low. The power good output comes back up once the output has reached 97% of its nominal value and 1ms to 5ms delay has passed , see timing diagram.

The LMS5258 internal circuit monitors overcurrent, temperature and falling output voltage. If one of these conditions is flaged that indicates a fault condition.

The flaged condition output is fed into an onchip delay circuit that drives the open drain output transistor.

TRANSIENT RESPONSE

The LMS5258 implements a unique output stage to dramatically improve transient response recovery time. The output is a totem-pole configuration with a P-channel MOSFET pass device and a N-channel MOSFET clamp. The N-channel clamp is a significantly smaller device that prevents the output voltage from overshooting when a heavy load is removed. This feature helps to speed up the transient response by significantly decreasing transient response recovery time during the transition from heavy load to light load.

THERMAL BEHAVIOR

The LMS5258 regulator has internal thermal shutdown to protect the device from over heating. Under all operating conditions, the maximum junction temperature of the LMS5258 must be below 125°C. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. The maximum power dissipation is

$$P_{D(MAX)} = (T_{J(MAX)} – T_A)/\theta_{JA} \quad (1)$$

θ_{JA} is the junction-to-ambient thermal resistance, 235°C/W for the LMS5258 in the SOT-5 package. T_A is the maximum ambient temperature $T_{J(MAX)}$ is the maximum junction temperature of the die, 125°C.

When operating the LMS5258 at room temperature, the maximum power dissipation is 425mW.

The actual power dissipated by the regulator is

$$P_D = (V_{IN} - V_{OUT})\ I_L + V_{IN}\ I_{GND} \quad (2)$$

Substituting $P_{D(MAX)}$, determined above, for P_D and solving for the operating condition that are critical to the application will give the maximum operating conditions for the regulator circuit. To prevent the device from entering thermal shutdown, maximum power dissipation cannot be exceeded.