

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

Check for Samples: [LMV321 SINGLE](#), [LMV358 DUAL](#), [LMV324 QUAD](#), [LMV324S QUAD WITH SHUTDOWN](#)

FEATURES

- 2.7-V and 5-V Performance
- –40°C to 125°C Operation
- Low-Power Shutdown Mode (LMV324S)
- No Crossover Distortion
- Low Supply Current
 - LMV321 . . . 130 μ A Typ
 - LMV358 . . . 210 μ A Typ
 - LMV324 . . . 410 μ A Typ
 - LMV324S . . . 410 μ A Typ
- Rail-to-Rail Output Swing
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

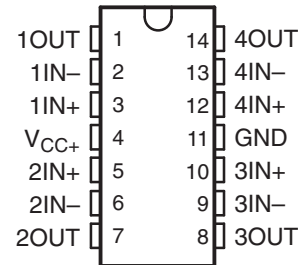
DESCRIPTION/ ORDERING INFORMATION

The LMV321, LMV358, and LMV324/LMV324S are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing. The LMV324S, which is a variation of the standard LMV324, includes a power-saving shutdown feature that reduces supply current to a maximum of 5 μ A per channel when the amplifiers are not needed. Channels 1 and 2 together are put in shutdown, as are channels 3 and 4. While in shutdown, the outputs actively are pulled low.

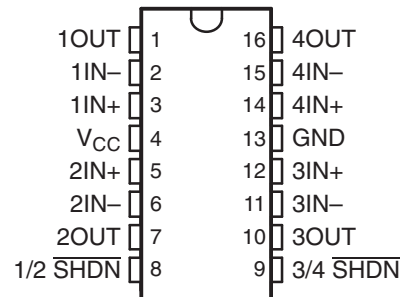
The LMV321, LMV358, LMV324, and LMV324S are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. Additional features of the LMV3xx devices are a common-mode input voltage range that includes ground, 1-MHz unity-gain bandwidth, and 1-V/ μ s slew rate.

The LMV321 is available in the ultra-small DCK (SC-70) package, which is approximately one-half the size of the DBV (SOT-23) package. This package saves space on printed circuit boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

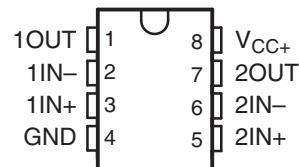
LMV324 . . . D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)



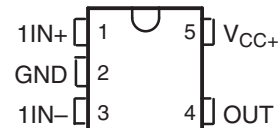
LMV324S . . . D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)



LMV358 . . . D (SOIC), DDU (VSSOP),
DGK (MSOP), OR PW (TSSOP) PACKAGE
(TOP VIEW)



LMV321 . . . DBV (SOT-23) OR DCK (SC-70) PACKAGE
(TOP VIEW)



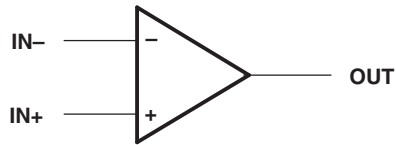
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

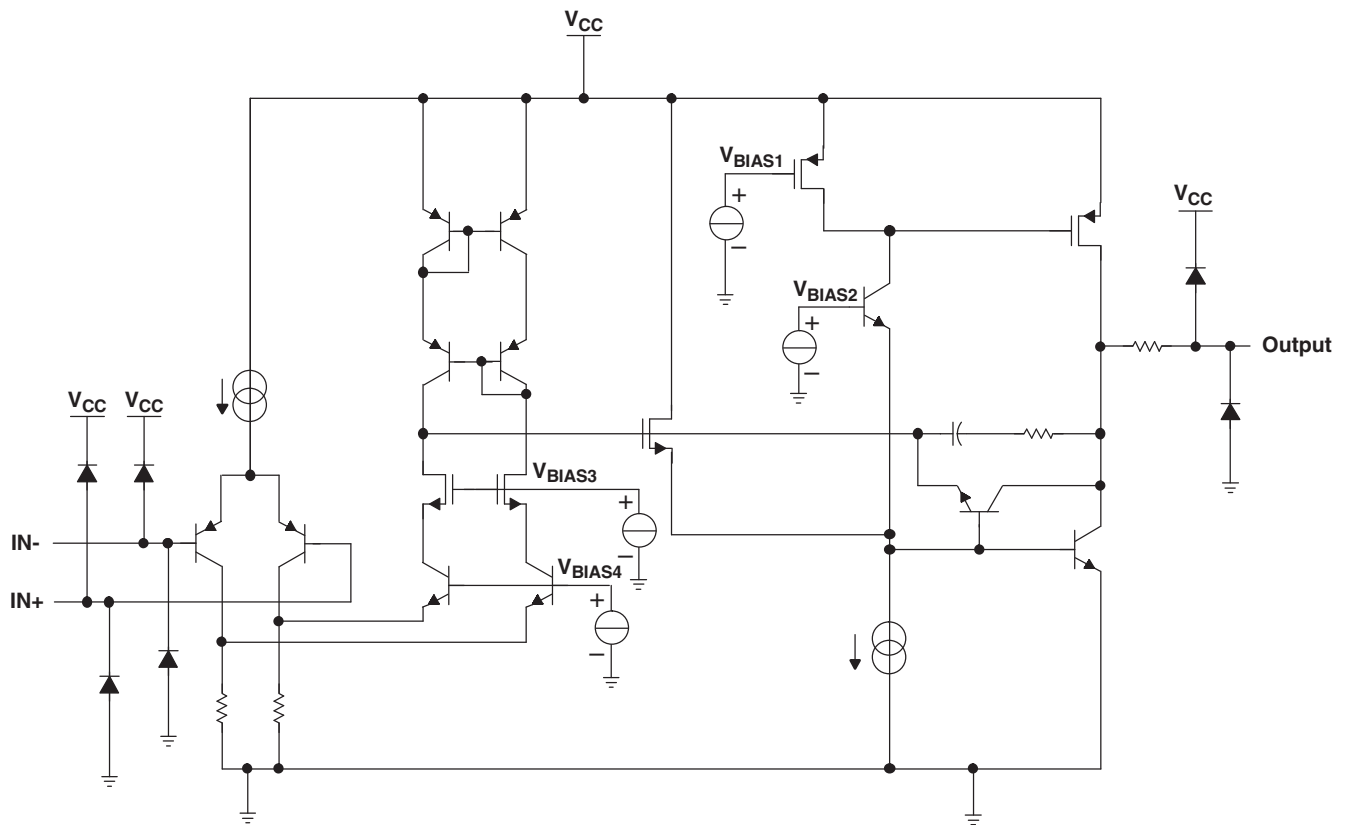
T_A	PACKAGE⁽²⁾			ORDERABLE PART NUMBER	TOP-SIDE MARKING⁽³⁾
–40°C to 85°C	Single	SC-70 – DCK	Reel of 3000	LMV321IDCKR	R3_
			Reel of 250	LMV321IDCKT	
–40°C to 125°C	Single	SOT-23 – DBV	Reel of 3000	LMV321IDBVR	RC1_
			Reel of 250	LMV321IDBVT	
–40°C to 125°C	Dual	MSOP/VSSOP – DGK	Reel of 2500	LMV358IDGKR	R5_
			Reel of 250	LMV358IDGKT	PREVIEW
		SOIC – D	Tube of 75	LMV358ID	MV358I
			Reel of 2500	LMV358IDR	
		TSSOP – PW	Tube of 150	LMV358IPW	MV358I
			Reel of 2000	LMV358IPWR	
		VSSOP – DDU	Reel of 3000	LMV358IDDU	RA5_
–40°C to 125°C	Quad	SOIC – D	Tube of 50	LMV324ID	LMV324I
			Reel of 2500	LMV324IDR	
–40°C to 85°C	Quad	SOIC – D	Tube of 50	LMV324SID	LMV324SI
			Reel of 2500	LMV324SIDR	
–40°C to 125°C	Quad	TSSOP – PW	Reel of 2000	LMV324IPWR	MV324I
			Reel of 2000	LMV324SIPWR	MV324SI
–40°C to 125°C	Dual	MSOP/VSSOP – DGK	Reel of 2500	LMV358QDGKR	RH_
			Reel of 250	LMV358QDGKT	
		SOIC – D	Tube of 75	LMV358QD	MV358Q
			Reel of 2500	LMV358QDR	
		TSSOP – PW	Tube of 150	LMV358QPW	MV358Q
			Reel of 2000	LMV358QPWR	
		VSSOP – DDU	Reel of 3000	LMV358QDDUR	RAH_
	Quad	SOIC – D	Tube of 50	LMV324QD	LMV324Q
			Reel of 2500	LMV324QDR	
		TSSOP – PW	Tube of 90	LMV324QPW	MV324Q
			Reel of 2000	LMV324QPWR	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK/DDU/DGK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

SYMBOL (EACH AMPLIFIER)



LMV324 SIMPLIFIED SCHEMATIC



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		5.5	V
V _{ID}	Differential input voltage ⁽³⁾		±5.5	V
V _I	Input voltage range (either input)	–0.2	5.5	V
	Duration of output short circuit (one amplifier) to ground ⁽⁴⁾	At or below T _A = 25°C, V _{CC} ≤ 5.5 V		Unlimited
θ _{JA}	Package thermal impedance ^{(5) (6)}	D package	8 pin	97
			14 pin	86
			16 pin	73
		DBV package	5 pin	206
		DCK package	5 pin	252
		DDU package	8 pin	210
		PW package	8 pin	172
			14 pin	149
			16 pin	113
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
- (5) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage (single-supply operation)	2.7	5.5	V
V _{IH}	Amplifier turn-on voltage level (LMV324S) ⁽²⁾	V _{CC} = 2.7 V	1.7	V
		V _{CC} = 5 V	3.5	
V _{IL}	Amplifier turn-off voltage level (LMV324S)	V _{CC} = 2.7 V	0.7	V
		V _{CC} = 5 V	1.5	
T _A	Operating free-air temperature	I temperature (LMV321, LMV358, LMV324)	–40	°C
		I temperature (LMV324S, LMV321IDCK)	–40	
		Q temperature	–40	

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).
- (2) V_{IH} should not be allowed to exceed V_{CC}.

Electrical Characteristics

 $V_{CC+} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IO} Input offset voltage			1.7	7	mV
α_{VIO} Average temperature coefficient of input offset voltage			5		$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current			11	250	nA
I_{IO} Input offset current			5	50	nA
CMRR Common-mode rejection ratio	$V_{CM} = 0$ to 1.7 V	50	63		dB
k_{SVR} Supply-voltage rejection ratio	$V_{CC} = 2.7\text{ V}$ to 5 V , $V_O = 1\text{ V}$	50	60		dB
V_{ICR} Common-mode input voltage range	CMRR $\geq 50\text{ dB}$	0	–0.2		V
			1.9	1.7	
V_O Output swing	$R_L = 10\text{ k}\Omega$ to 1.35 V	High level	$V_{CC} - 100$	$V_{CC} - 10$	mV
		Low level		60	180
I_{CC} Supply current	LMV321I		80	170	μA
	LMV358I (both amplifiers)		140	340	
	LMV324I/LMV324SI (all four amplifiers)		260	680	
B_1 Unity-gain bandwidth	$C_L = 200\text{ pF}$		1		MHz
Φ_m Phase margin			60		deg
G_m Gain margin			10		dB
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$		46		$\text{nV}/\sqrt{\text{Hz}}$
I_n Equivalent input noise current	$f = 1\text{ kHz}$		0.17		$\text{pA}/\sqrt{\text{Hz}}$

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

Shutdown Characteristics (LMV324S)

 $V_{CC+} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$I_{CC(SHDN)}$ Supply current in shutdown mode (per channel)	$\overline{\text{SHDN}} \leq 0.6\text{ V}$			5	μA
$t_{(on)}$ Amplifier turn-on time	$A_V = 1$, $R_L = \text{Open}$ (measured at 50% point)		2		μs
$t_{(off)}$ Amplifier turn-off time	$A_V = 1$, $R_L = \text{Open}$ (measured at 50% point)		40		ns

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

Electrical Characteristics

$V_{CC+} = 5\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V_{IO} Input offset voltage		25°C		1.7	7	mV
		Full range			9	
α_{VIO} Average temperature coefficient of input offset voltage		25°C		5		$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current		25°C		15	250	nA
		Full range			500	
I_{IO} Input offset current		25°C		5	50	nA
		Full range			150	
CMRR Common-mode rejection ratio	$V_{CM} = 0\text{ to }4\text{ V}$	25°C	50	65		dB
k_{SVR} Supply-voltage rejection ratio	$V_{CC} = 2.7\text{ V to }5\text{ V}$, $V_O = 1\text{ V}$, $V_{CM} = 1\text{ V}$	25°C	50	60		dB
V_{ICR} Common-mode input voltage range	CMRR $\geq 50\text{ dB}$	25°C	0	-0.2		V
				4.2	4	
V_O Output swing	$R_L = 2\text{ k}\Omega\text{ to }2.5\text{ V}$	High level	25°C	$V_{CC} - 300$	$V_{CC} - 40$	mV
			Full range	$V_{CC} - 400$		
		Low level	25°C		120	
			Full range		400	
	$R_L = 10\text{ k}\Omega\text{ to }2.5\text{ V}$	High level	25°C	$V_{CC} - 100$	$V_{CC} - 10$	
			Full range	$V_{CC} - 200$		
		Low level	25°C		65	
			Full range		280	
A_{VD} Large-signal differential voltage gain	$R_L = 2\text{ k}\Omega$	25°C	15	100		V/mV
		Full range	10			
I_{OS} Output short-circuit current	Sourcing, $V_O = 0\text{ V}$	25°C	5	60		mA
	Sinking, $V_O = 5\text{ V}$		10	160		
I_{CC} Supply current	LMV321I	25°C		130	250	μA
		Full range			350	
	LMV358I (both amplifiers)	25°C		210	440	
		Full range			615	
	LMV324I/LMV324SI (all four amplifiers)	25°C		410	830	
		Full range			1160	
B_1 Unity-gain bandwidth	$C_L = 200\text{ pF}$	25°C		1		MHz
Φ_m Phase margin		25°C		60		deg
G_m Gain margin		25°C		10		dB
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$	25°C		39		$\text{nV}/\sqrt{\text{Hz}}$
I_n Equivalent input noise current	$f = 1\text{ kHz}$	25°C		0.21		$\text{pA}/\sqrt{\text{Hz}}$
SR Slew rate		25°C		1		$\text{V}/\mu\text{s}$

- (1) Full range $T_A = -40^\circ\text{C}$ to 125°C for I temperature (LMV321, LMV358, LMV324), -40°C to 85°C for (LMV324S, LMV321IDCK) and -40°C to 125°C for Q temperature.
- (2) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

Shutdown Characteristics (LMV324S)

$V_{CC+} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	$\overline{\text{SHDN}} \leq 0.6\text{ V}$, $T_A = \text{Full Temperature Range}$			5	μA
$t_{(on)}$	Amplifier turn-on time	$A_V = 1$, $R_L = \text{Open}$ (measured at 50% point)		2		μs
$t_{(off)}$	Amplifier turn-off time	$A_V = 1$, $R_L = \text{Open}$ (measured at 50% point)		40		ns

- (1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

TYPICAL CHARACTERISTICS

LMV321 FREQUENCY RESPONSE
VS
RESISTIVE LOAD

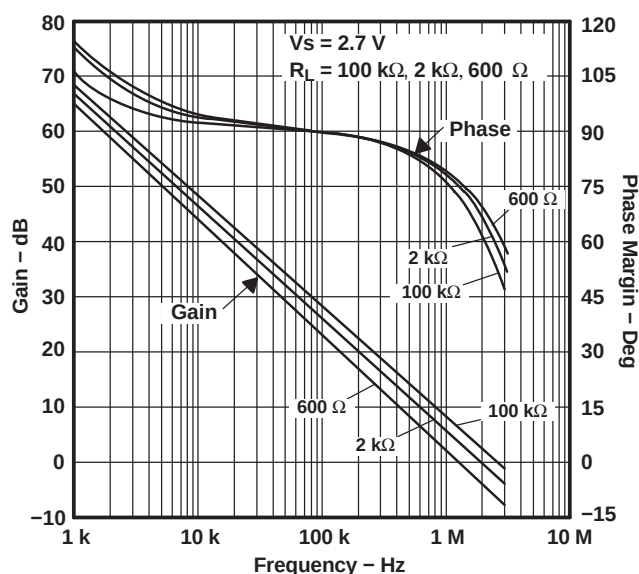


Figure 1.

LMV321 FREQUENCY RESPONSE
VS
RESISTIVE LOAD

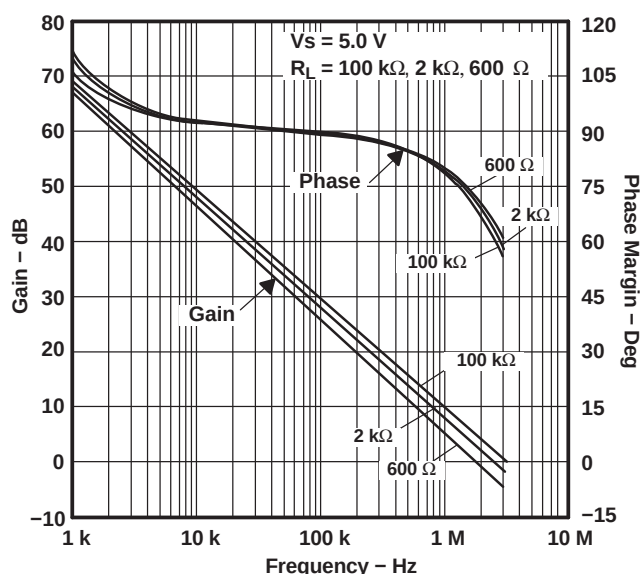


Figure 2.

LMV321 FREQUENCY RESPONSE
VS
CAPACITIVE LOAD

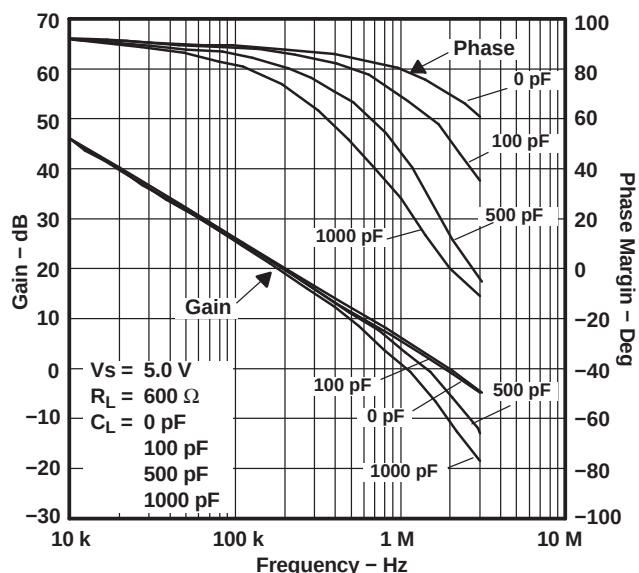


Figure 3.

LMV321 FREQUENCY RESPONSE
VS
CAPACITIVE LOAD

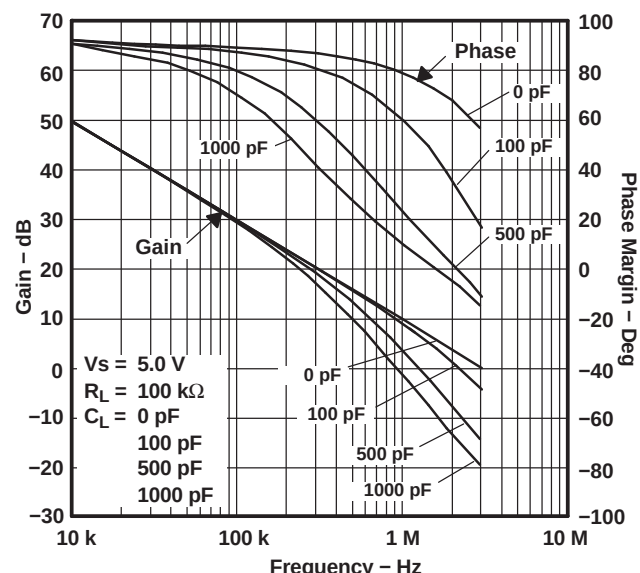


Figure 4.

TYPICAL CHARACTERISTICS (continued)

LMV321 FREQUENCY RESPONSE
VS
TEMPERATURE

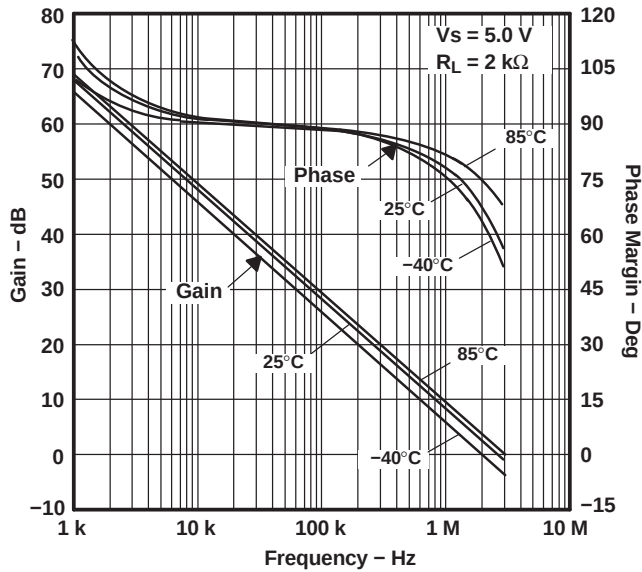


Figure 5.

STABILITY
VS
CAPACITIVE LOAD

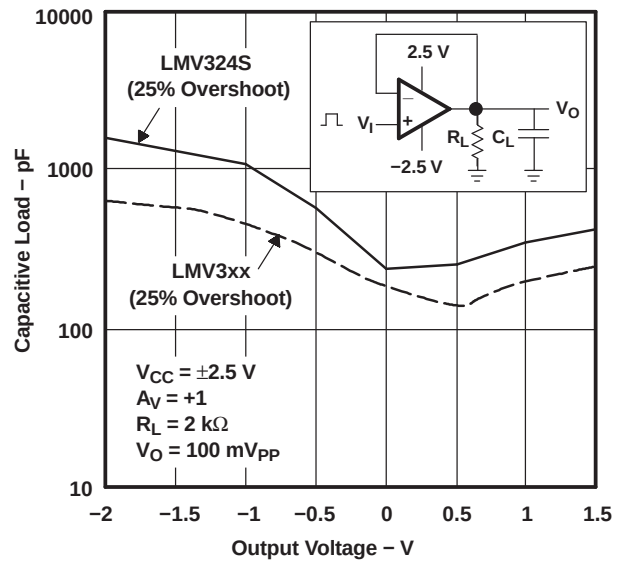


Figure 6.

STABILITY
VS
CAPACITIVE LOAD

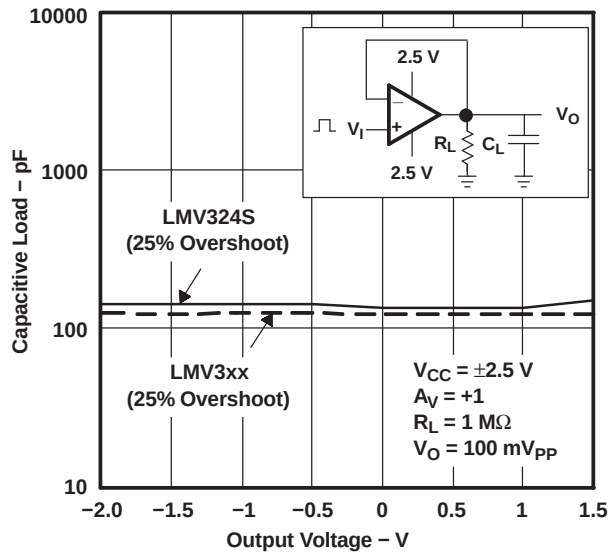


Figure 7.

STABILITY
VS
CAPACITIVE LOAD

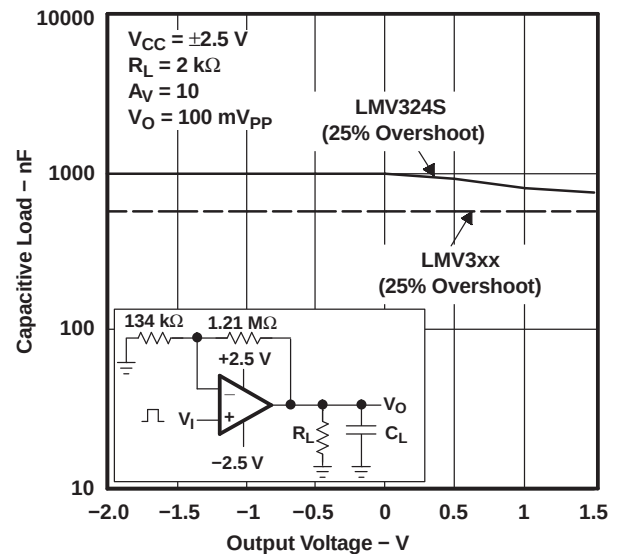
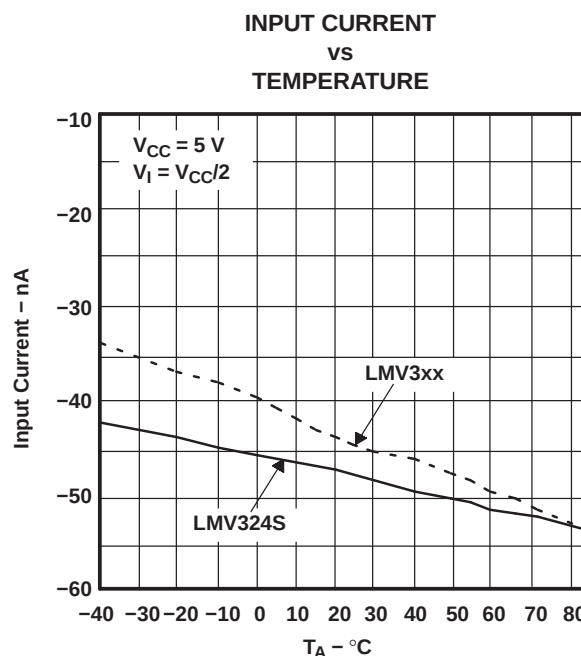
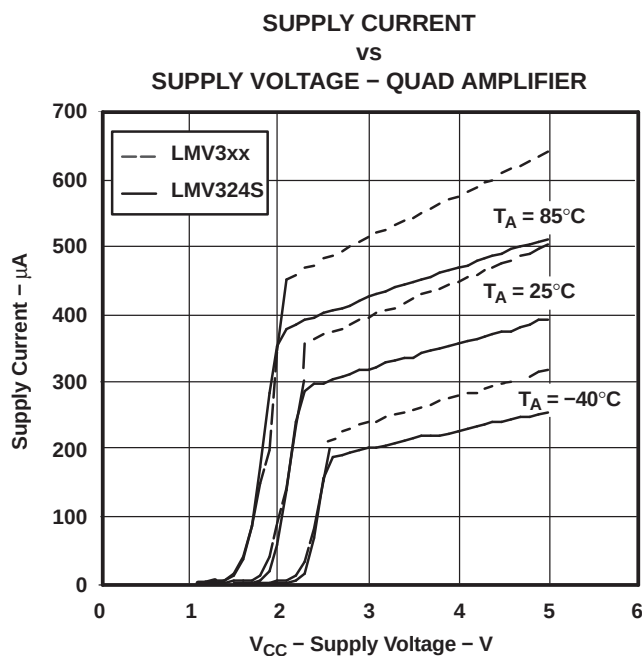
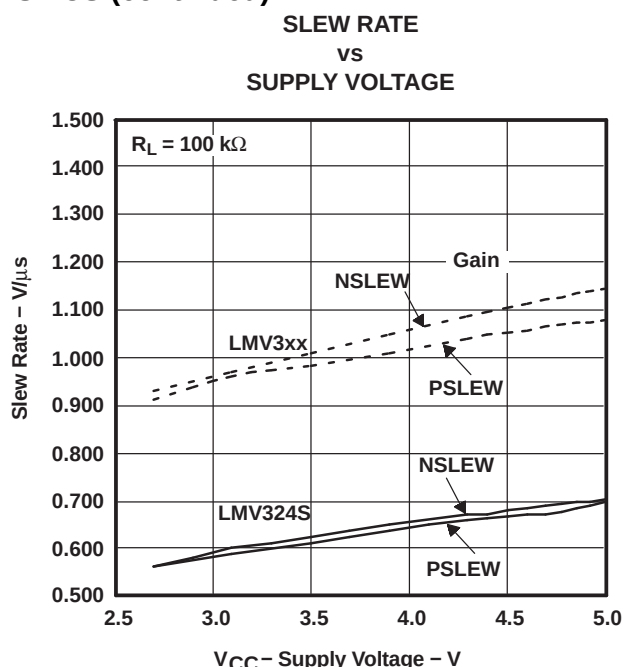
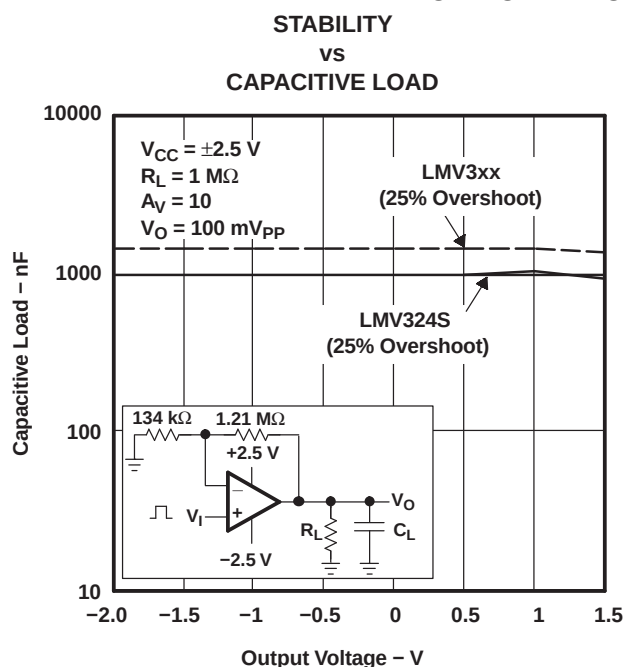
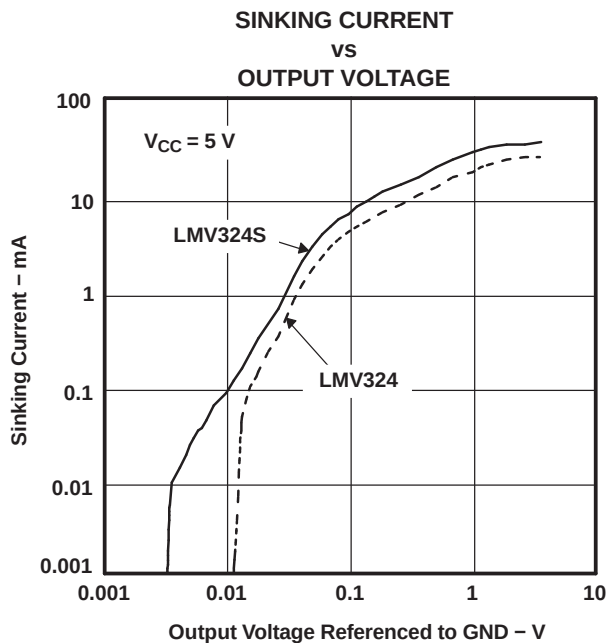
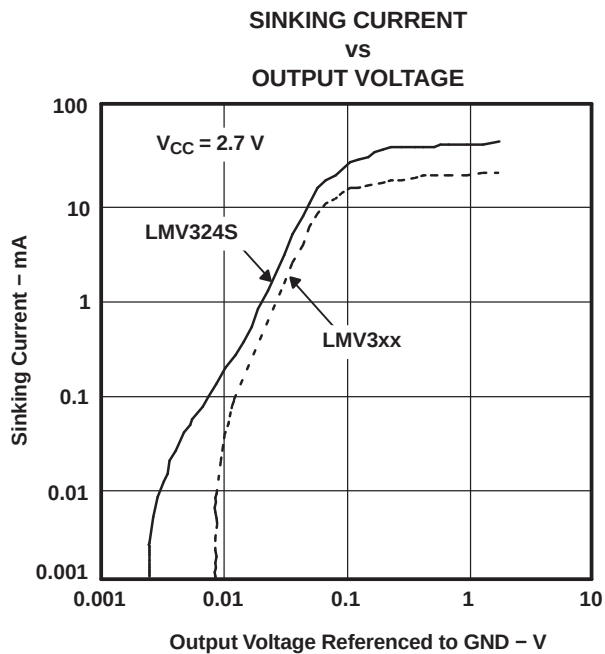
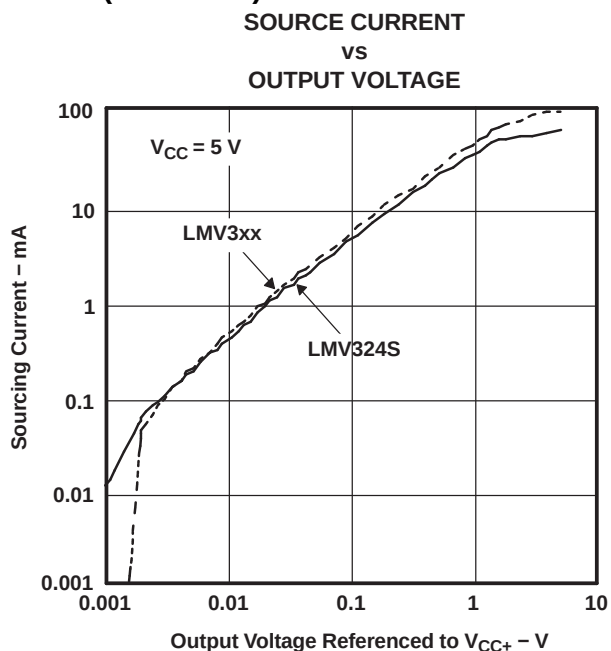
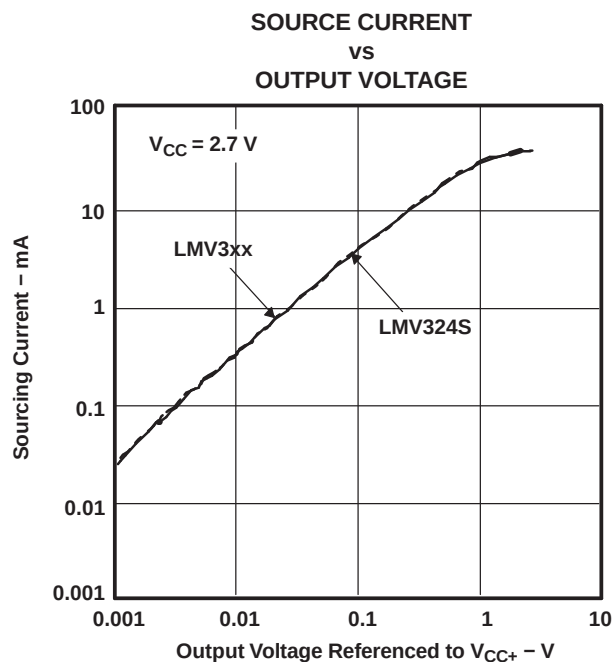


Figure 8.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

SHORT-CIRCUIT CURRENT
VS
TEMPERATURE

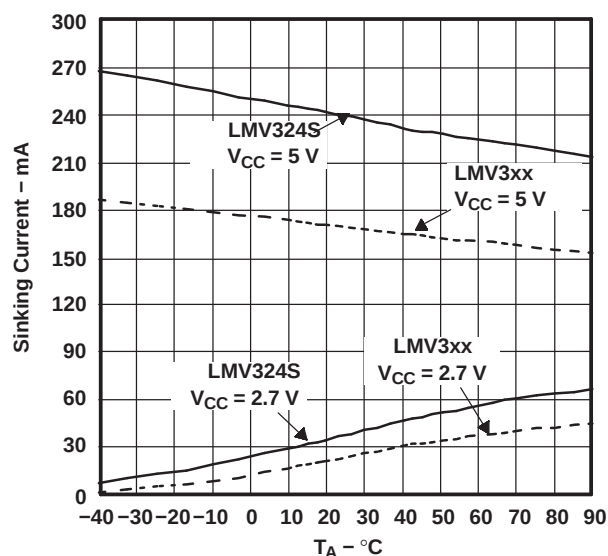


Figure 17.

SHORT-CIRCUIT CURRENT
VS
TEMPERATURE

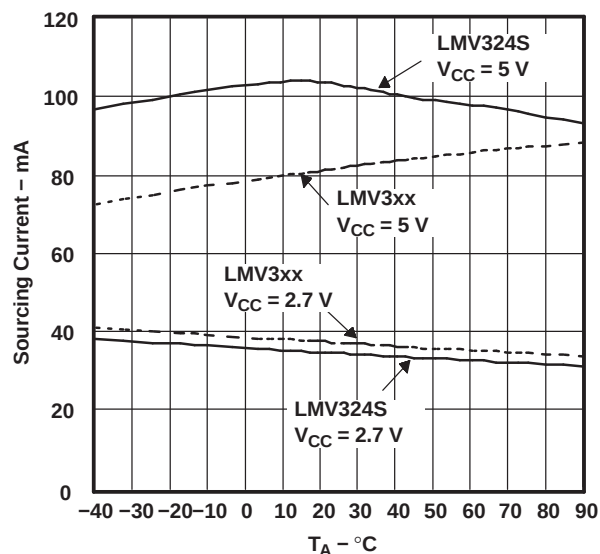


Figure 18.

$-k_{SVR}$
VS
FREQUENCY

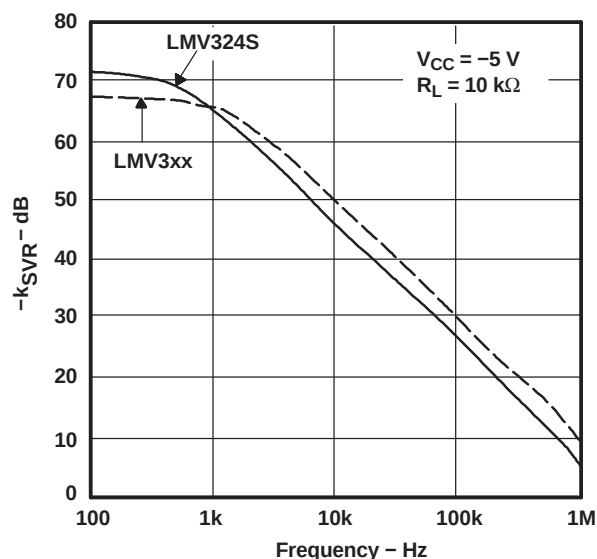


Figure 19.

$+k_{SVR}$
VS
FREQUENCY

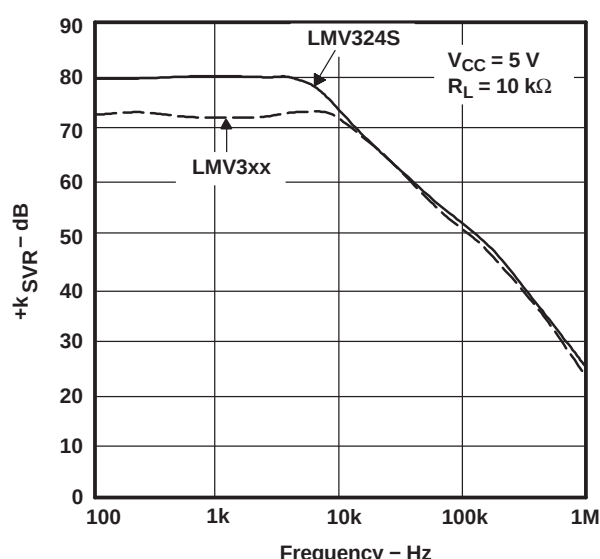
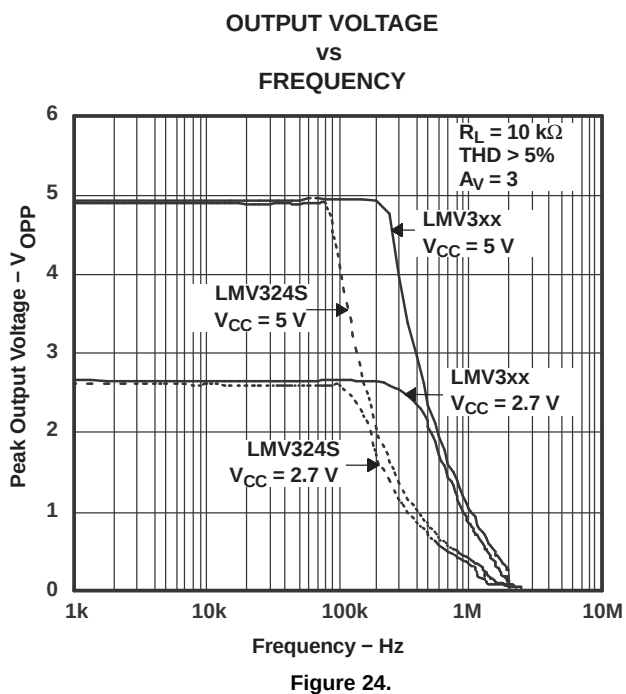
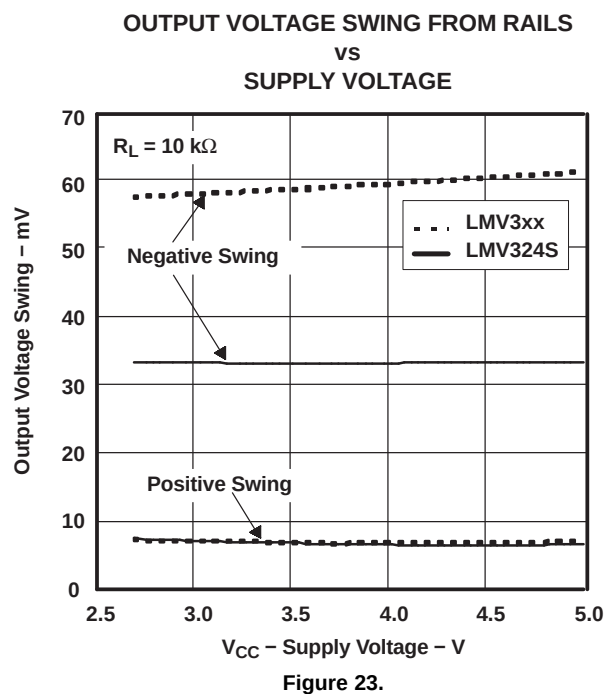
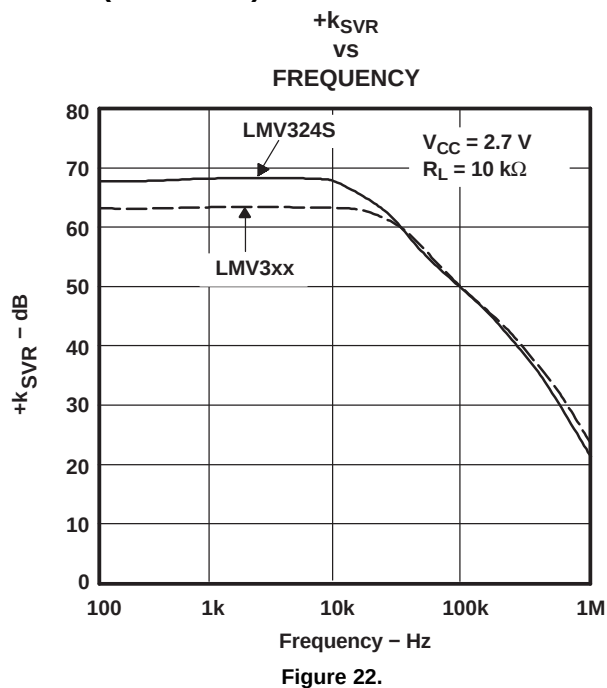
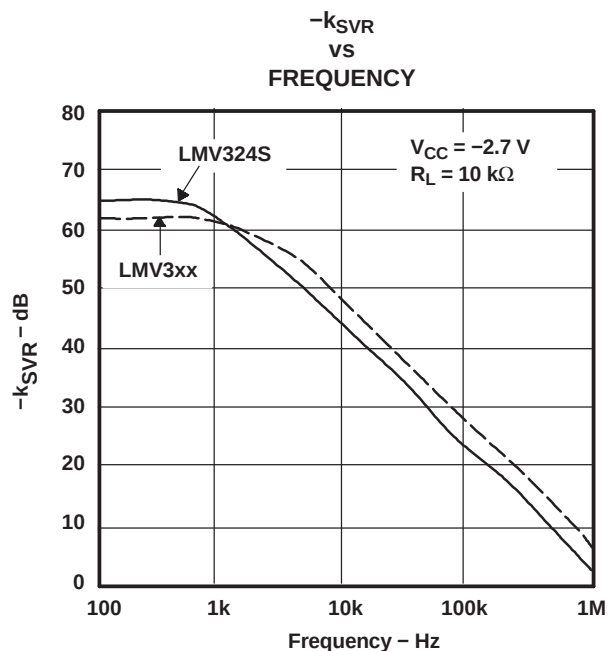


Figure 20.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

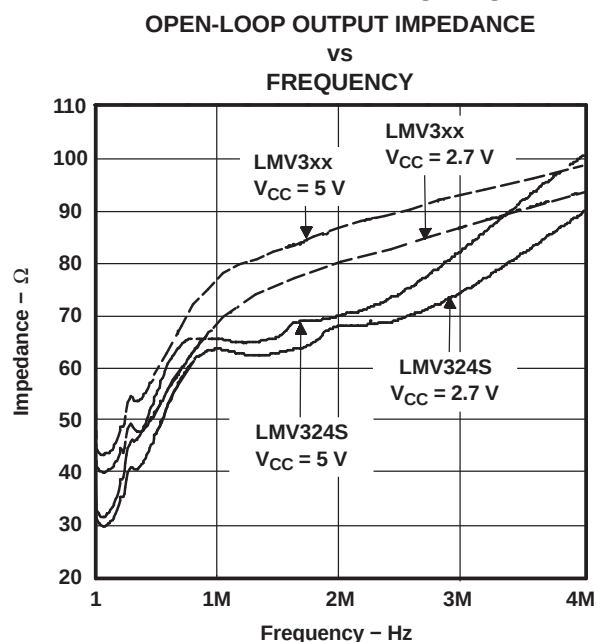


Figure 25.

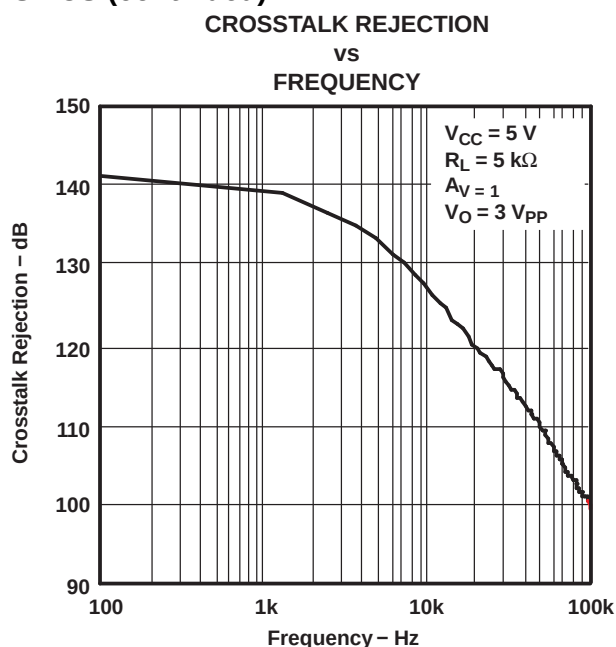


Figure 26.

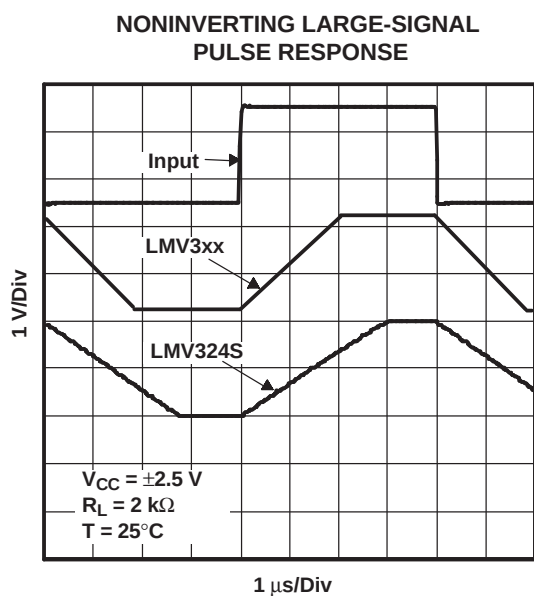


Figure 27.

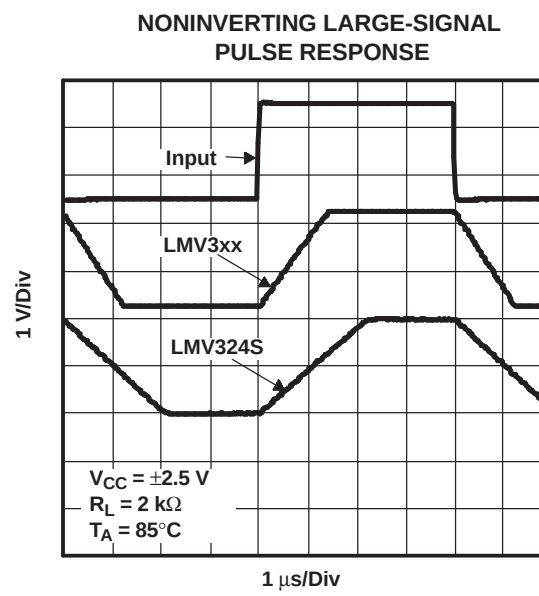
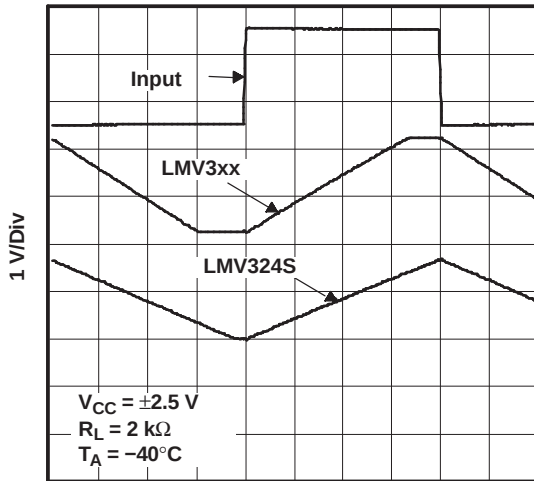


Figure 28.

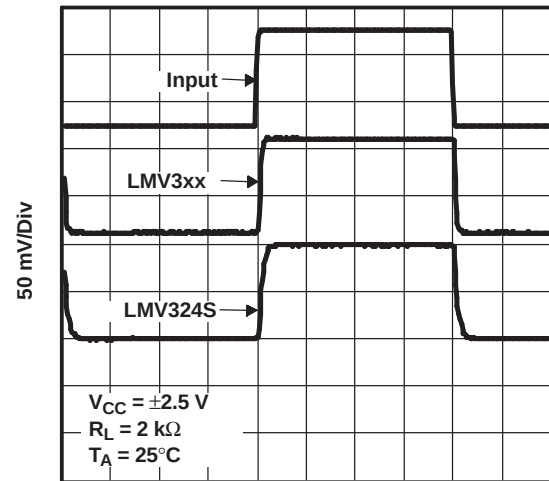
TYPICAL CHARACTERISTICS (continued)

**NONINVERTING LARGE-SIGNAL
PULSE RESPONSE**



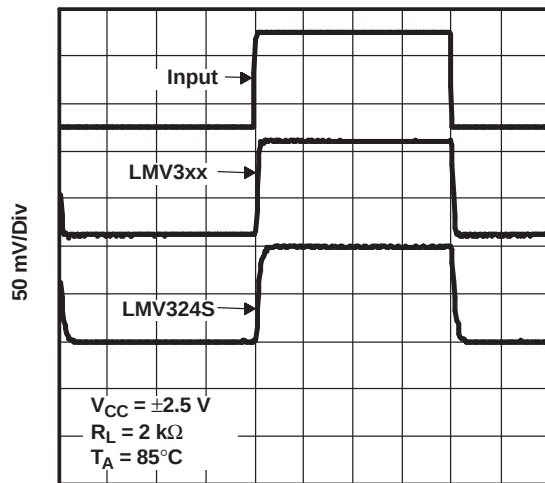
1 $\mu\text{s}/\text{Div}$
Figure 29.

**NONINVERTING SMALL-SIGNAL
PULSE RESPONSE**



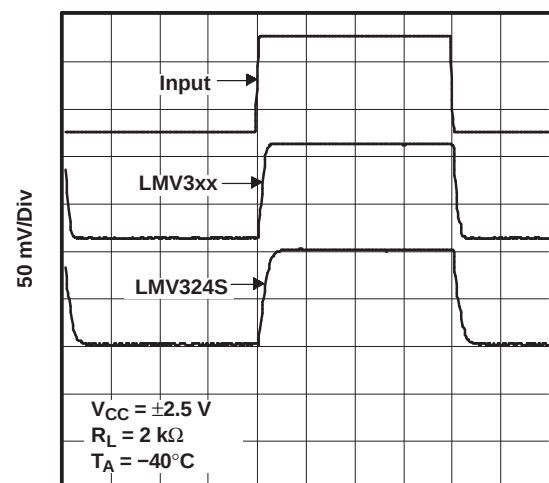
1 $\mu\text{s}/\text{Div}$
Figure 30.

**NONINVERTING SMALL-SIGNAL
PULSE RESPONSE**



1 $\mu\text{s}/\text{Div}$
Figure 31.

**NONINVERTING SMALL-SIGNAL
PULSE RESPONSE**



1 $\mu\text{s}/\text{Div}$
Figure 32.

TYPICAL CHARACTERISTICS (continued)

INVERTING LARGE-SIGNAL
PULSE RESPONSE

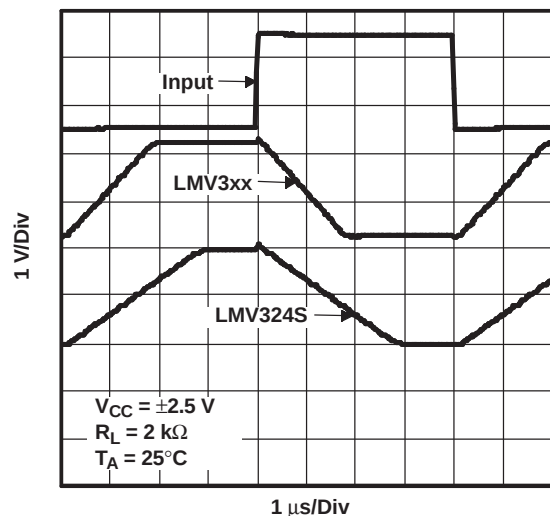


Figure 33.

INVERTING LARGE-SIGNAL
PULSE RESPONSE

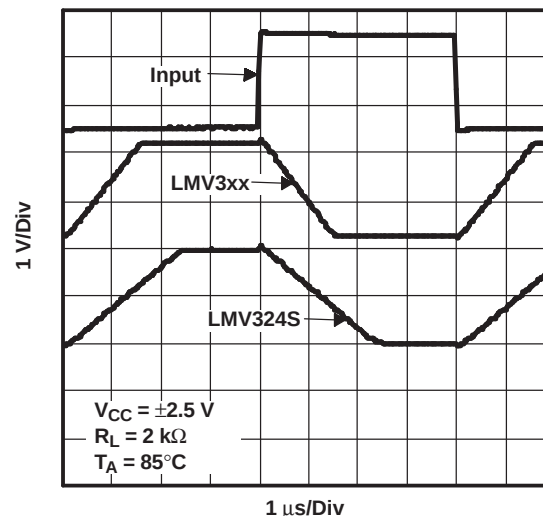


Figure 34.

INVERTING LARGE-SIGNAL
PULSE RESPONSE

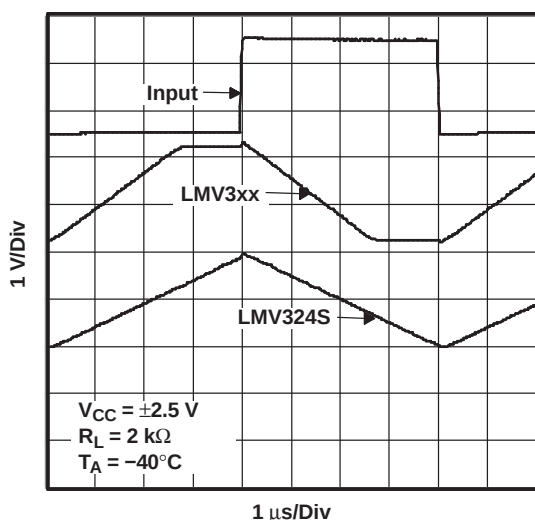


Figure 35.

INVERTING SMALL-SIGNAL
PULSE RESPONSE

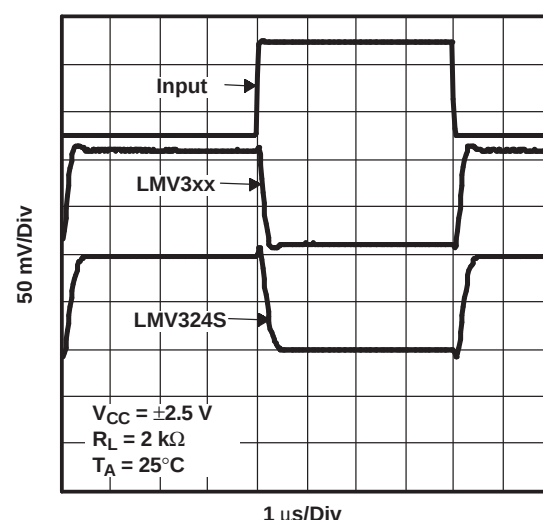


Figure 36.

TYPICAL CHARACTERISTICS (continued)

INVERTING SMALL-SIGNAL PULSE RESPONSE

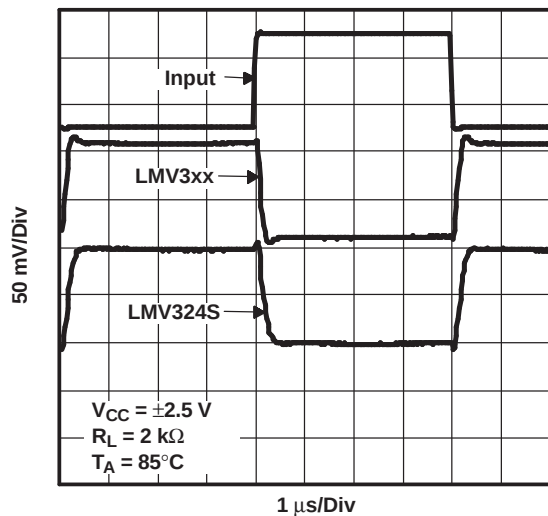


Figure 37.

INVERTING SMALL-SIGNAL PULSE RESPONSE

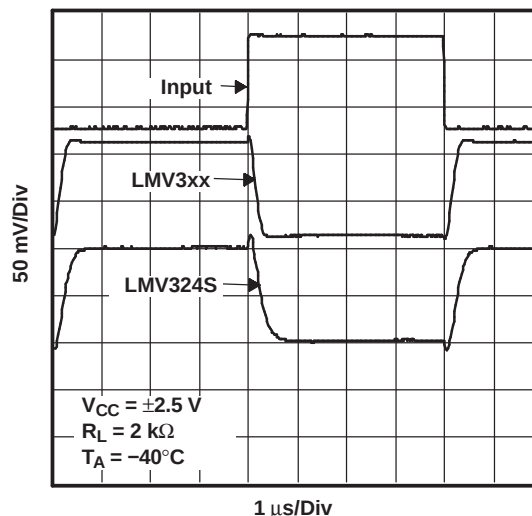


Figure 38.

INPUT CURRENT NOISE vs FREQUENCY

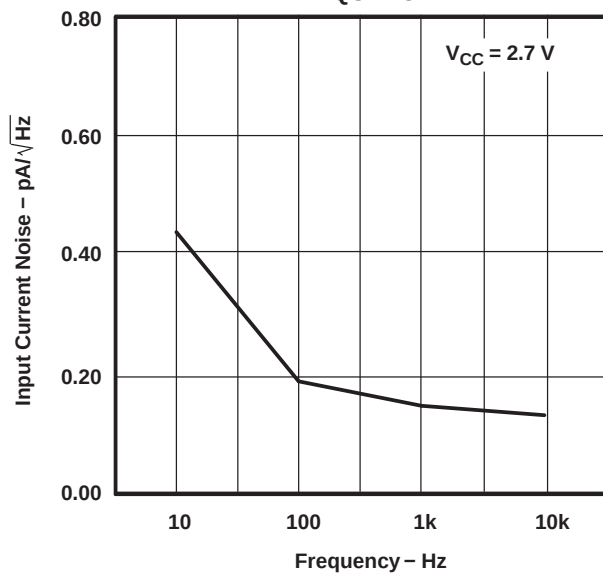


Figure 39.

INPUT CURRENT NOISE vs FREQUENCY

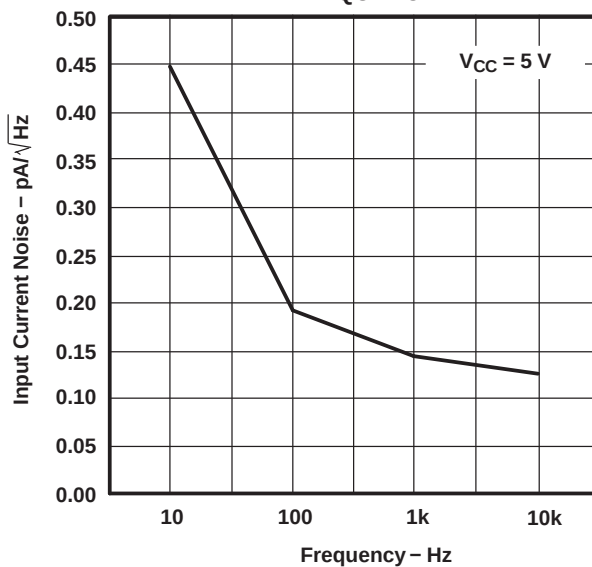


Figure 40.

TYPICAL CHARACTERISTICS (continued)

INPUT VOLTAGE NOISE
vs
FREQUENCY

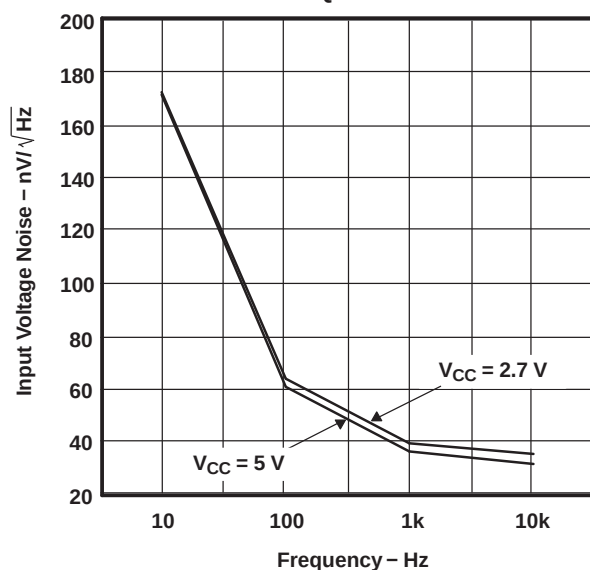


Figure 41.

THD + N
vs
FREQUENCY

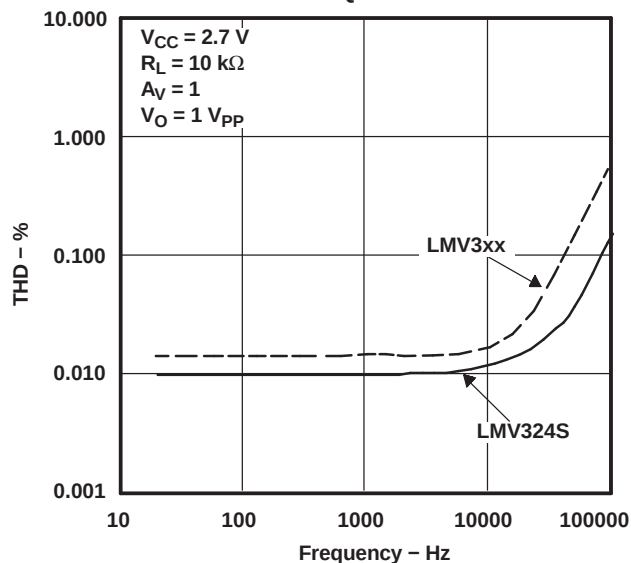


Figure 42.

THD + N
vs
FREQUENCY

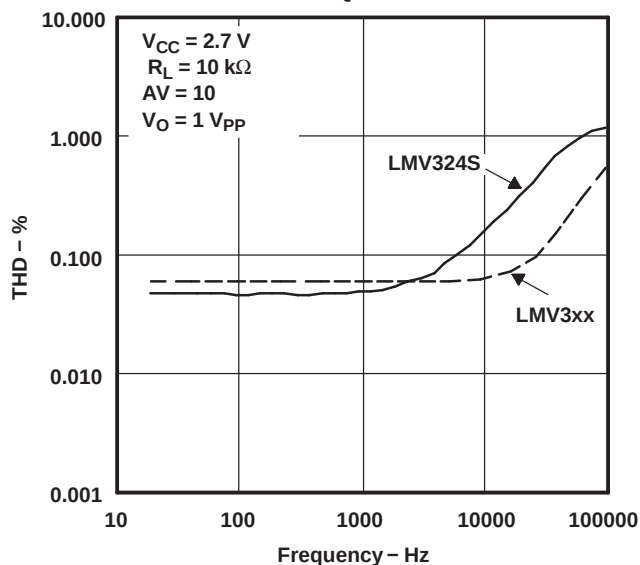


Figure 43.

THD + N
vs
FREQUENCY

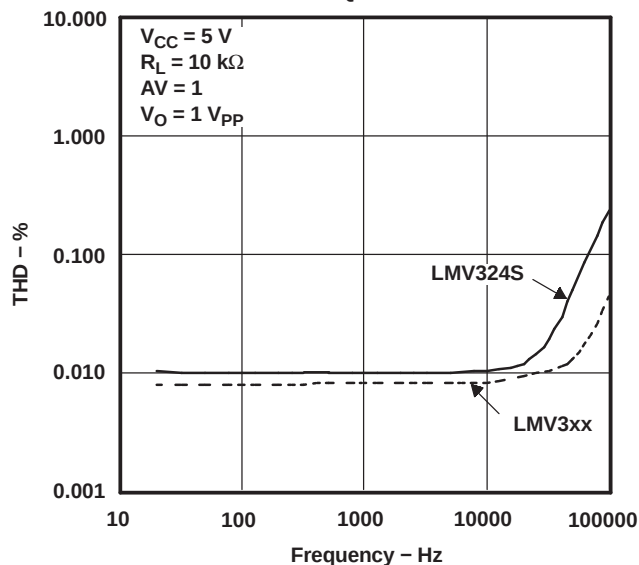
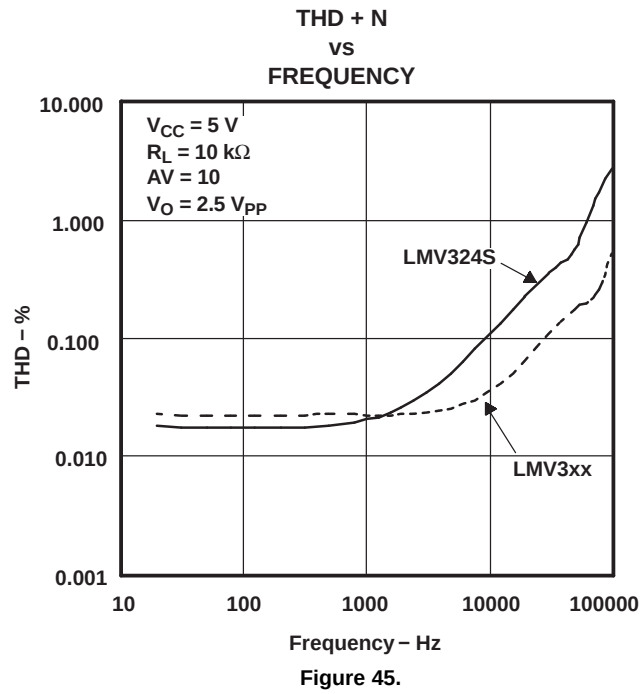


Figure 44.

TYPICAL CHARACTERISTICS (continued)



REVISION HISTORY

Changes from Revision T (September 2007) to Revision U	Page
• Updated θ_{JA} value for DDU package.	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV321IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321IDBVT E4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321IDCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321IDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IPWRE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV324QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324SID	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
LMV324SIDE4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
LMV324SIDG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
LMV324SIDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
LMV324SIDRE4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
LMV324SIDRG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
LMV324SIPWR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	
LMV324SIPWRE4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	
LMV324SIPWRG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	
LMV358ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDDURE4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV358IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDDURE4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV358QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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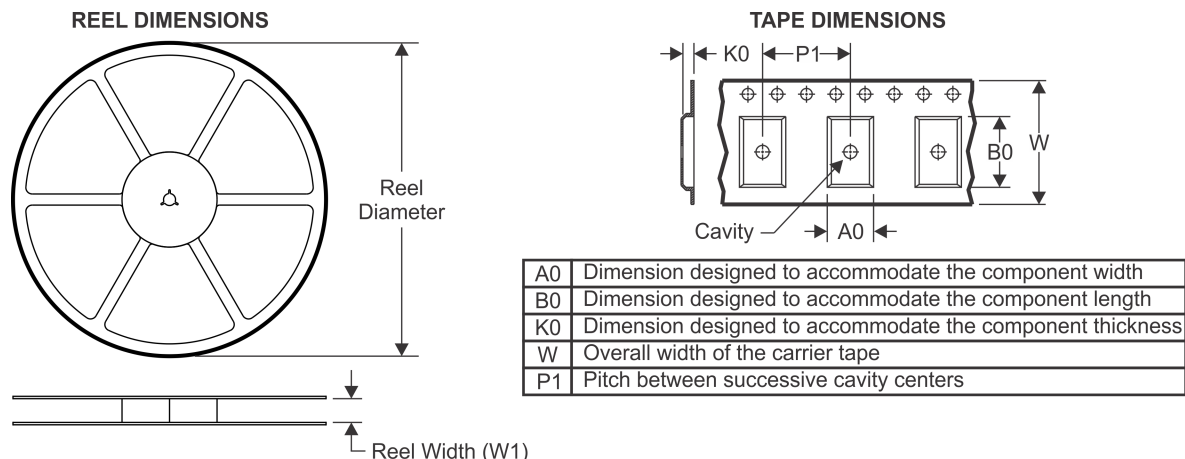
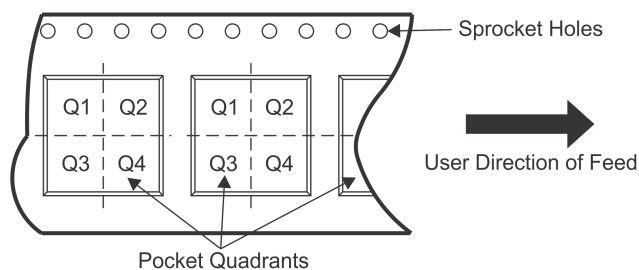
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV324, LMV358 :

- Automotive: [LMV324-Q1](#), [LMV358-Q1](#)

NOTE: Qualified Version Definitions:

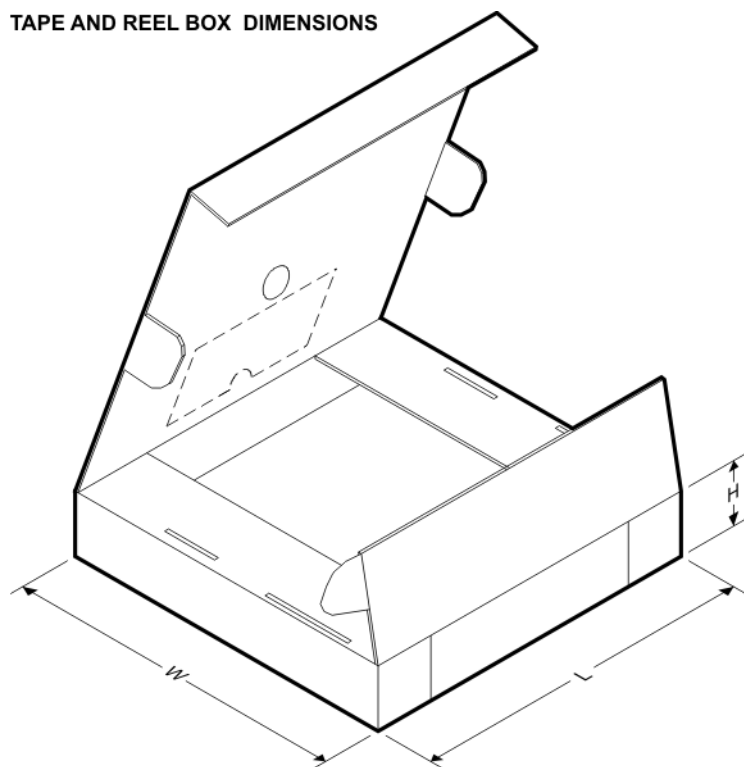
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV321IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV321IDBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
LMV321IDBVT	SOT-23	DBV	5	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
LMV321IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV321IDCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV321IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV321IDCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV321IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324IPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
LMV324IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324QPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV358IDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LMV358IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV358IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358IPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358QDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LMV358QDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


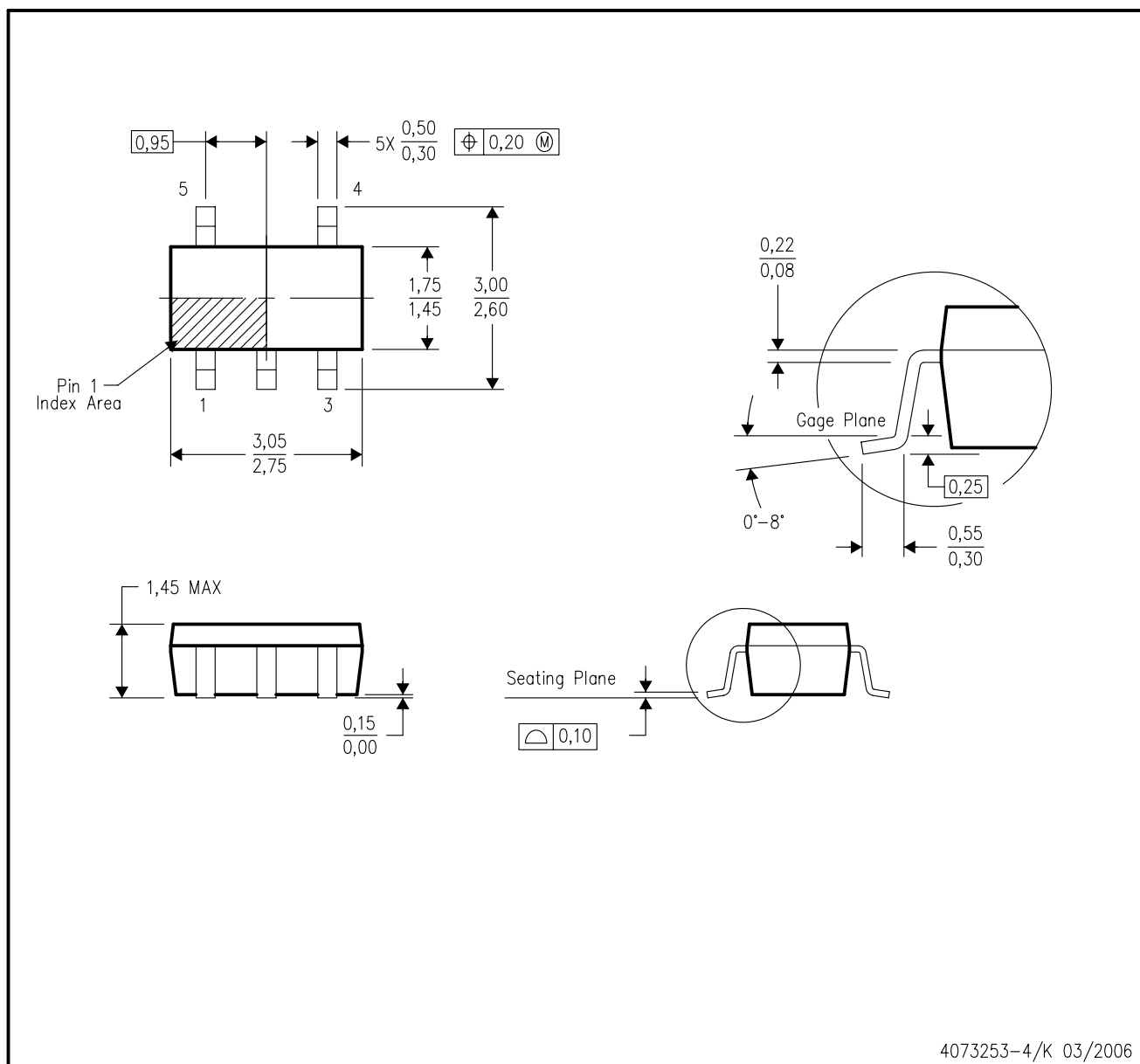
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV321IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LMV321IDBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
LMV321IDBVT	SOT-23	DBV	5	250	205.0	200.0	33.0
LMV321IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LMV321IDCKR	SC70	DCK	5	3000	205.0	200.0	33.0
LMV321IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV321IDCKT	SC70	DCK	5	250	205.0	200.0	33.0
LMV321IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
LMV324IDR	SOIC	D	14	2500	367.0	367.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV324IDR	SOIC	D	14	2500	333.2	345.9	28.6
LMV324IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LMV324IPWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LMV324IPWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
LMV324QDR	SOIC	D	14	2500	367.0	367.0	38.0
LMV324QPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LMV358IDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LMV358IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LMV358IDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV358IDR	SOIC	D	8	2500	367.0	367.0	35.0
LMV358IPWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LMV358IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LMV358IPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LMV358QDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LMV358QDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LMV358QDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV358QPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

DBV (R-PDSO-G5)

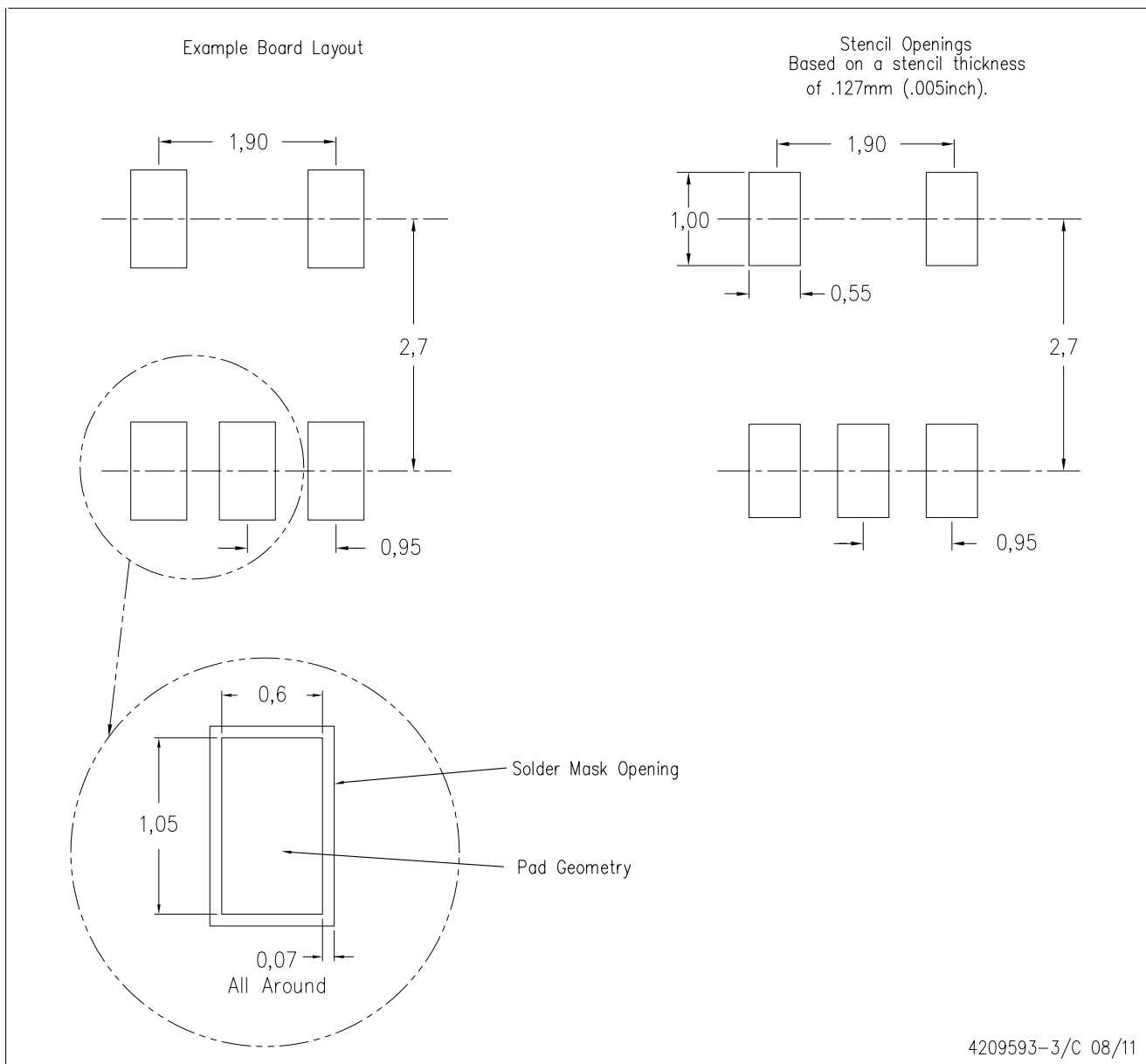
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

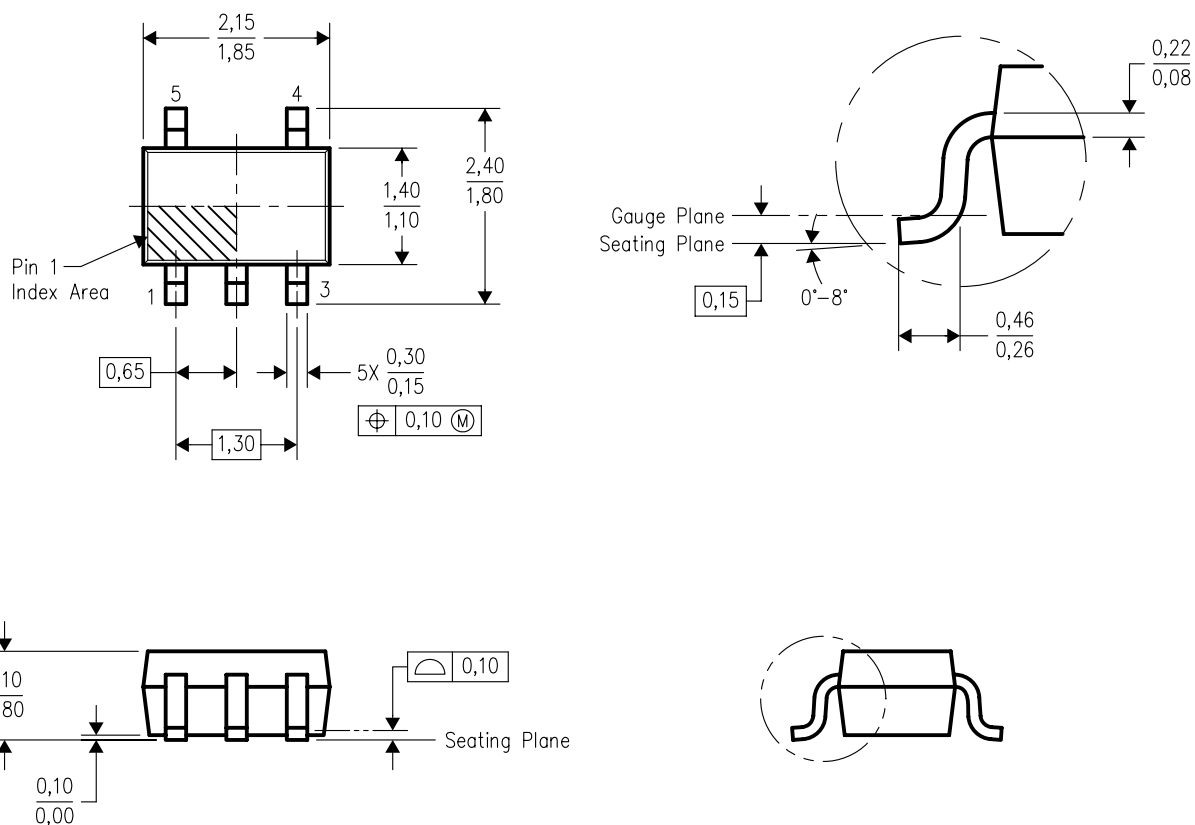
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

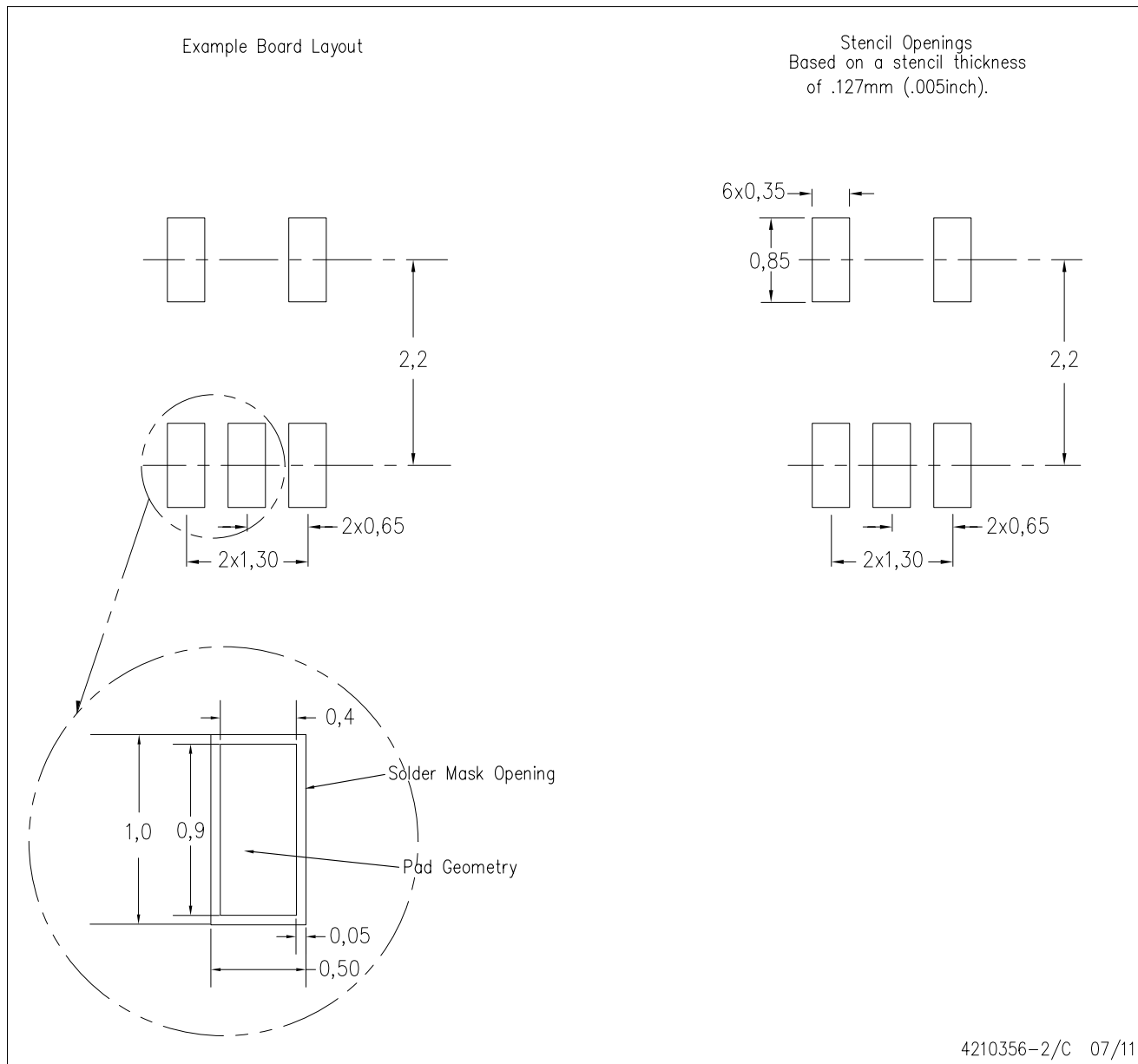


4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

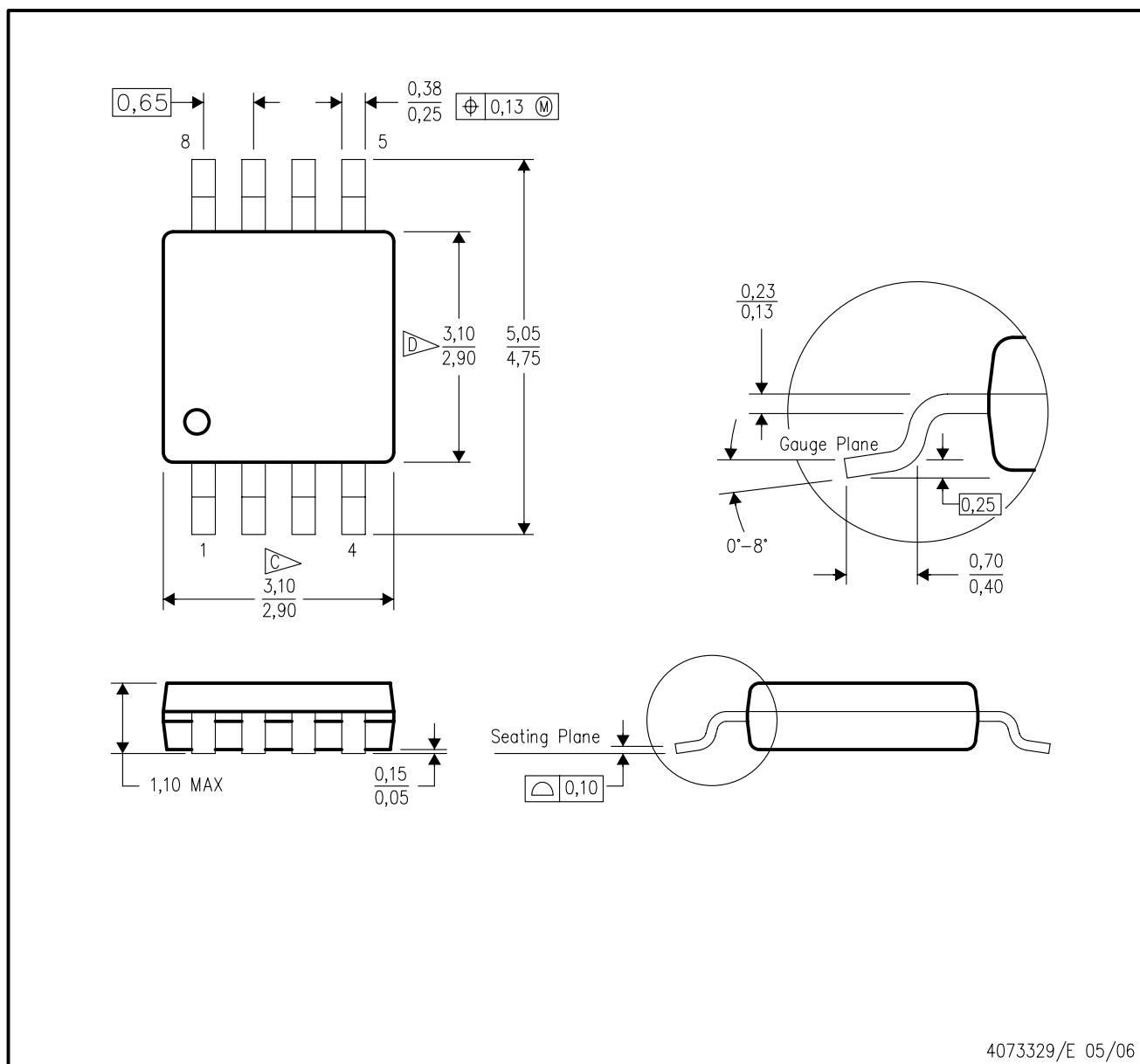
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

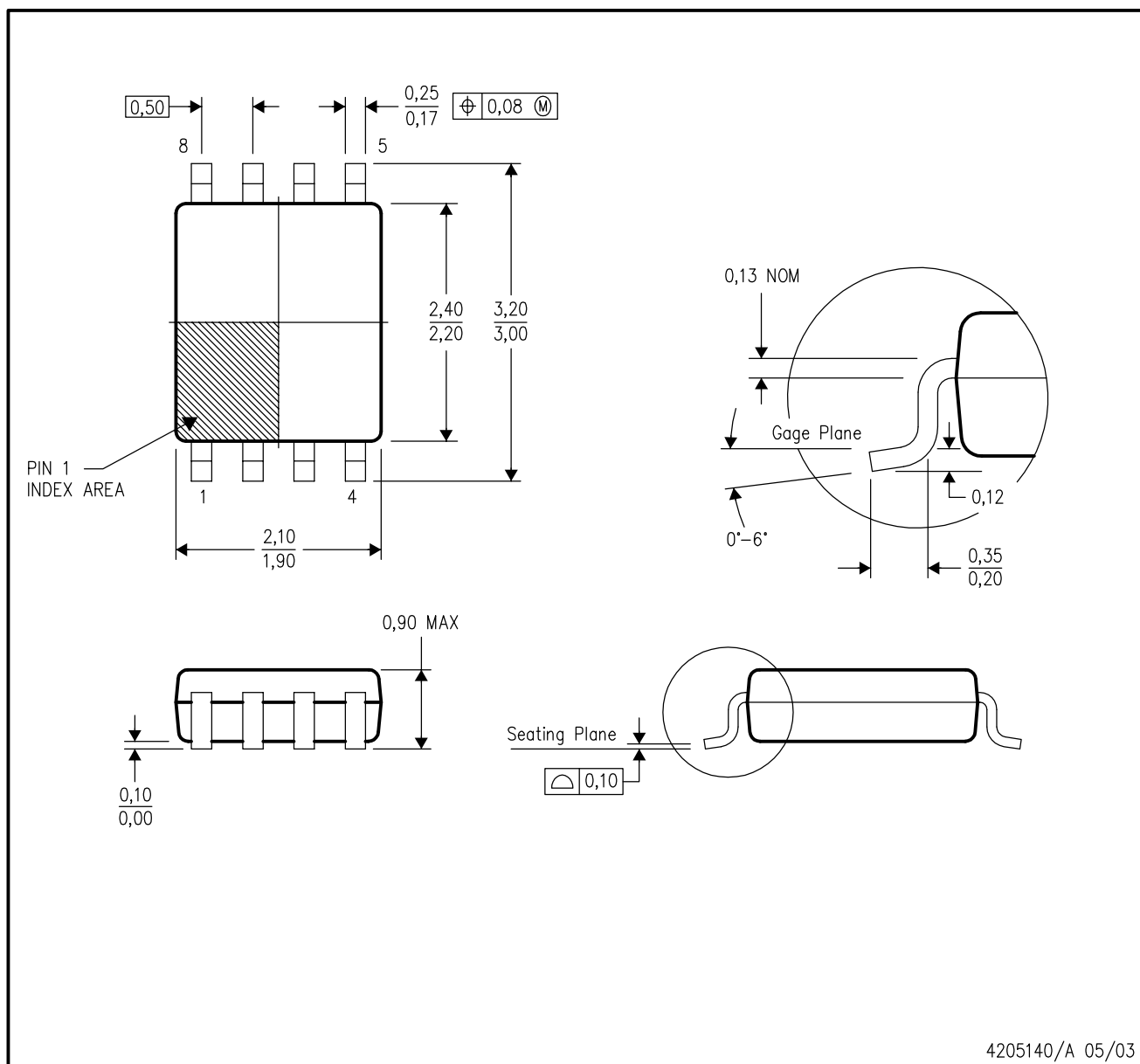


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DDU (R-PDSO-G8)

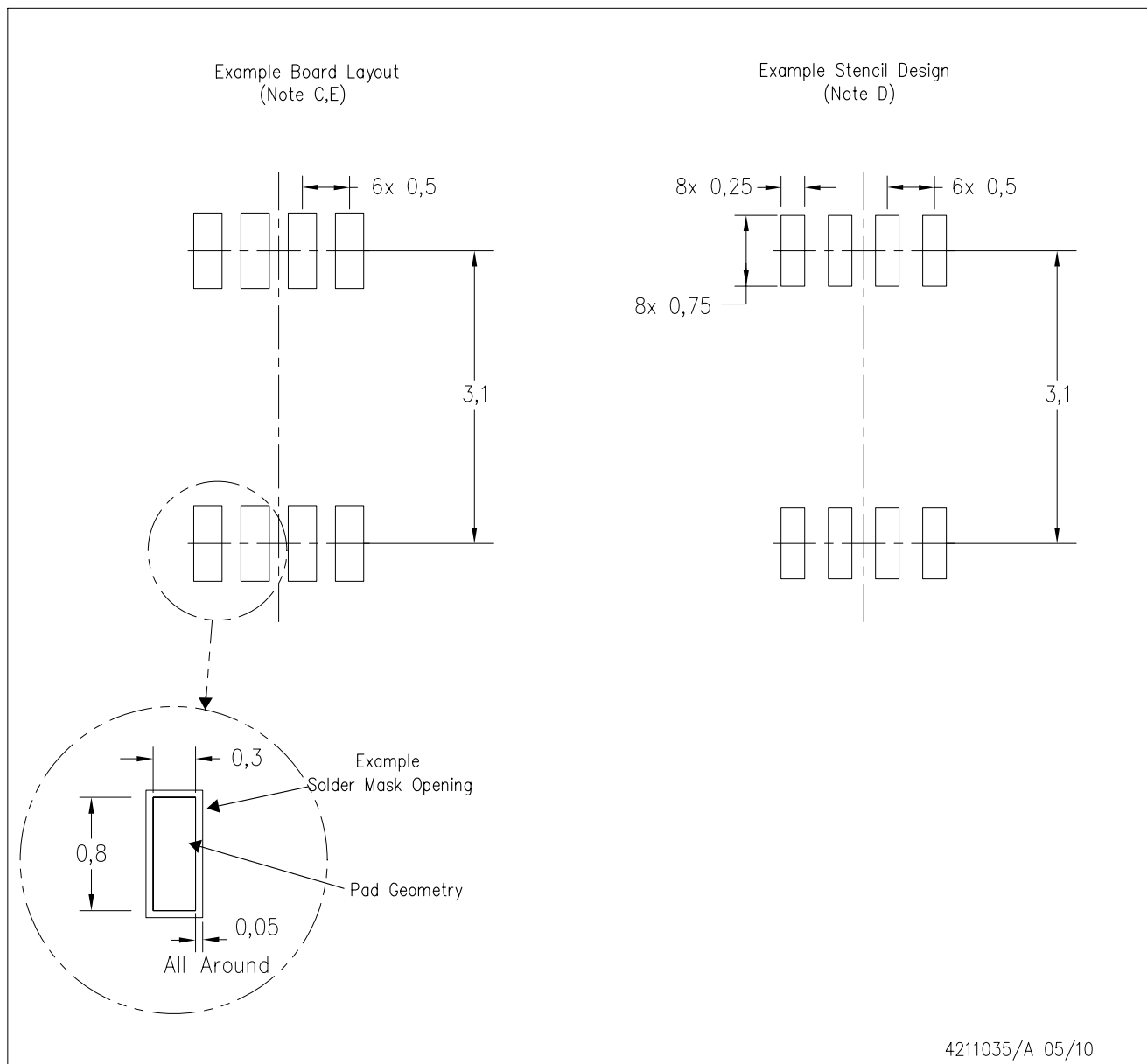
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation CA.

DDU (S-PDSO-G8)

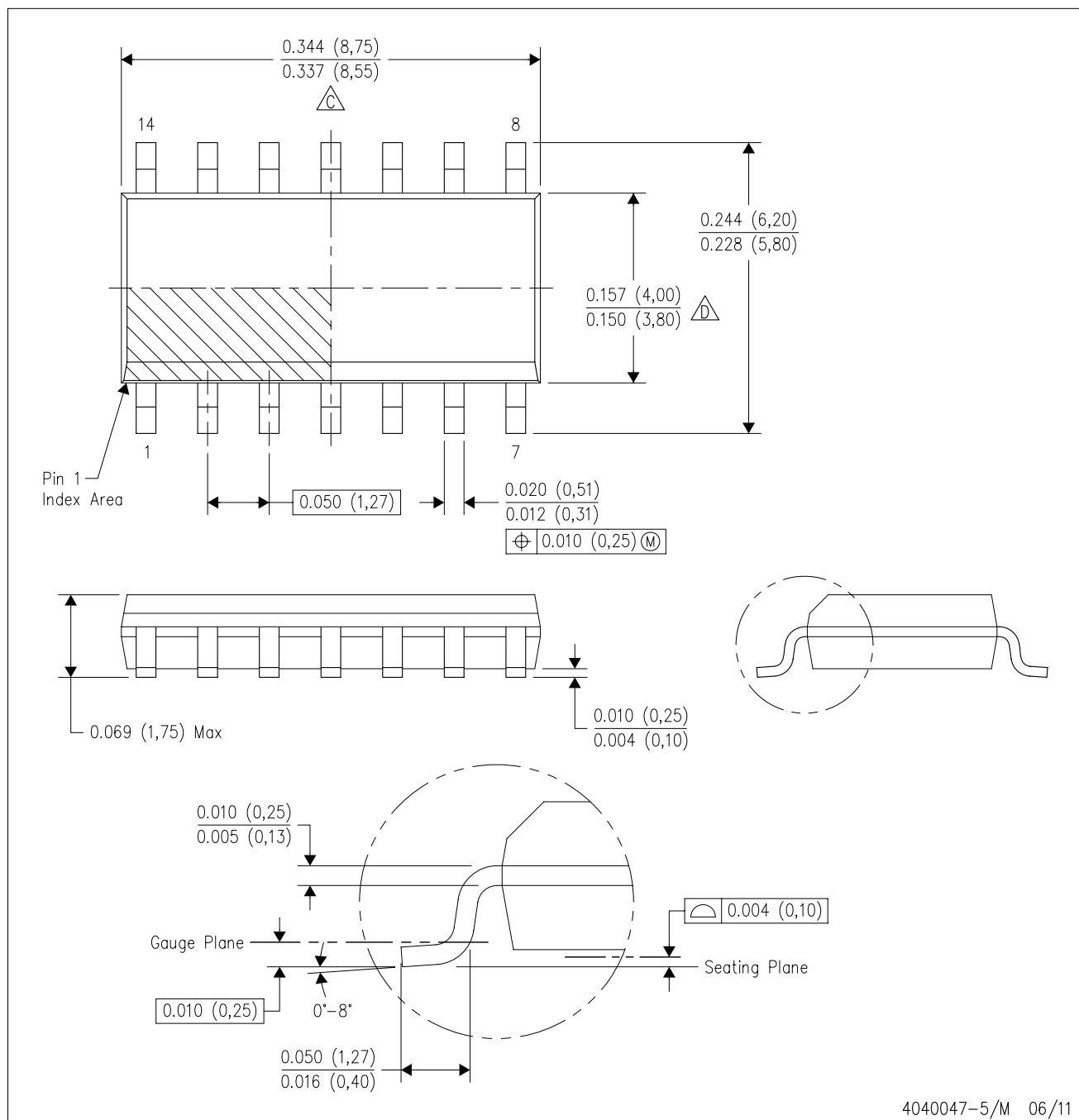
PLASTIC SMALL OUTLINE PACKAGE (DIE UP)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



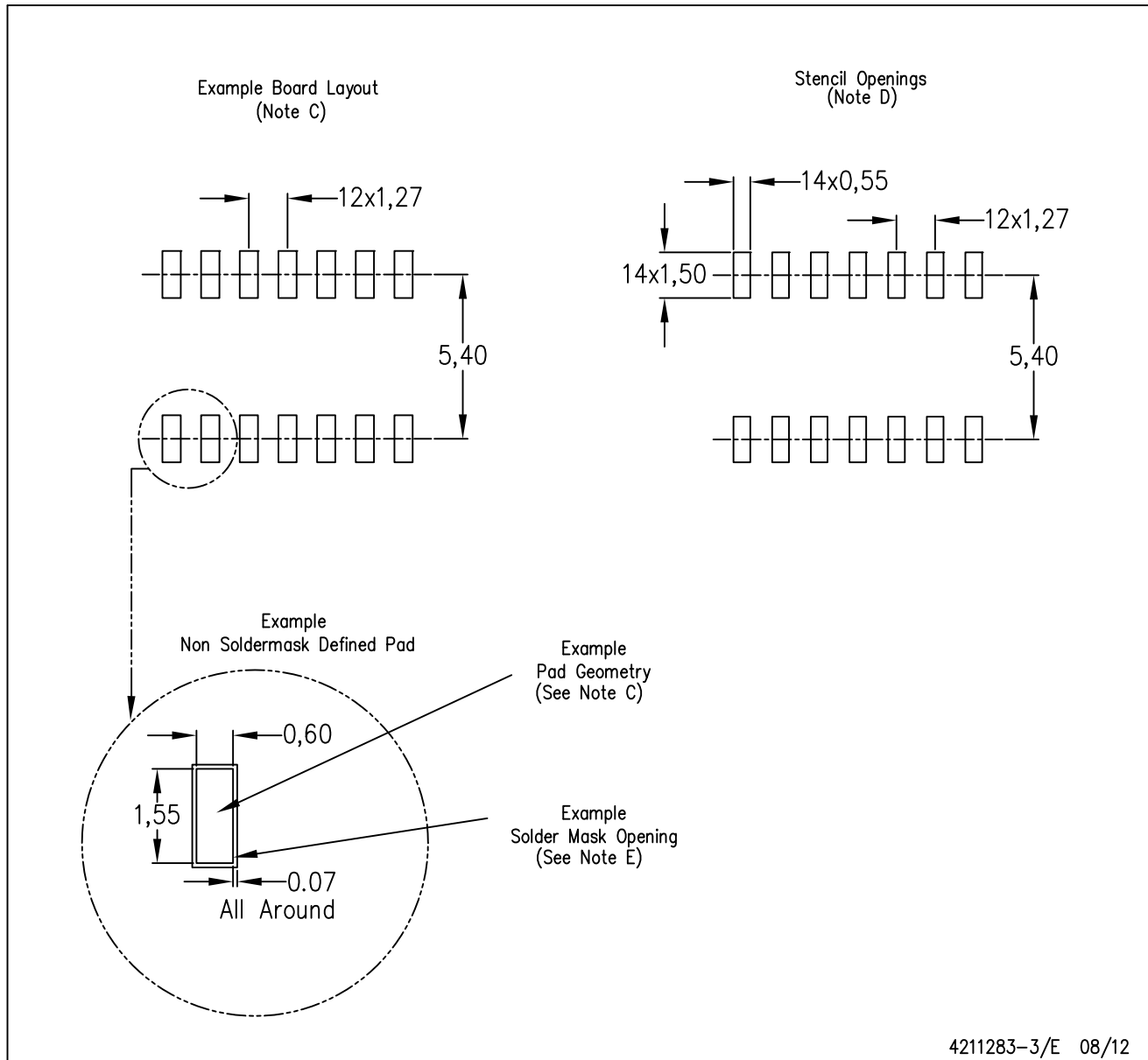
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

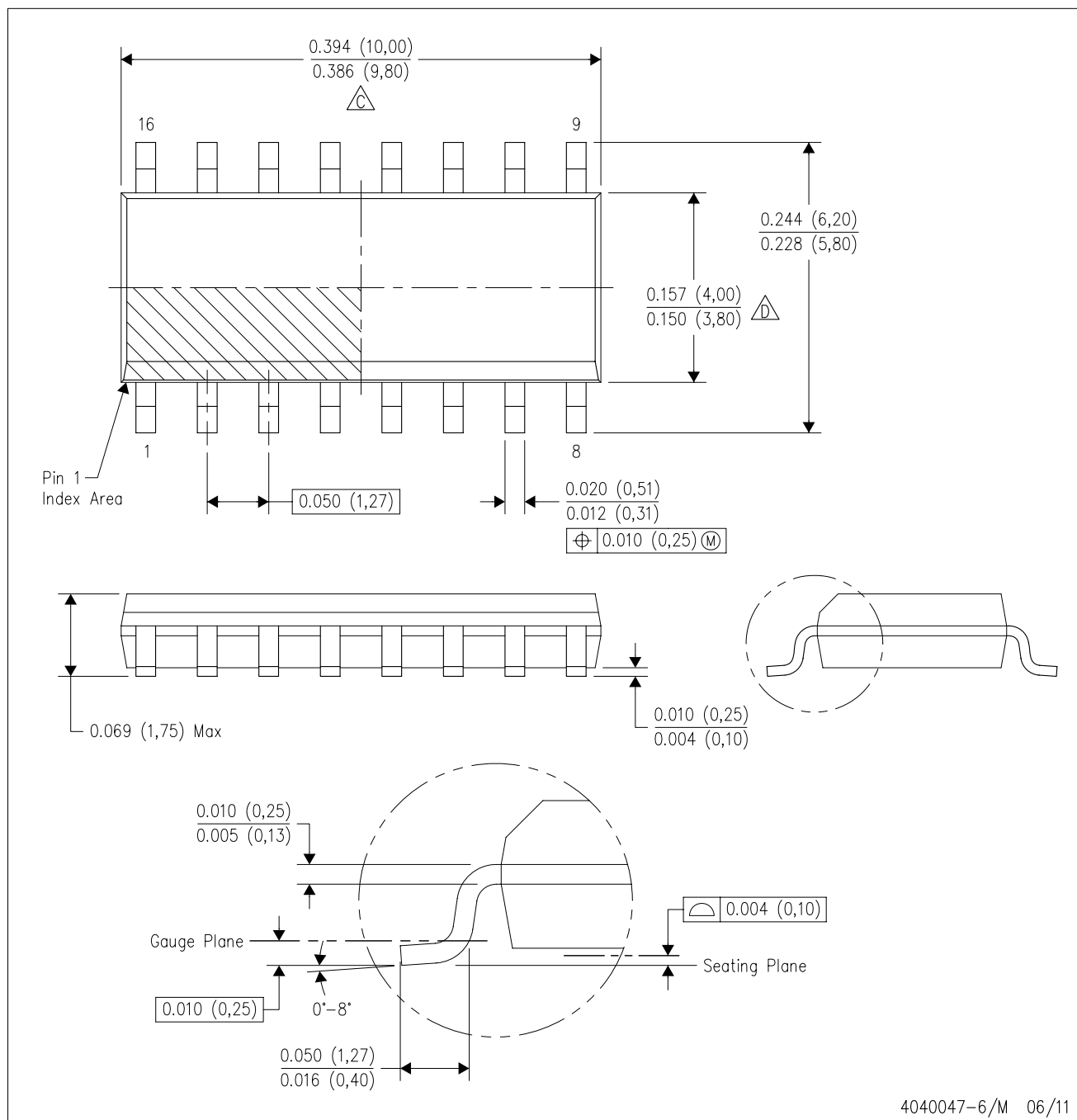
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

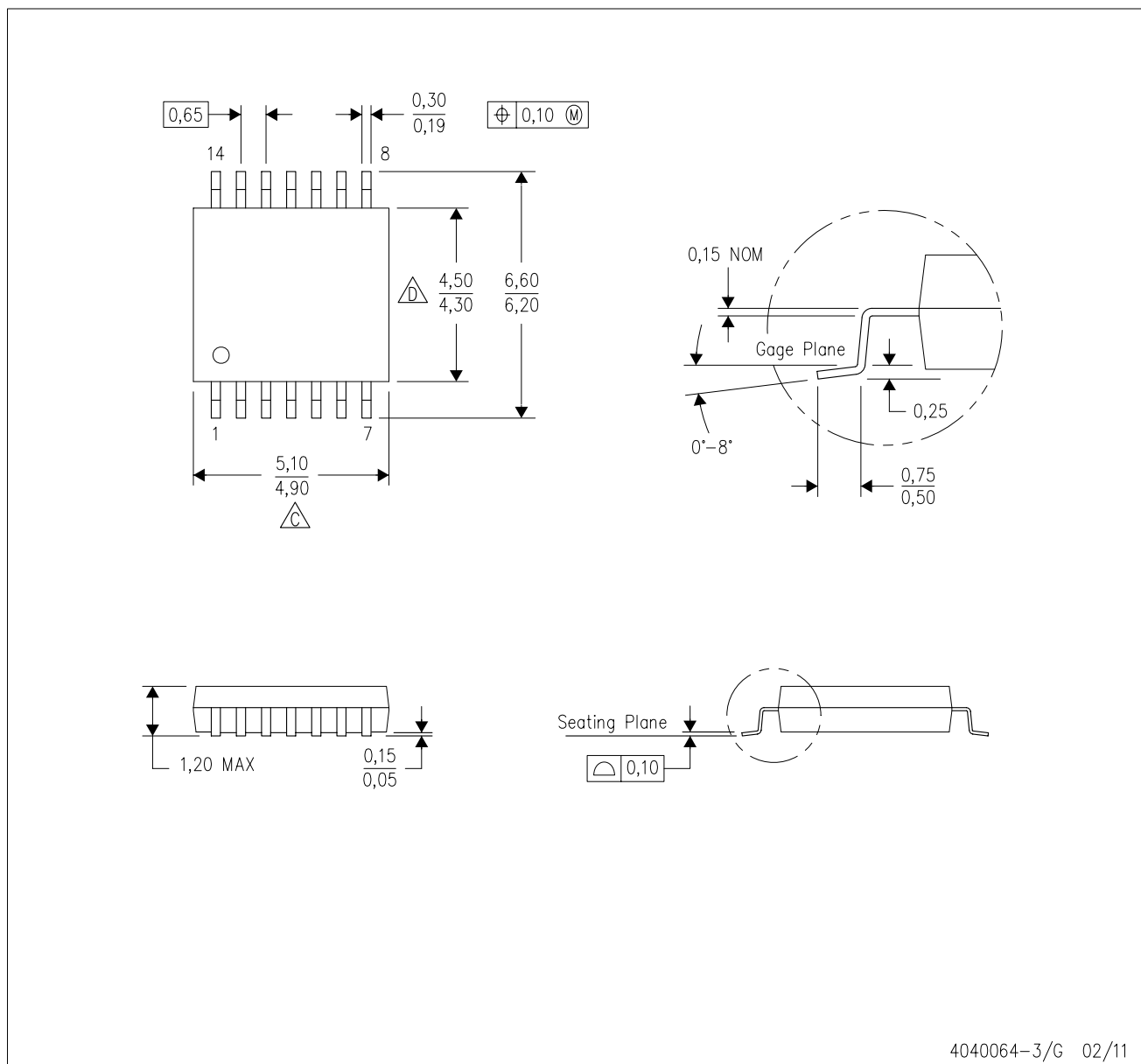


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G14)

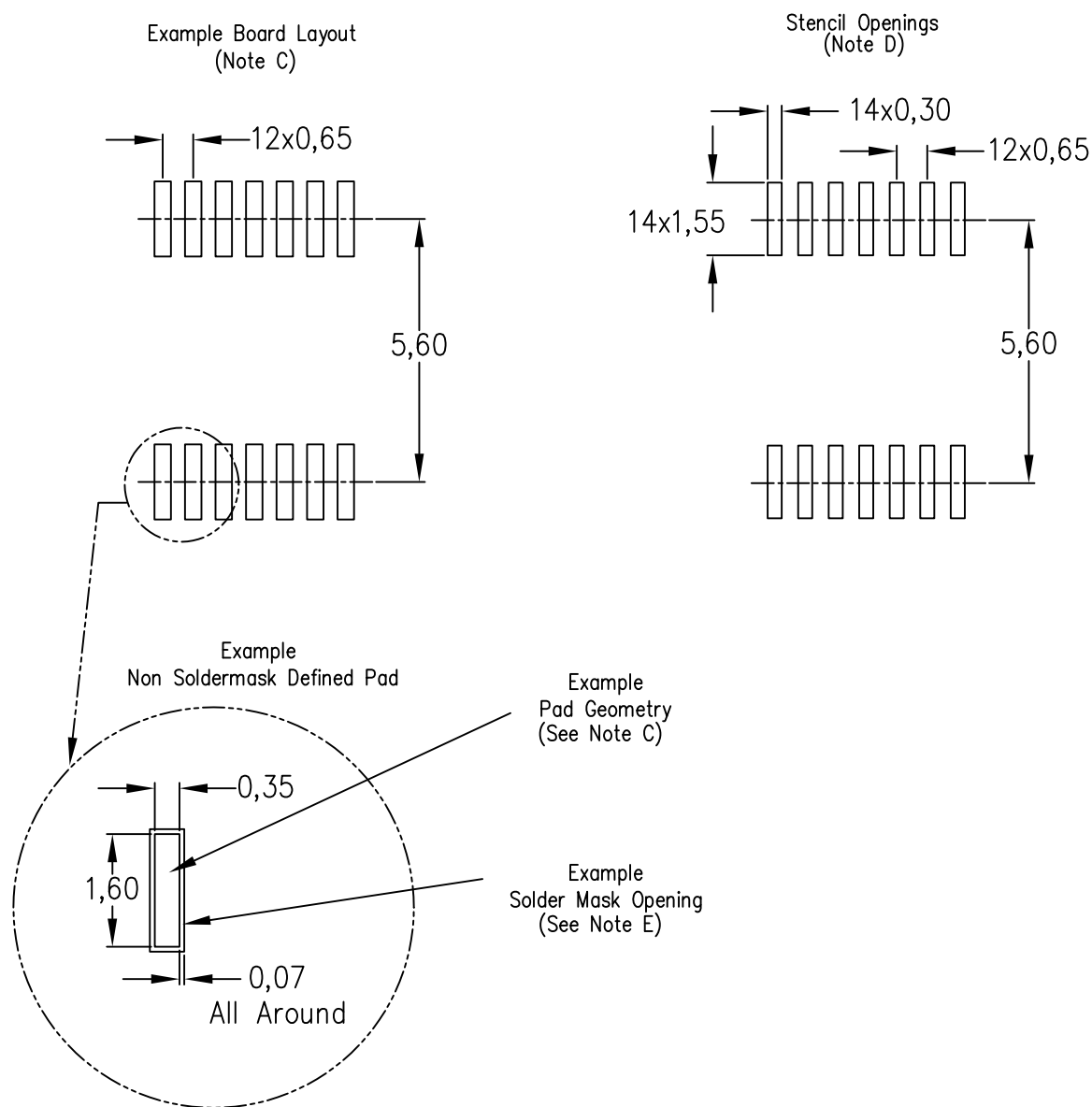
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

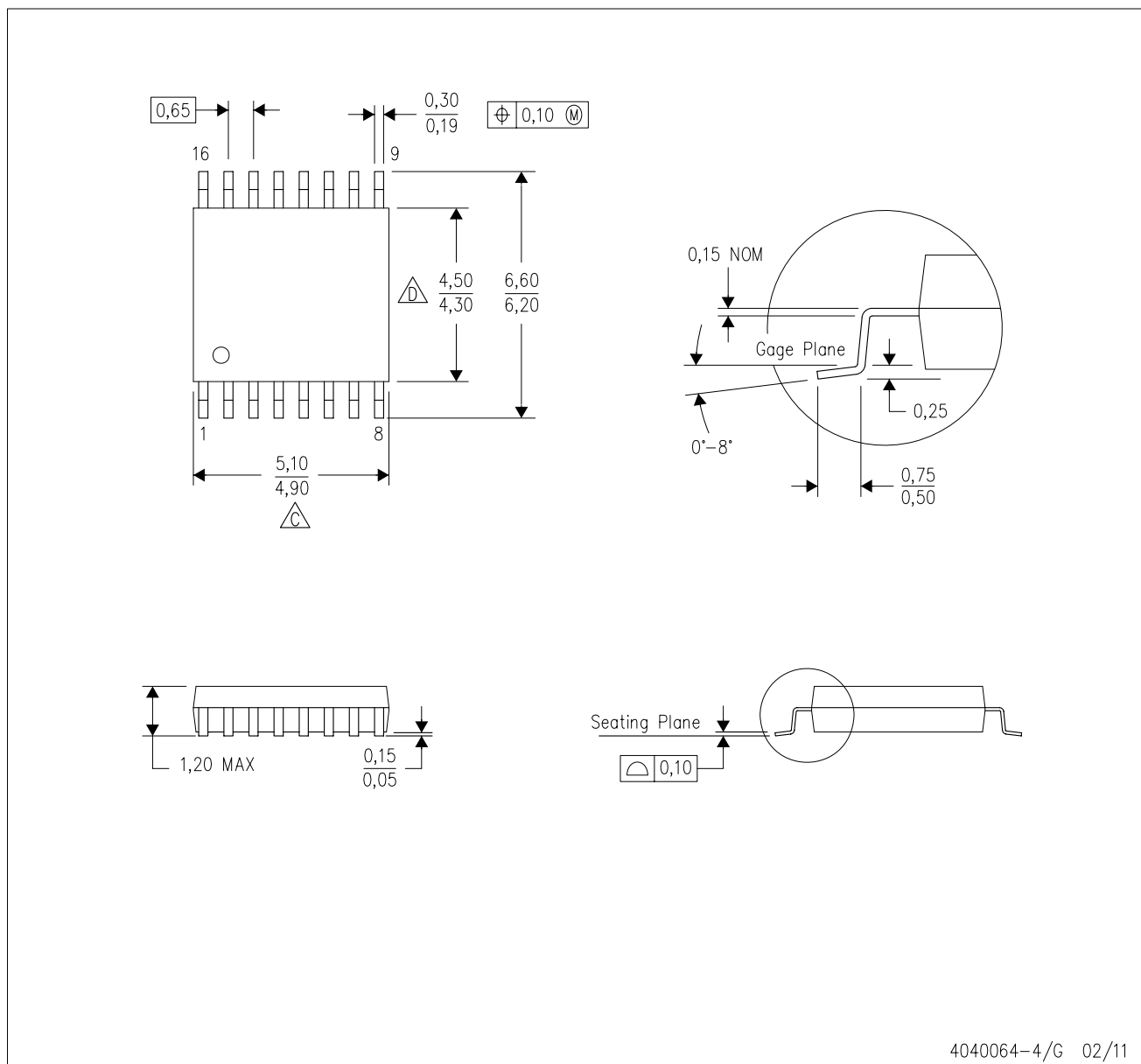


4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

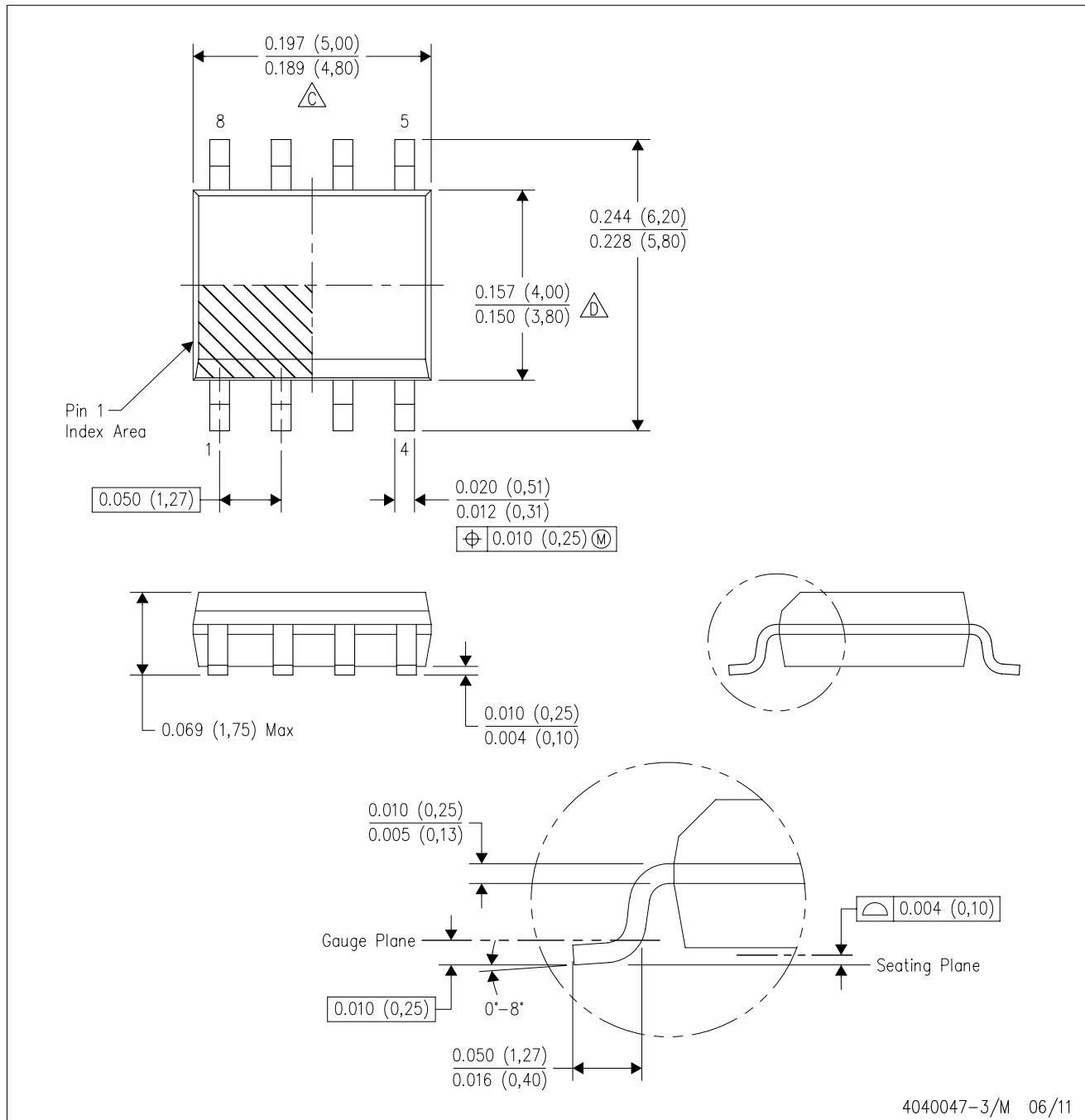
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

D (R-PDSO-G8)

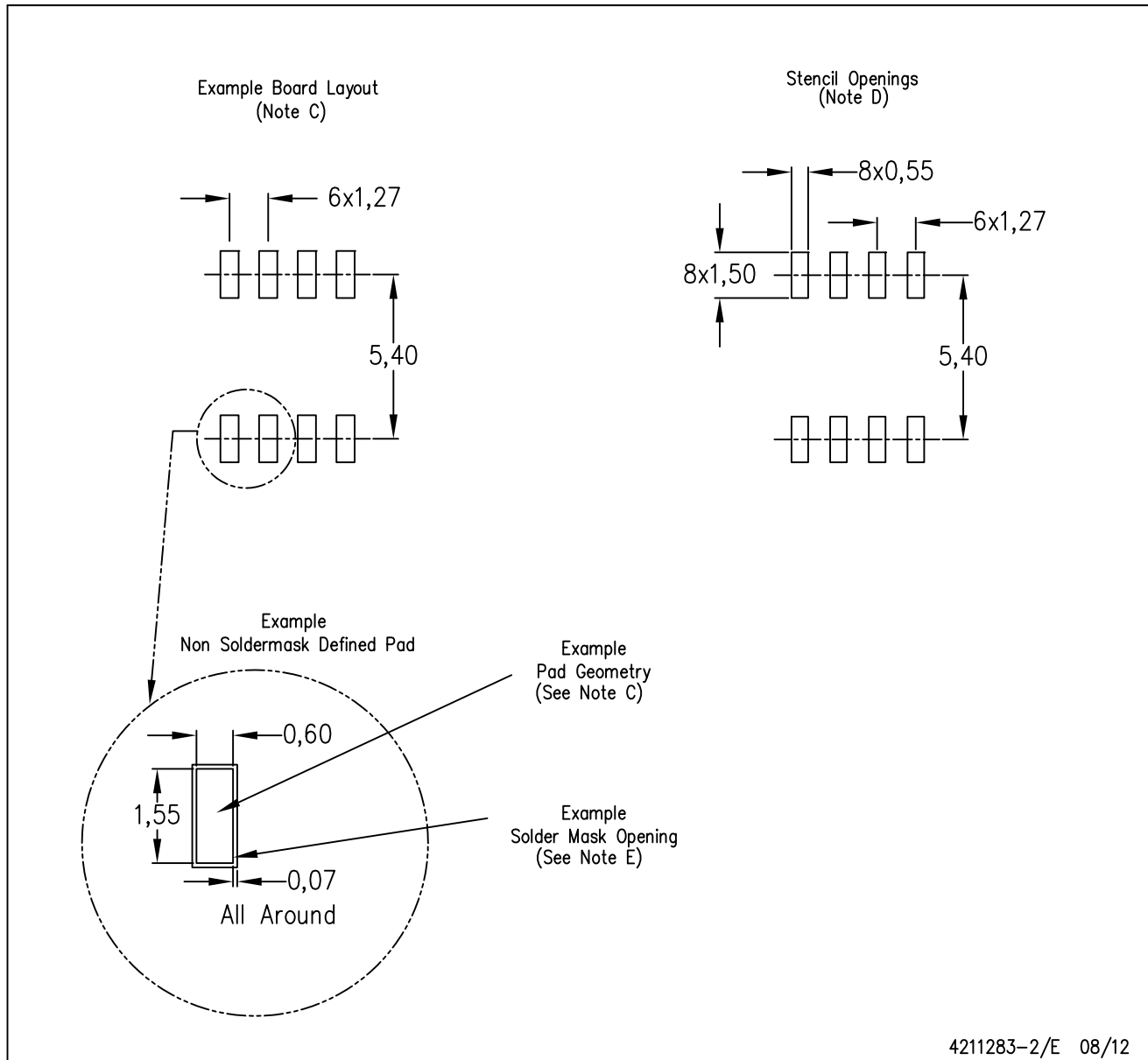
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

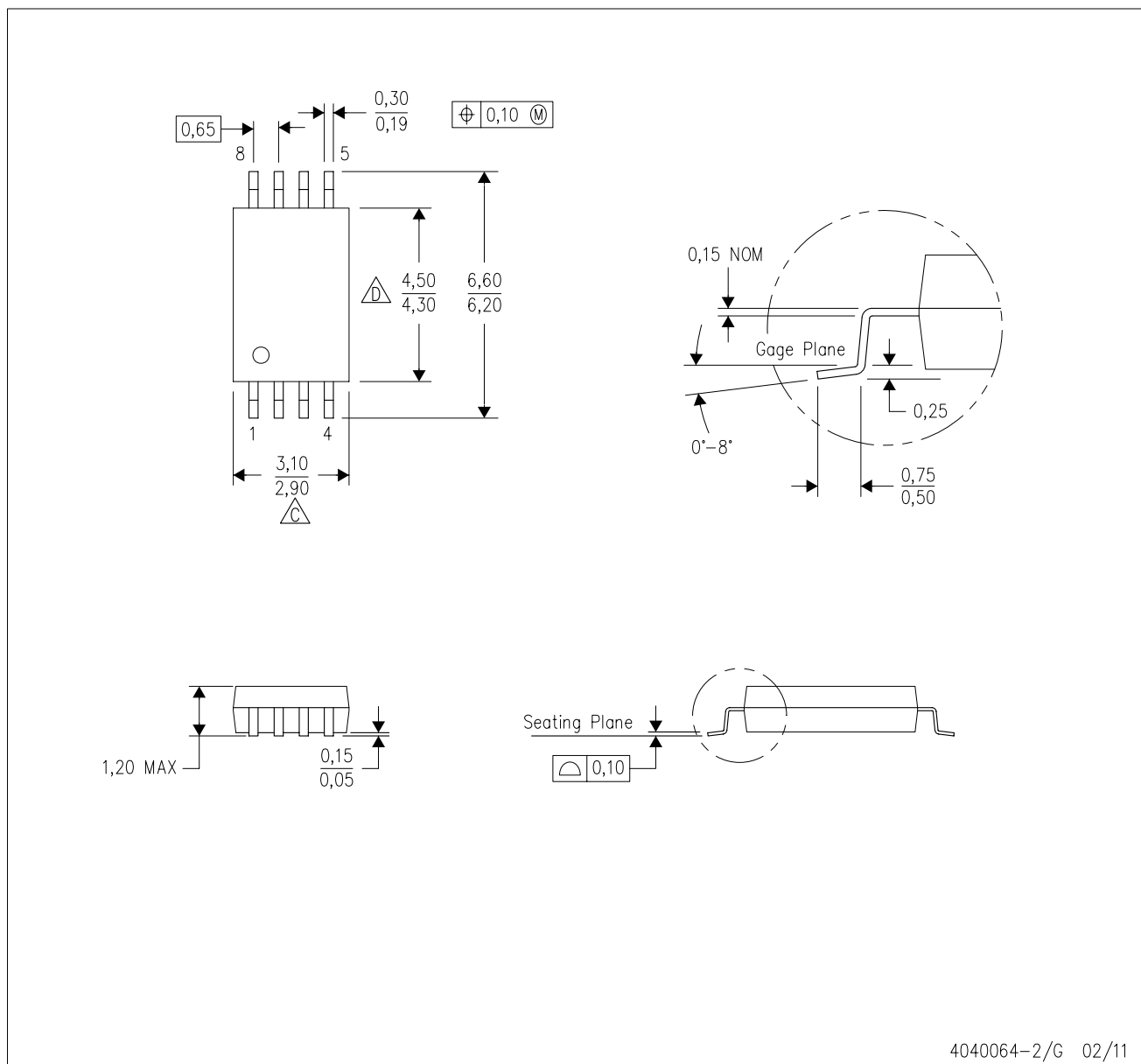
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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