

LMV341/LMV342/LMV344 Single with Shutdown/Dual/Quad General Purpose, 2.7V, Rail-to-Rail Output, 125°C, Operational Amplifiers

 Check for Samples: [LMV341-N](#), [LMV342-N](#), [LMV344-N](#)

FEATURES

- (Typical 2.7V supply values; unless otherwise noted)
- Guaranteed 2.7V and 5V specifications
- Input referred voltage noise (@ 10kHz) 29nV/√Hz
- Supply current (per amplifier) 100µA
- Gain bandwidth product 1.0MHz
- Slew rate 1.0V/µs
- Shutdown Current (LMV341) 45pA
- Turn-on time from shutdown (LMV341) 5µs
- Input bias current 20fA

APPLICATIONS

- Cordless/cellular phones
- Laptops
- PDAs
- PCMCIA/Audio
- Portable/battery-powered electronic equipment
- Supply current monitoring
- Battery monitoring
- Buffer
- Filter
- Driver

DESCRIPTION

The LMV341/LMV342/LMV344 are single, dual, and quad low voltage, low power Operational Amplifiers. They are designed specifically for low voltage portable applications. Other important product characteristics are low input bias current, rail-to-rail output, and wide temperature range.

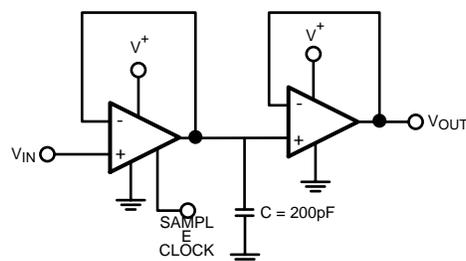
The patented class AB turnaround stage significantly reduces the noise at higher frequencies, power consumption, and offset voltage. The PMOS input stage provides the user with ultra-low input bias current of 20fA (typical) and high input impedance.

The industrial-plus temperature range of -40°C to 125°C allows the LMV341/LMV342/LMV344 to accommodate a broad range of extended environment applications. LMV341 expands National Semiconductor's Silicon Dust™ amplifier portfolio offering enhancements in size, speed, and power savings. The LMV341/LMV342/LMV344 are guaranteed to operate over the voltage range of 2.7V to 5.5V and all have rail-to-rail output.

The LMV341 offers a shutdown pin that can be used to disable the device. Once in shutdown mode, the supply current is reduced to 45pA (typical). The LMV341/LMV342/LMV344 have 29nV Voltage Noise at 10KHz, 1MHz GBW, 1.0V/µs Slew Rate, 0.25mVos, and 0.1µA shutdown current (LMV341.)

The LMV341 is offered in the tiny 6-Pin SC70 package, the LMV342 in space saving 8-Pin MSOP and SOIC, and the LMV344 in 14-Pin TSSOP and SOIC. These small package amplifiers offer an ideal solution for applications requiring minimum PC board footprint. Applications with area constrained PC board requirements include portable electronics such as cellular handsets and PDAs.

Sample and Hold Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

ESD Tolerance ⁽²⁾	
Machine Model	200V
Human Body Model	2000V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V ⁺ -V ⁻)	6.0V
Output Short Circuit to V ⁺	⁽³⁾
Output Short Circuit to V ⁻	⁽⁴⁾
Storage Temperature Range	-65°C to 150°C
Junction Temperature ⁽⁵⁾	150°C
Mounting Temperature	
Infrared or Convection Reflow (20 sec.)	235°C
Wave Soldering Lead Temp. (10 sec.)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (3) Shorting output to V⁺ will adversely affect reliability.
- (4) Shorting output to V⁻ will adversely affect reliability.
- (5) The maximum power dissipation is a function of T_{J(MAX)}, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / θ_{JA}. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings ⁽¹⁾

Supply Voltage	2.7V to 5.5V
Temperature Range	-40°C to 125°C
Thermal Resistance (θ _{JA})	
6-Pin SC70	414°C/W
8-Pin SOIC	190°C/W
8-Pin MSOP	235°C/W
14-Pin TSSOP	155°C/W
14-Pin SOIC	145°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

2.7V DC Electrical Characteristics ⁽¹⁾

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{M}\Omega$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Units
V_{OS}	Input Offset Voltage	LMV341		0.25	4 4.5	mV
		LMV342/LMV344		0.55	5 5.5	
TCV_{OS}	Input Offset Voltage Average Drift			1.7		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current			0.02	120 250	pA
I_{OS}	Input Offset Current			6.6		fA
I_S	Supply Current	Per Amplifier		100	170 230	μA
		Shutdown Mode, $V_{\text{SD}} = 0\text{V}$ (LMV341)		45pA	1 μA 1.5μA	
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 1.7\text{V}$ $0\text{V} \leq V_{\text{CM}} \leq 1.6\text{V}$	56 50	80		dB
PSRR	Power Supply Rejection Ratio	$2.7\text{V} \leq V^+ \leq 5\text{V}$	65 60	82		dB
V_{CM}	Input Common Mode Voltage	For CMRR $\geq 50\text{dB}$	0	-0.2 to 1.9 (Range)	1.7	V
A_V	Large Signal Voltage Gain	$R_L = 10\text{k}\Omega$ to 1.35V	78 70	113		dB
		$R_L = 2\text{k}\Omega$ to 1.35V	72 64	103		
V_O	Output Swing	$R_L = 2\text{k}\Omega$ to 1.35V		24	60 95	mV
				60 95	26	
		$R_L = 10\text{k}\Omega$ to 1.35V		5.0	30 40	
				30 40	5.3	
I_O	Output Short Circuit Current	Sourcing LMV341/LMV342	20	32		mA
		Sourcing LMV344	18	24		
		Sinking	15	24		
t_{on}	Turn-on Time from Shutdown	(LMV341)		5		μs
V_{SD}	Shutdown Pin Voltage Range	ON Mode (LMV341)		1.7 to 2.7	2.4 to 2.7	V
		Shutdown Mode (LMV341)		0 to 1	0 to 0.8	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.

(2) All limits are guaranteed by testing or statistical analysis.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

2.7V AC Electrical Characteristics ⁽¹⁾

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{M}\Omega$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Units
SR	Slew Rate	$R_L = 10\text{k}\Omega$, ⁽⁴⁾		1.0		V/ μs
GBW	Gain Bandwidth Product	$R_L = 100\text{k}\Omega$, $C_L = 200\text{pF}$		1.0		MHz
Φ_m	Phase Margin	$R_L = 100\text{k}\Omega$		72		deg
G_m	Gain Margin	$R_L = 100\text{k}\Omega$		20		dB
e_n	Input-Referred Voltage Noise	$f = 1\text{kHz}$		40		nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$f = 1\text{kHz}$		0.001		pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$, $A_V = +1$ $R_L = 600\Omega$, $V_{\text{IN}} = 1\text{V}_{\text{PP}}$		0.017		%

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.
- (2) All limits are guaranteed by testing or statistical analysis.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (4) Connected as voltage follower with 2V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

5V DC Electrical Characteristics ⁽¹⁾

 Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{M}\Omega$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Units
V_{OS}	Input Offset Voltage	LMV341		0.025	4 4.5	mV
		LMV342/LMV344		0.70	5 5.5	
TCV_{OS}	Input Offset Voltage Average Drift			1.9		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current			0.02	200 375	pA
I_{OS}	Input Offset Current			6.6		fA
I_S	Supply Current	Per Amplifier		107	200 260	μA
		Shutdown Mode, $V_{\text{SD}} = 0\text{V}$ (LMV341)		0.033	1 1.5	μA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 4.0\text{V}$ $0\text{V} \leq V_{\text{CM}} \leq 3.9\text{V}$	56 50	86		dB
PSRR	Power Supply Rejection Ratio	$2.7\text{V} \leq V^+ \leq 5\text{V}$	65 60	82		dB
V_{CM}	Input Common Mode Voltage	For CMRR $\geq 50\text{dB}$	0	-0.2 to 4.2 (Range)	4	V
A_V	Large Signal Voltage Gain ⁽⁴⁾	$R_L = 10\text{k}\Omega$ to 2.5V	78 70	116		dB
		$R_L = 2\text{k}\Omega$ to 2.5V	72 64	107		
V_O	Output Swing	$R_L = 2\text{k}\Omega$ to 2.5V		32	60 95	mV
				60 95	34	
		$R_L = 10\text{k}\Omega$ to 2.5V		7	30 40	mV
				30 40	7	
I_O	Output Short Circuit Current	Sourcing	85	113		mA
		Sinking	50	75		
t_{on}	Turn-on Time from Shutdown	(LMV341)		5		μs
V_{SD}	Shutdown Pin Voltage Range	ON Mode (LMV341)		3.1 to 5	4.5 to 5.0	V
		Shutdown Mode (LMV341)		0 to 1	0 to 0.8	

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.
- (2) All limits are guaranteed by testing or statistical analysis.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (4) R_L is connected to mid-supply. The output voltage is $\text{GND} + 0.2\text{V} \leq V_O \leq V^+ - 0.2\text{V}$

5V AC Electrical Characteristics ⁽¹⁾

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\text{M}\Omega$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Units
SR	Slew Rate	$R_L = 10\text{k}\Omega$, ⁽⁴⁾		1.0		V/ μs
GBW	Gain-Bandwidth Product	$R_L = 10\text{k}\Omega$, $C_L = 200\text{pF}$		1.0		MHz
Φ_m	Phase Margin	$R_L = 100\text{k}\Omega$		70		deg
G_m	Gain Margin	$R_L = 100\text{k}\Omega$		20		dB
e_n	Input-Referred Voltage Noise	$f = 1\text{kHz}$		39		nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$f = 1\text{kHz}$		0.001		pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$, $A_V = +1$ $R_L = 600\Omega$, $V_{\text{IN}} = 1\text{V}_{\text{PP}}$		0.012		%

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.
- (2) All limits are guaranteed by testing or statistical analysis.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (4) Connected as voltage follower with 2V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

Connection Diagram

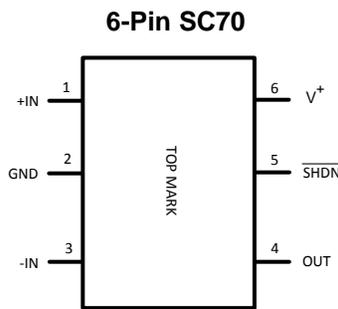


Figure 1. Top View

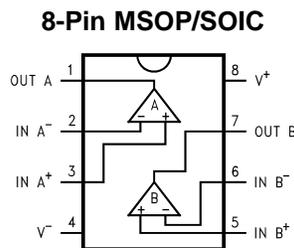


Figure 2. Top View

14-Pin TSSOP/SOIC

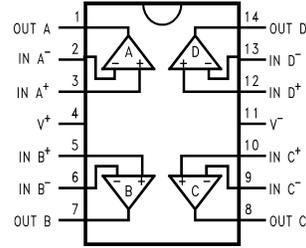
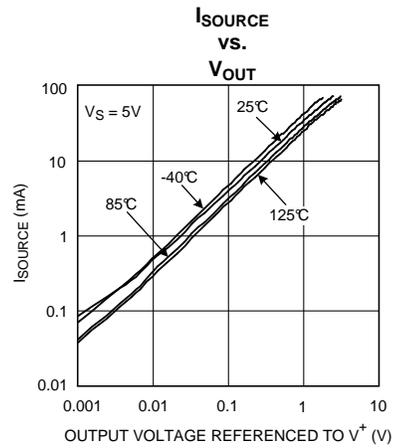
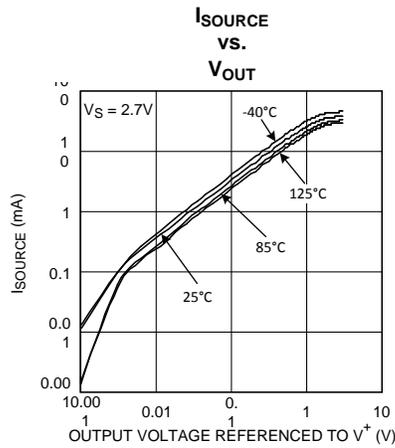
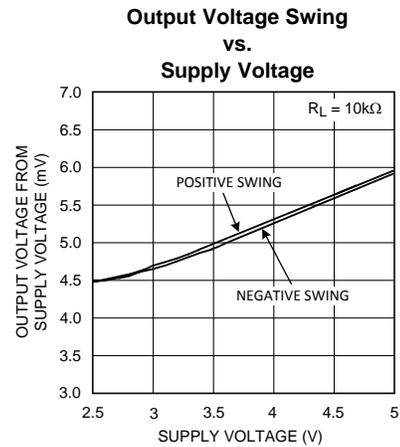
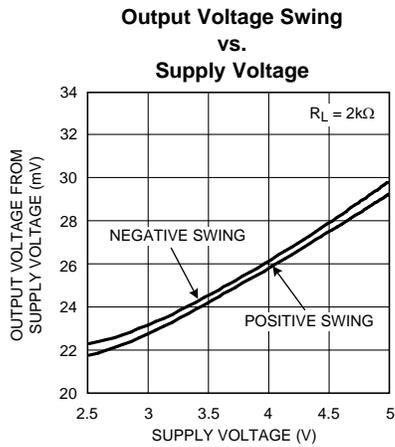
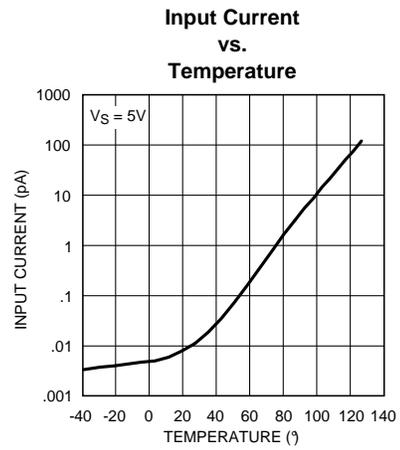
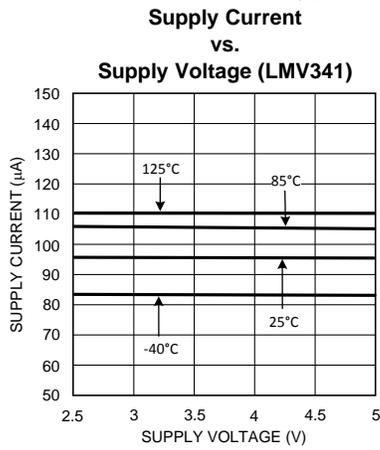
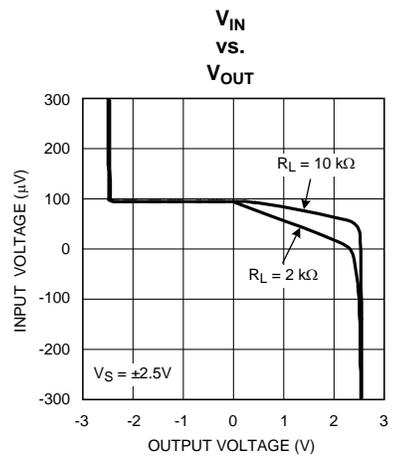
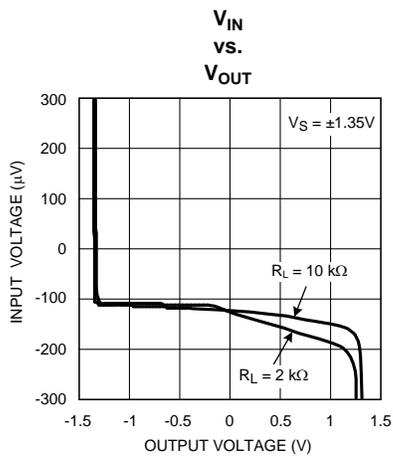
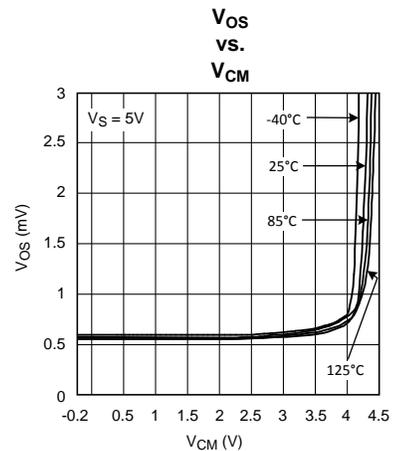
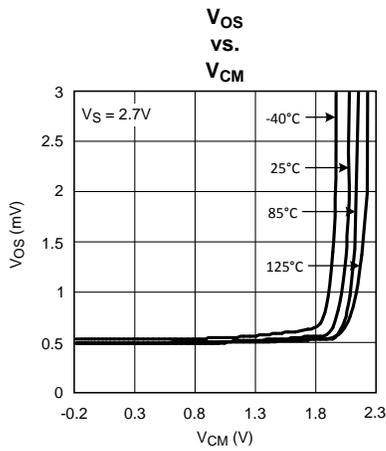
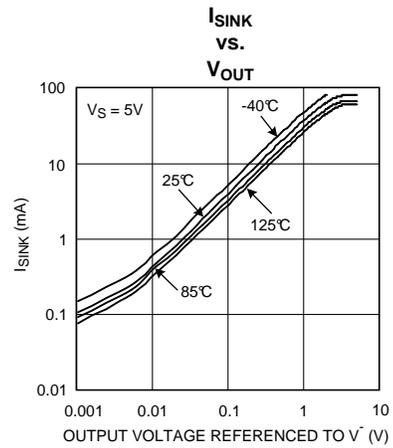
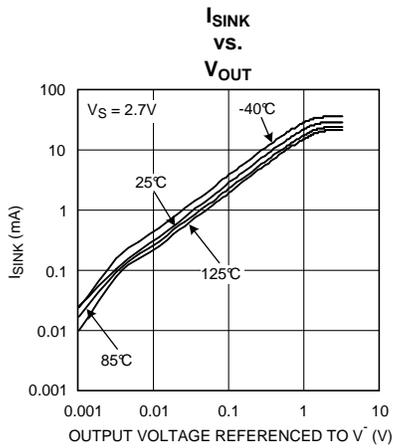


Figure 3. Top View

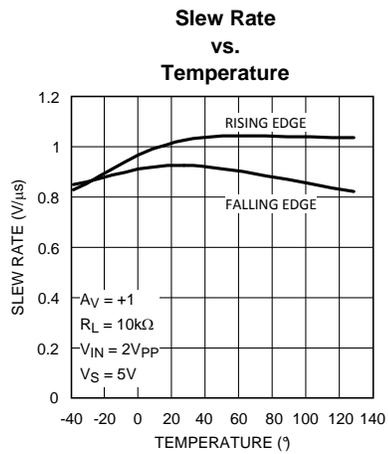
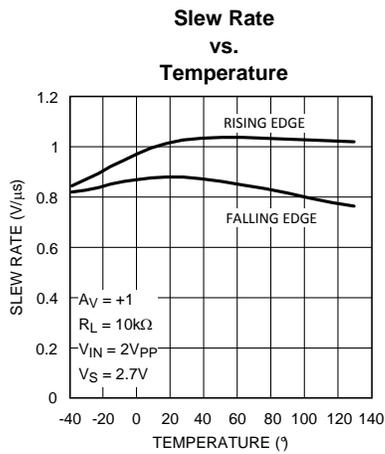
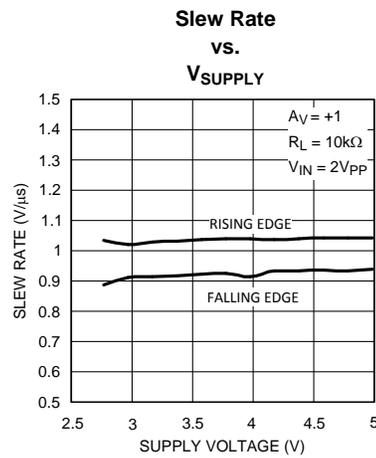
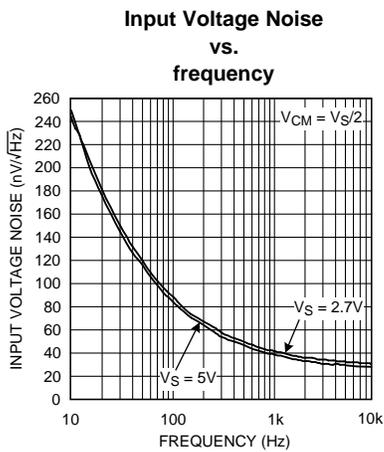
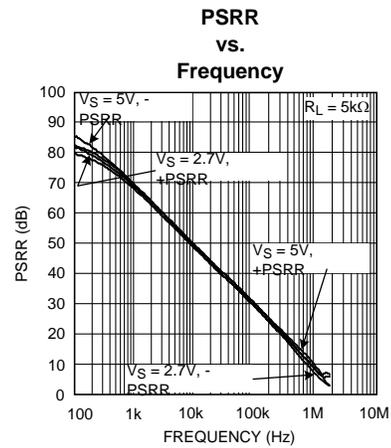
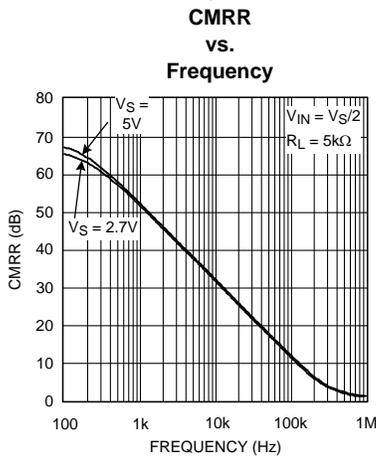
Typical Performance Characteristics



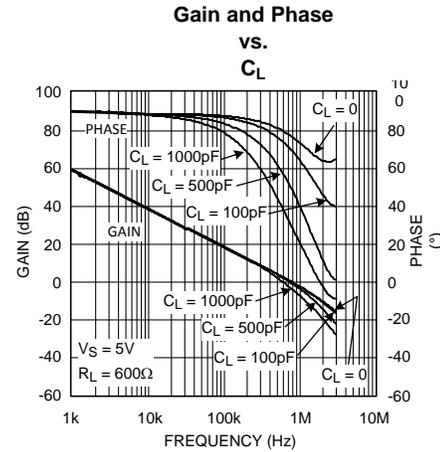
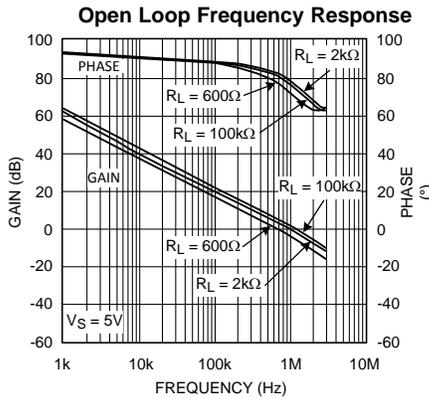
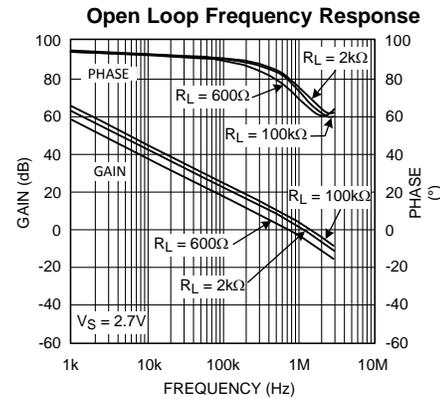
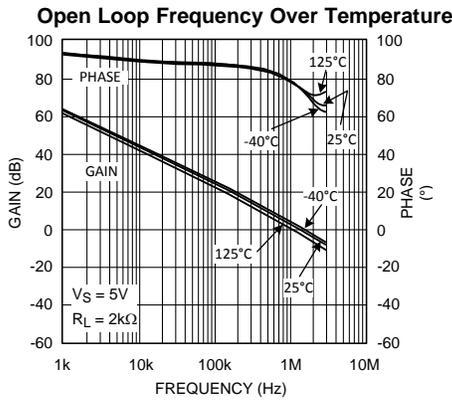
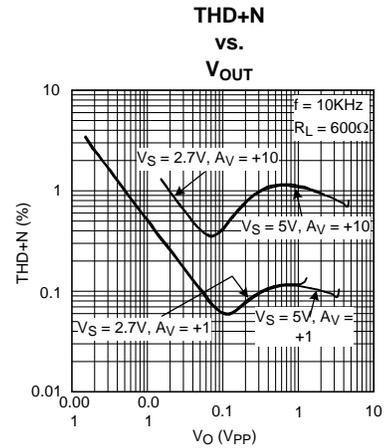
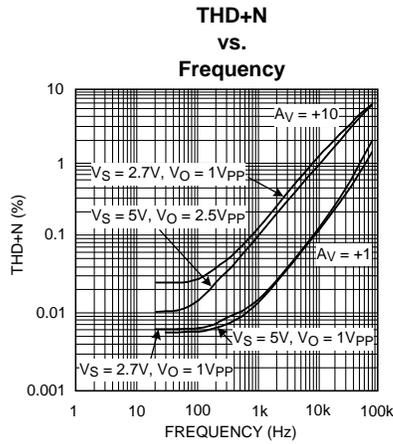
Typical Performance Characteristics (continued)



Typical Performance Characteristics (continued)

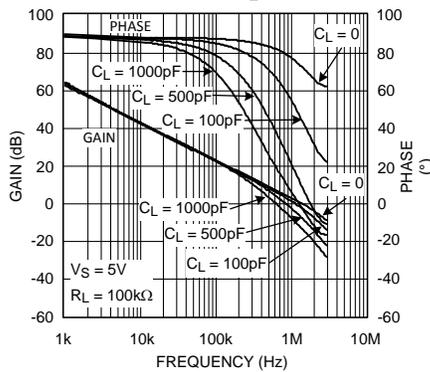


Typical Performance Characteristics (continued)

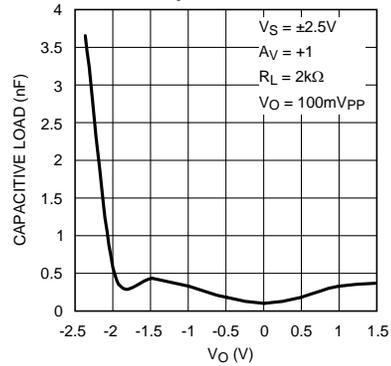


Typical Performance Characteristics (continued)

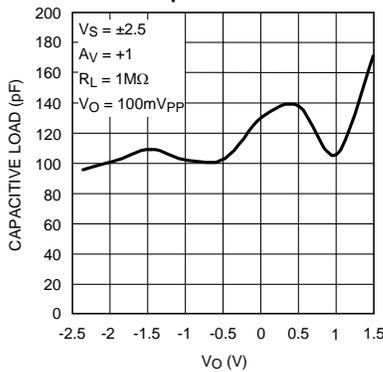
Gain and Phase vs. C_L



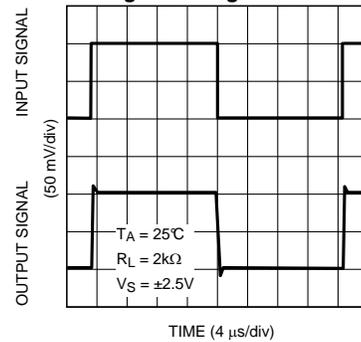
Stability vs. Capacitive Load



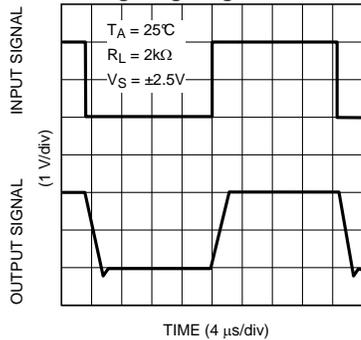
Stability vs. Capacitive Load



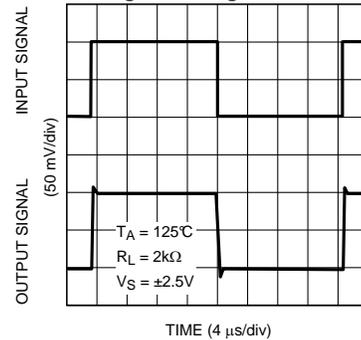
Non-Inverting Small Signal Pulse Response



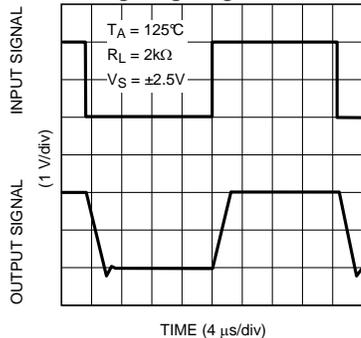
Non-Inverting Large Signal Pulse Response



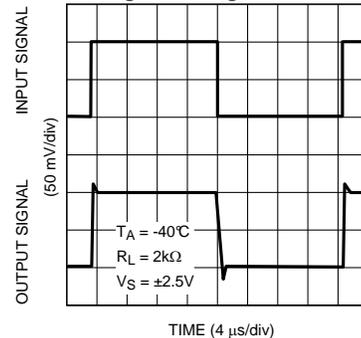
Non-Inverting Small Signal Pulse Response



Non-Inverting Large Signal Pulse Response

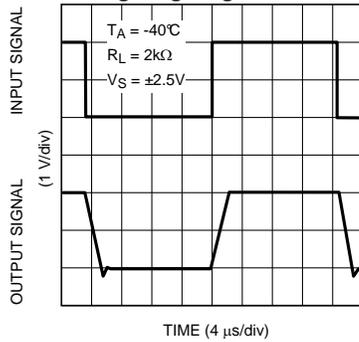


Non-Inverting Small Signal Pulse Response

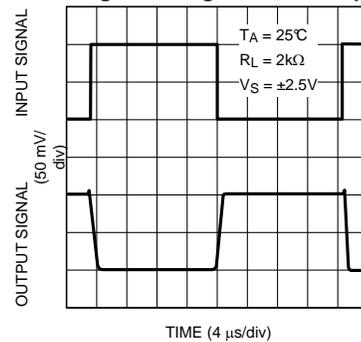


Typical Performance Characteristics (continued)

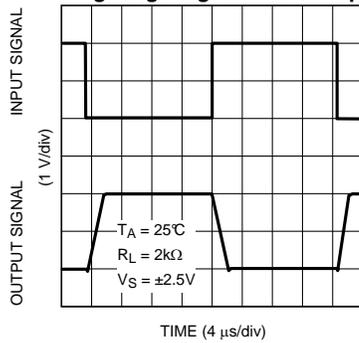
Non-Inverting Large Signal Pulse Response



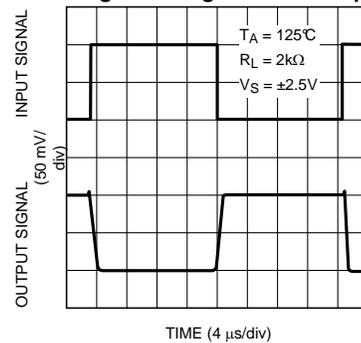
Inverting Small Signal Pulse Response



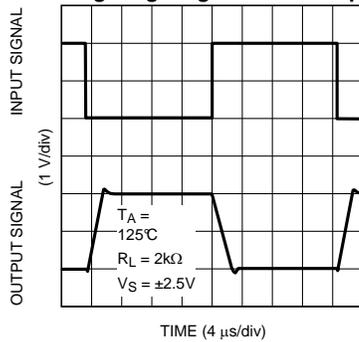
Inverting Large Signal Pulse Response



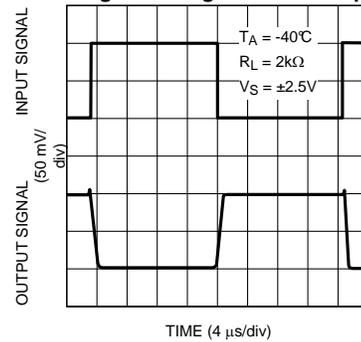
Inverting Small Signal Pulse Response



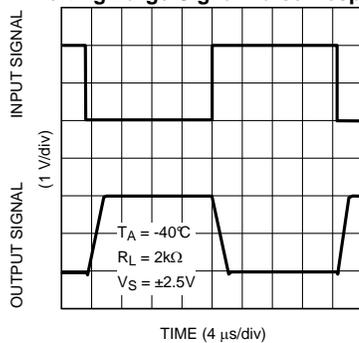
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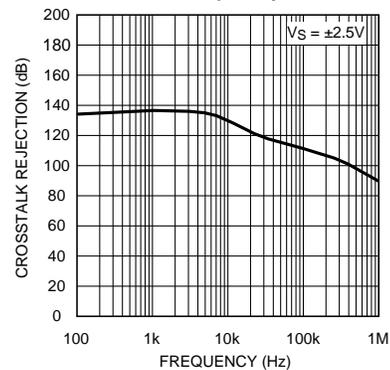
Inverting Small Signal Pulse Response



Inverting Large Signal Pulse Response



Crosstalk Rejection vs. Frequency



Application Section

LMV341/LMV342/LMV344

The LMV341/LMV342/LMV344 family of amplifiers features low voltage, low power, and rail-to-rail output operational amplifiers designed for low voltage portable applications. The family is designed using all CMOS technology. This results in an ultra low input bias current. The LMV341 has a shutdown option, which can be used in portable devices to increase battery life.

A simplified schematic of the LMV341/LMV342/LMV344 family of amplifiers is shown in [Figure 4](#). The PMOS input differential pair allows the input to include ground. The output of this differential pair is connected to the Class AB turnaround stage. This Class AB turnaround has a lower quiescent current, compared to regular turnaround stages. This results in lower offset, noise, and power dissipation, while slew rate equals that of a conventional turnaround stage. The output of the Class AB turnaround stage provides gate voltage to the complementary common-source transistors at the output stage. These transistors enable the device to have rail-to-rail output.

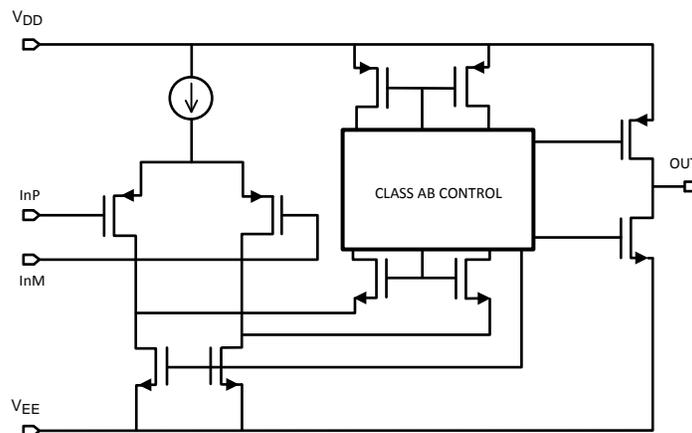


Figure 4. Simplified Schematic

CLASS AB TURNAROUND STAGE AMPLIFIER

This patented folded cascode stage has a combined class AB amplifier stage, which replaces the conventional folded cascode stage. Therefore, the class AB folded cascode stage runs at a much lower quiescent current compared to conventional folded cascode stages. This results in significantly smaller offset and noise contributions. The reduced offset and noise contributions in turn reduce the offset voltage level and the voltage noise level at the input of the LMV341/LMV342/LMV344. Also the lower quiescent current results in a high open-loop gain for the amplifier. The lower quiescent current does not affect the slew rate of the amplifier nor its ability to handle the total current swing coming from the input stage.

The input voltage noise of the device at low frequencies, below 1kHz, is slightly higher than devices with a BJT input stage; However the PMOS input stage results in a much lower input bias current and the input voltage noise drops at frequencies above 1kHz.

SAMPLE AND HOLD CIRCUIT

The lower input bias current of the LMV341 results in a very high input impedance. The output impedance when the device is in shutdown mode is quite high. These high impedances, along with the ability of the shutdown pin to be derived from a separate power source, make LMV341 a good choice for sample and hold circuits. The sample clock should be connected to the shutdown pin of the amplifier to rapidly turn the device on or off.

Figure 5 shows the schematic of a simple sample and hold circuit. When the sample clock is high the first amplifier is in normal operation mode and the second amplifier acts as a buffer. The capacitor, which appears as a load on the first amplifier, will be charging at this time. The voltage across the capacitor is that of the non-inverting input of the first amplifier since it is connected as a voltage-follower. When the sample clock is low the first amplifier is shut off, bringing the output impedance to a high value. The high impedance of this output, along with the very high impedance on the input of the second amplifier, prevents the capacitor from discharging. There is very little voltage droop while the first amplifier is in shutdown mode. The second amplifier, which is still in normal operation mode and is connected as a voltage follower, also provides the voltage sampled on the capacitor at its output.

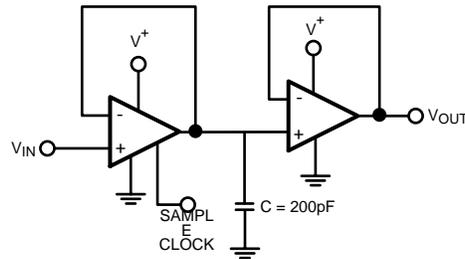


Figure 5. Sample and Hold Circuit

SHUTDOWN FEATURE

The LMV341 is capable of being turned off in order to conserve power and increase battery life in portable devices. Once in shutdown mode the supply current is drastically reduced, 1 μ A maximum, and the output will be "tri-stated."

The device will be disabled when the shutdown pin voltage is pulled low. The shutdown pin should never be left unconnected. Leaving the pin floating will result in an undefined operation mode and the device may oscillate between shutdown and active modes.

The LMV341 typically turns on 2.8 μ s after the shutdown voltage is pulled high. The device turns off in less than 400ns after shutdown voltage is pulled low. Figure 6 and Figure 7 show the turn-on and turn-off time of the LMV341, respectively. In order to reduce the effect of the capacitance added to the circuit by the scope probe, in the turn-off time circuit a resistive load of 600 Ω is added. Figure 8 and Figure 9 show the test circuits used to obtain the two plots.

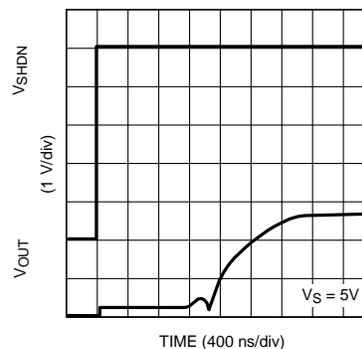


Figure 6. Turn-on Time

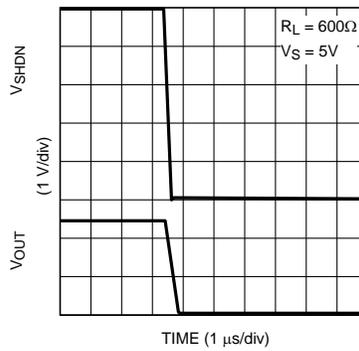


Figure 7. Turn-off Time

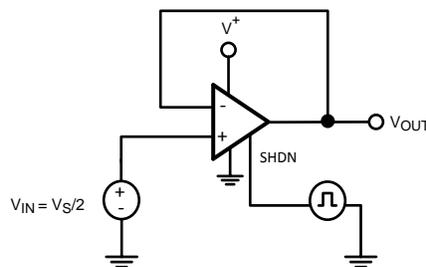


Figure 8. Turn-on Time

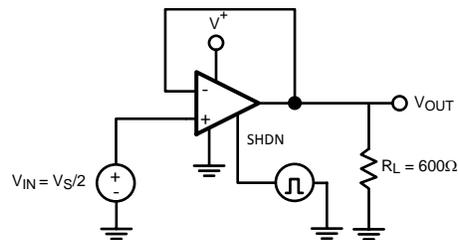


Figure 9. Turn-off Time

LOW INPUT BIAS CURRENT

The LMV341/LMV342/LMV344 Amplifiers have a PMOS input stage. As a result, they will have a much lower input bias current than devices with BJT input stages. This feature makes these devices ideal for sensor circuits. A typical curve of the input bias current of the LMV341 is shown in [Figure 10](#).

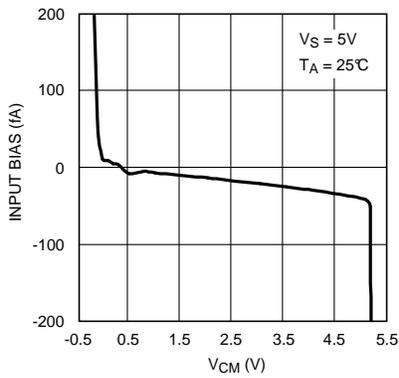


Figure 10. Input Bias Current vs. V_{CM}

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV341MG	ACTIVE	SC70	DCK	6	1000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV341MG/NOPB	ACTIVE	SC70	DCK	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV341MGX	ACTIVE	SC70	DCK	6	3000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV341MGX/NOPB	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV342MA	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	
LMV342MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV342MAX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LMV342MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV342MM	ACTIVE	VSSOP	DGK	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV342MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV342MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV342MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV344MA	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	
LMV344MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV344MAX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LMV344MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV344MT	ACTIVE	TSSOP	PW	14	94	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV344MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV344MTX	ACTIVE	TSSOP	PW	14	2500	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV344MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

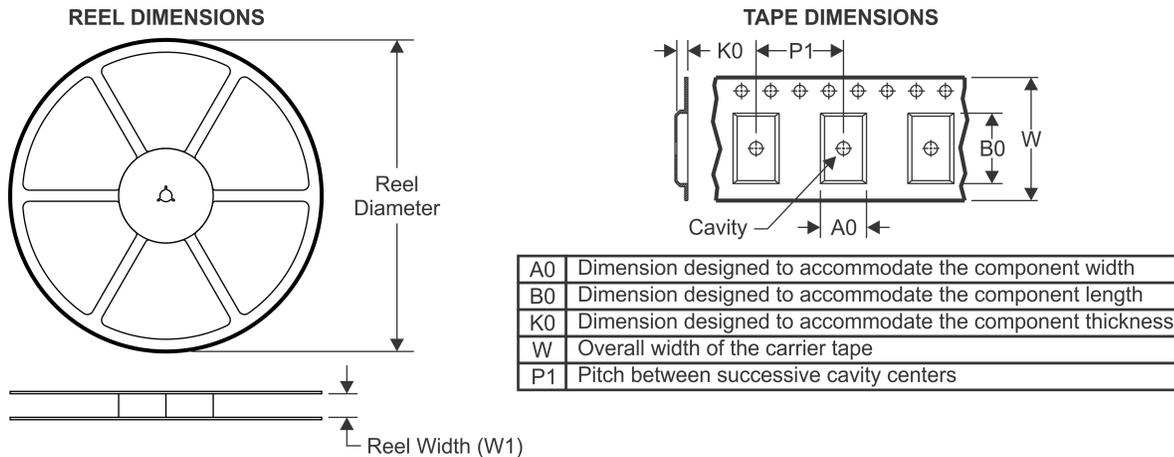
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

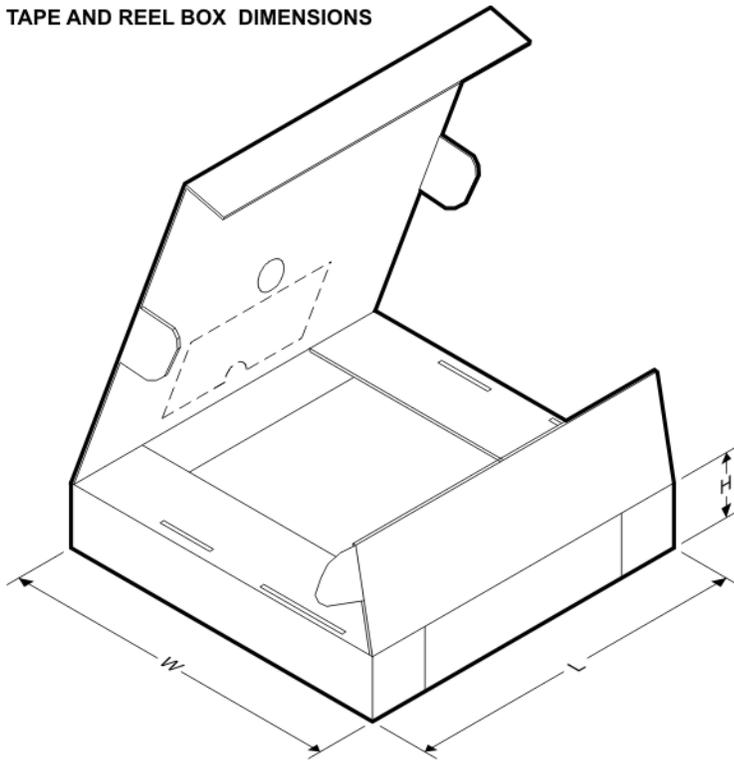
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV341MG	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV341MG/NOPB	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV341MGX	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV341MGX/NOPB	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV342MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV342MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV342MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV342MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV342MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV342MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV344MAX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV344MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV344MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMV344MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

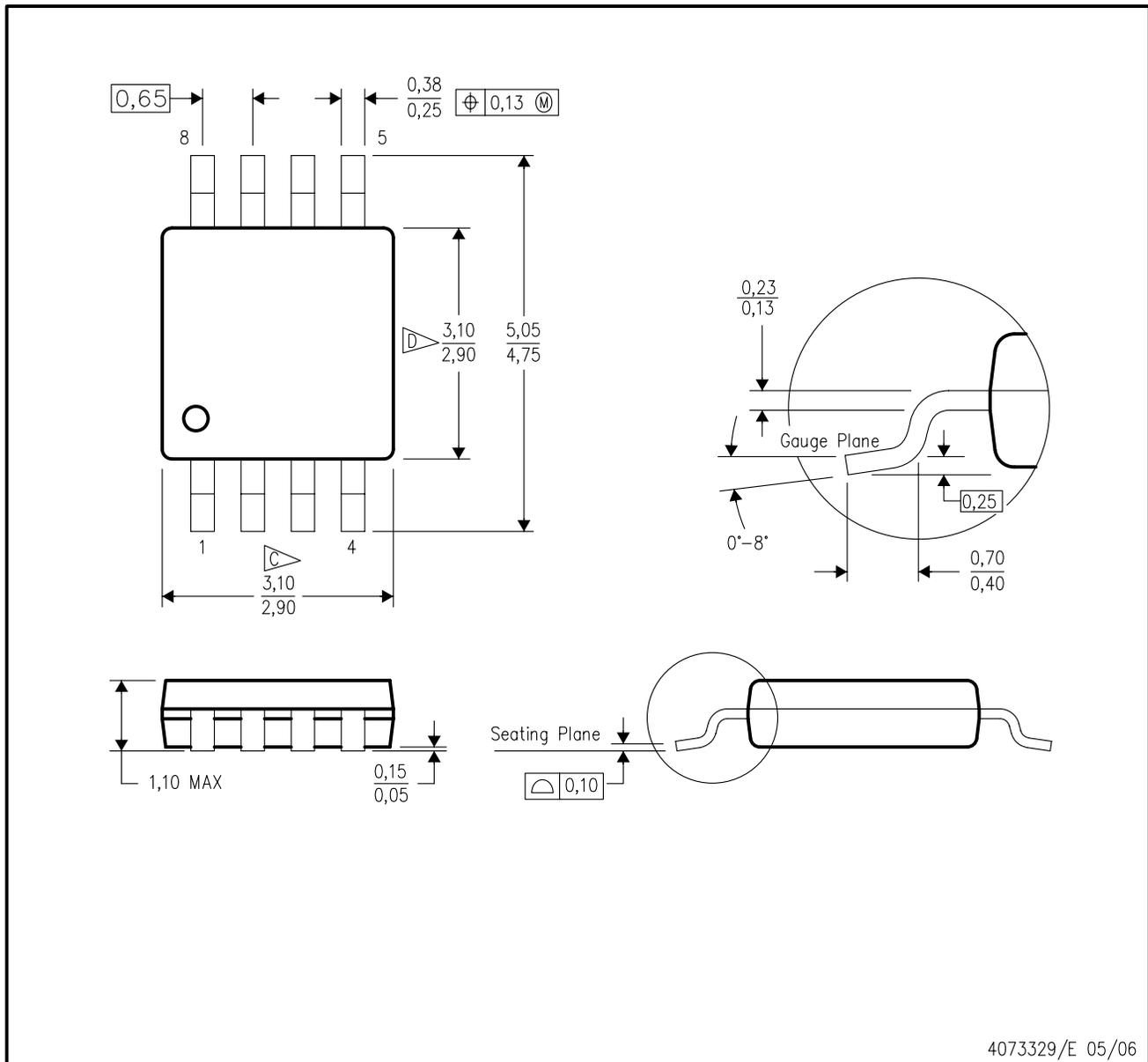
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV341MG	SC70	DCK	6	1000	203.0	190.0	41.0
LMV341MG/NOPB	SC70	DCK	6	1000	203.0	190.0	41.0
LMV341MGX	SC70	DCK	6	3000	206.0	191.0	90.0
LMV341MGX/NOPB	SC70	DCK	6	3000	206.0	191.0	90.0
LMV342MAX	SOIC	D	8	2500	349.0	337.0	45.0
LMV342MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMV342MM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV342MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV342MMX	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV342MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV344MAX	SOIC	D	14	2500	349.0	337.0	45.0
LMV344MAX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0
LMV344MTX	TSSOP	PW	14	2500	349.0	337.0	45.0
LMV344MTX/NOPB	TSSOP	PW	14	2500	349.0	337.0	45.0

DGK (S-PDSO-G8)

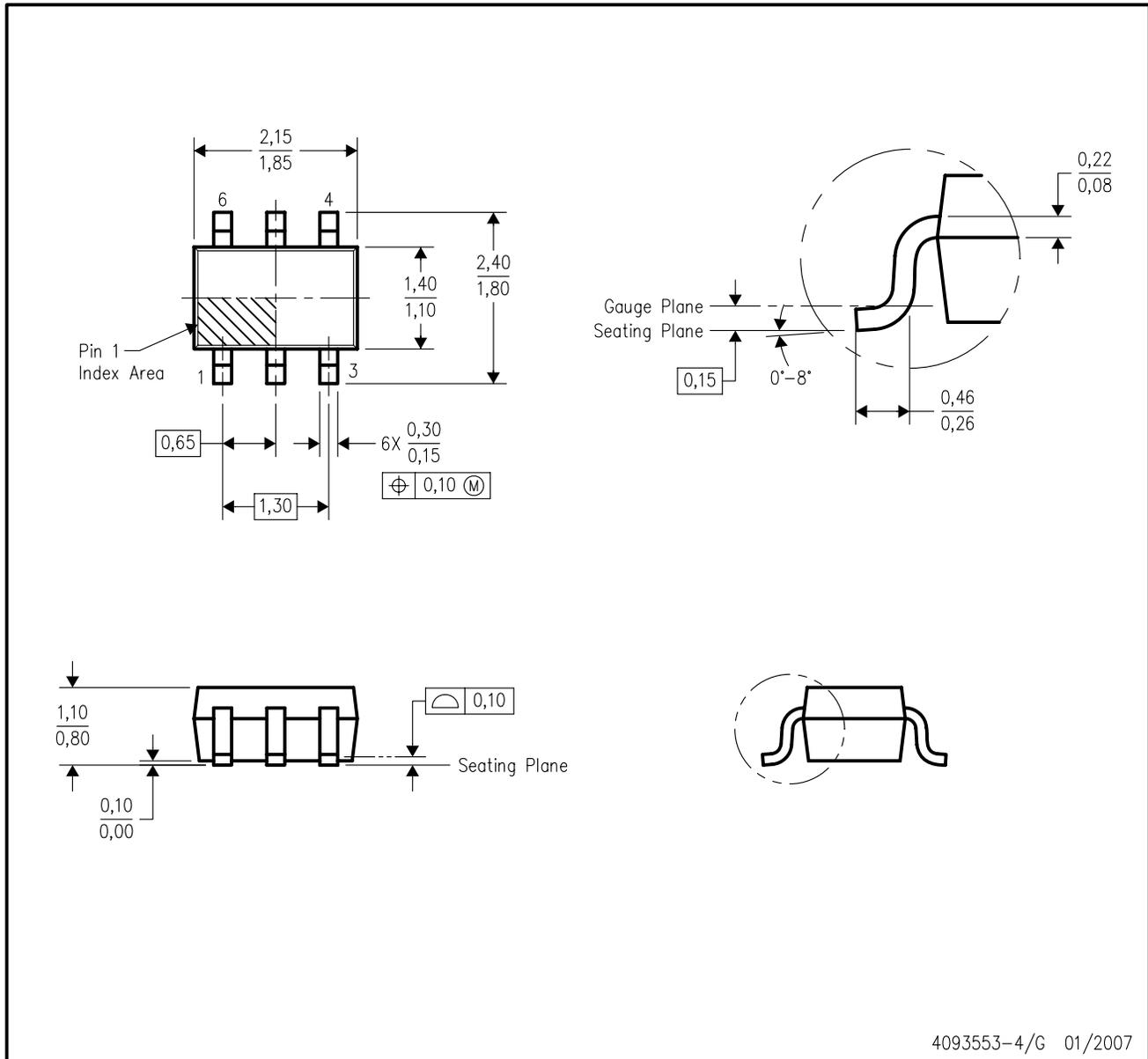
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 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DCK (R-PDSO-G6)

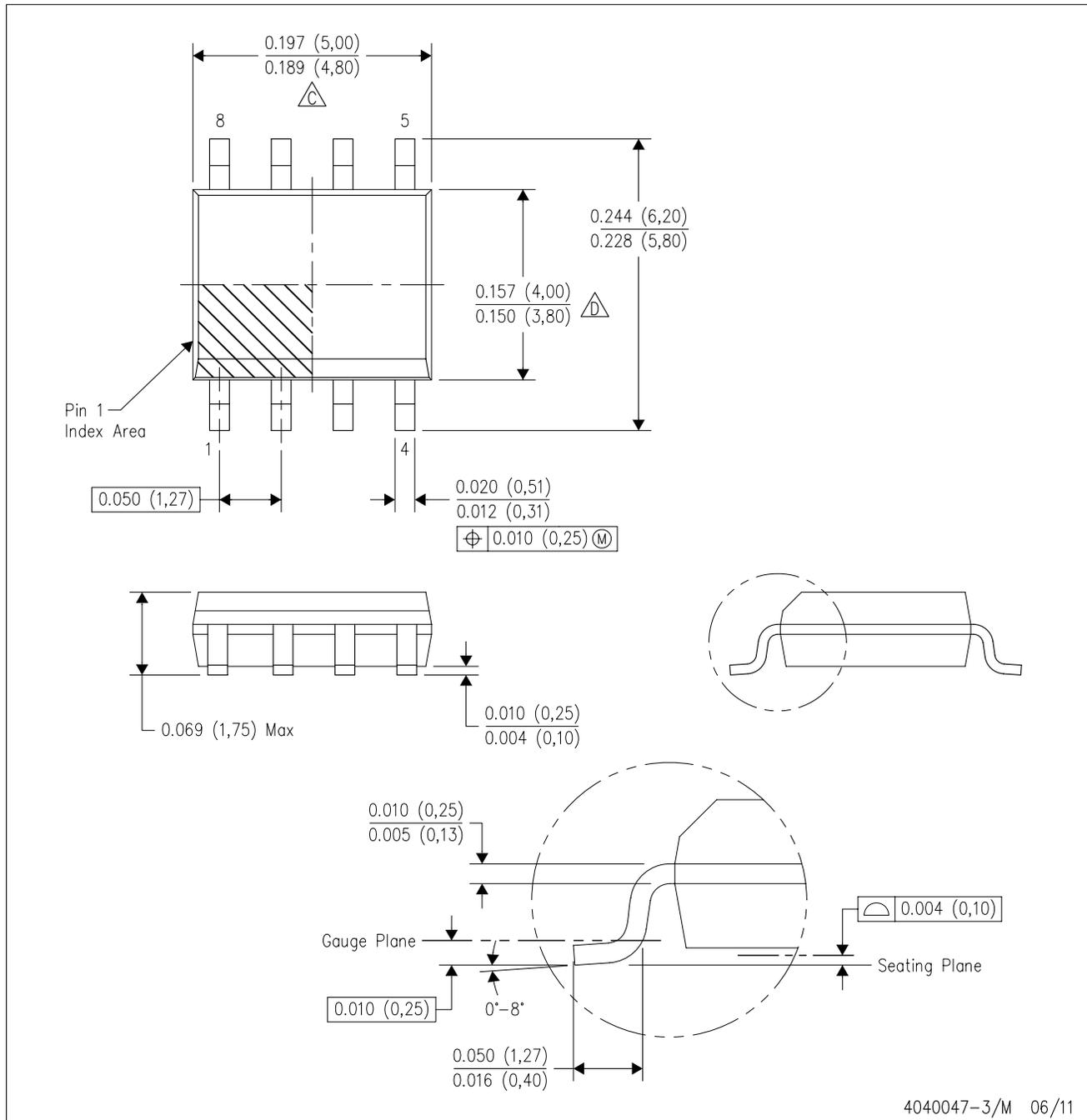
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 - D. Falls within JEDEC MO-203 variation AB.

D (R-PDSO-G8)

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 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

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