LMV651/LMV652/LMV654 12 MHz, Low Voltage, Low Power Amplifiers

Check for Samples: LMV651, LMV652, LMV654

FEATURES

- **(Typical 5V supply, unless otherwise noted.)**
- **Specified 3.0V and 5.0V performance**
- **Low power supply current**
  - **LMV651 116 µA**
  - **LMV652 118 µA per amplifier**
  - **LMV654 122 µA per amplifier**
- **High unity gain bandwidth 12 MHz**
- **Max input offset voltage 1.5 mV**
- **CMRR 100 dB**
- **PSRR 95 dB**
- **Input referred voltage noise 17 nV/√Hz**
- **Output swing with 2 kΩ load 120 mV from rail**
- **Total harmonic distortion 0.003% at 1 kHz, 2 kΩ**
- **Temperature range −40°C to 125°C**

APPLICATIONS

- **Portable equipment**
- **Automotive**
- **Battery powered systems**
- **Sensors and Instrumentation**

DESCRIPTION

National's LMV651/LMV652/LMV654 are high performance, low power operational amplifier ICs implemented with National's advanced VIP50 process. This family of parts features 12 MHz of bandwidth while consuming only 116 µA of current, which is an exceptional bandwidth to power ratio in this op amp class. The LMV651/LMV652/LMV654 are unity gain stable and provide an excellent solution for general purpose amplification in low voltage, low power applications.

This family of low voltage, low power amplifiers provides superior performance and economy in terms of power and space usage. These op amps have a maximum input offset voltage of 1.5 mV, a rail-to-rail output stage and an input common-mode voltage range that includes ground. The LMV651/LMV652/LMV654 provide a PSRR of 95 dB, a CMRR of 100 dB and a total harmonic distortion (THD) of 0.003% at 1 kHz frequency and 2 kΩ load.

The operating supply voltage range for this family of parts is from 2.7V and 5.5V. These op amps can operate over a wide temperature range (−40°C to 125°C) making them ideal for automotive applications, sensor applications and portable equipment applications. The LMV651 is offered in the ultra tiny 5-Pin SC70 and 5-Pin SOT-23 package. The LMV652 is offered in an 8-Pin MSOP package. The LMV654 is offered in a 14-Pin TSSOP package.

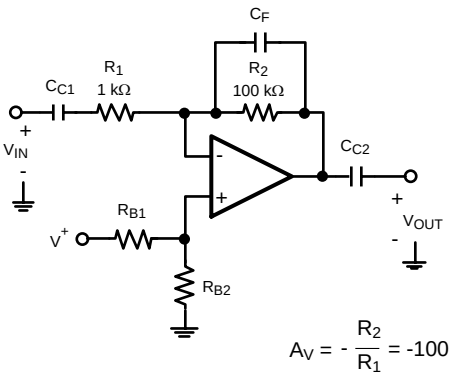


Figure 1. High Gain Wide Bandwidth Inverting Amplifier

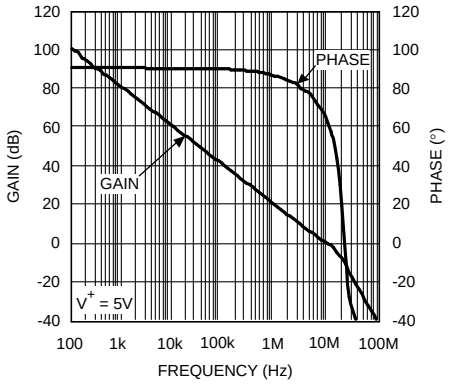


Figure 2. Open Loop Gain and Phase vs. Frequency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Human Body Model	2000V
Machine Model	100V
Differential Input V_{ID}	±0.3V
Supply Voltage ($V_S = V^+ - V^-$)	6V
Input/Output Pin Voltage	V^+ +0.3V, V^- −0.3V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (3)	150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

(3) The maximum power dissipation is a function of $T_{J(MAX}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Temperature Range (2)	−40°C to 125°C
Supply Voltage	2.7V to 5.5V
Package Thermal Resistance (θ_{JA})(2)	
5-Pin SC70	456°C/W
5-Pin SOT-23	234°C/W
8-Pin MSOP	234°C/W
14-Pin TSSOP	160°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

(2) The maximum power dissipation is a function of $T_{J(MAX}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3V DC Electrical Characteristics

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 3V, V^- = 0V, V_O = V_{CM} = $V^+/2$, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			0.1	±1.5 **2.7**	mV
TC V_{OS}	Input Offset Average Drift			6.6		µV/°C
I_B	Input Bias Current	(3)		80	120	nA
I_{OS}	Input Offset Current			2.2	15	nA
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM}≤ 2.0 V	87 **80**	100		dB
PSRR	Power Supply Rejection Ratio	3.0 ≤ V^+ ≤ 5V, V_{CM} = 0.5	87 **81**	95		dB
		2.7 ≤ V^+ ≤ 5.5V, V_{CM} = 0.5	87 **81**	95		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 75 dB **CMRR ≥ 60 dB**	0 **0**		2.1 **2.1**	V
A_{VOL}	Large Signal Voltage Gain	0.3 ≤ V_O ≤ 2.7, R_L = 2 kΩ to $V^+/2$ **0.4 ≤ V_O ≤ 2.6, R_L = 2 kΩ to $V^+/2$**	80 **76**	85		dB
		0.3 ≤ V_O ≤ 2.7, R_L = 10 kΩ to $V^+/2$ **0.4 ≤ V_O ≤ 2.6, R_L = 10 kΩ to $V^+/2$**	86 **83**	93		
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$		80	95 **120**	mV from rail
		R_L = 10 kΩ to $V^+/2$		45	50 **60**	
	Output Swing Low	R_L = 2 kΩ to $V^+/2$		95	110 **125**	
		R_L = 10 kΩ to $V^+/2$		60	65 **75**	
I_{SC}	Maximum Continuous Output Current	Sourcing (4)		17		mA
		Sinking (4)		25		
I_S	Supply Current per Amplifier	LMV651		115	140 **175**	µA
		LMV652		118		
		LMV654		122		
SR	Slew Rate	A_V = +1, 10% to 90% (5)		3.0		V/µs
GBW	Gain Bandwidth Product			12		MHz
e_n	Input-Referred Voltage Noise	f = 100 kHz		17		$nV/\sqrt{Hz}$
		f = 1 kHz		17		
i_n	Input-Referred Current Noise	f = 100 kHz		0.1		$pA/\sqrt{Hz}$
		f = 1 kHz		0.15		
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ		0.003		%

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Positive current corresponds to current flowing into the device.
(4) The part is not short circuit protected and is not recommended for operation with low resistive loads. Typical sourcing and sinking output current curves are provided in the Typical Performance Characteristics and should be consulted before designing for heavy loads.
(5) Slew rate is the average of the rising and falling slew rates.

5V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_O = V_{CM} = $V^+/2$, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			0.1	±1.5 **2.7**	mV
TC V_{OS}	Input Offset Average Drift			6.6		µV/°C
I_B	Input Bias Current	(3)		80	120	nA
I_{OS}	Input Offset Current			2.2	15	nA
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM}≤ 4.0 V	90 **83**	100		dB
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 5V, V_{CM} = 0.5V	87 **81**	95		dB
		2.7V ≤ V^+ ≤ 5.5V, V_{CM} = 0.5V	87 **81**	95		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB **CMRR ≥ 68 dB**	0 **0**		4.1 **4.1**	V
A_{VOL}	Large Signal Voltage Gain	0.3 ≤ V_O ≤ 4.7V, R_L = 2 kΩ to $V^+/2$ **0.4 ≤ V_O ≤ 4.6, R_L = 2 kΩ to $V^+/2$**	79 **76**	84		dB
		0.3 ≤ V_O ≤ 4.7V, R_L = 10 kΩ to $V^+/2$ **0.4 ≤ V_O ≤ 4.6, R_L = 10 kΩ to $V^+/2$**	87 **84**	94		
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$		120	140 **185**	mV from rail
		R_L = 10 kΩ to $V^+/2$		75	90 **120**	
	Output Swing Low	R_L = 2 kΩ to $V^+/2$		110	130 **150**	
		R_L = 10 kΩ to $V^+/2$		70	80 **95**	
I_{SC}	Maximum Continuous Output Current	Sourcing (4)		18.5		mA
		Sinking (4)		25		
I_S	Supply Current per Amplifier	LMV651		116	140 **175**	µA
		LMV652		118		
		LMV654		122		
SR	Slew Rate	A_V = +1, V_O = 1 V_{PP} 10% to 90% (5)		3.0		V/µs
GBW	Gain Bandwidth Product			12		MHz
e_n	Input-Referred Voltage Noise	f = 100 kHz		17		nV/√Hz
		f = 1 kHz		17		
i_n	Input-Referred Current Noise	f = 100 kHz		0.1		pA/√Hz
		f = 1 kHz		0.15		
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ		0.003		%

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Positive current corresponds to current flowing into the device.
(4) The part is not short circuit protected and is not recommended for operation with low resistive loads. Typical sourcing and sinking output current curves are provided in the Typical Performance Characteristics and should be consulted before designing for heavy loads.
(5) Slew rate is the average of the rising and falling slew rates.

Connection Diagram

5-Pin SC70/ SOT-23

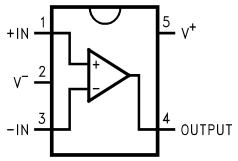


Figure 3. Top View

8-Pin MSOP

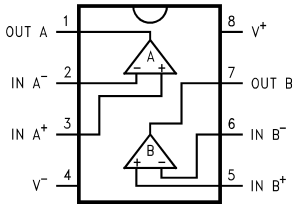


Figure 4. Top View

14-Pin TSSOP

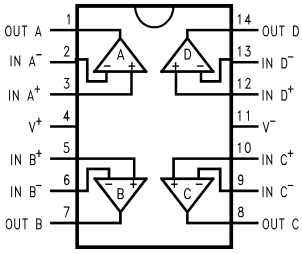
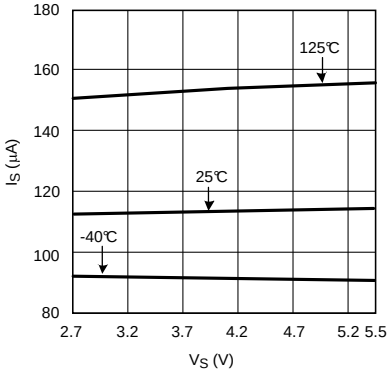


Figure 5. Top View

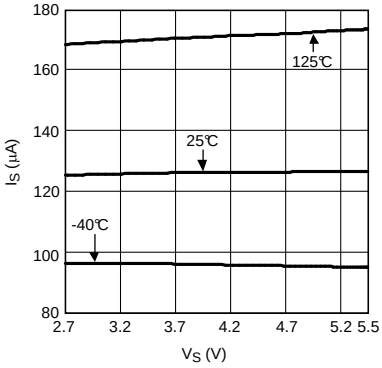
Typical Performance Characteristics

Unless otherwise specified, T_A= 25°C, V_S= 5V, V^+= 5V, V^-= 0V, V_{CM}= V_S/2

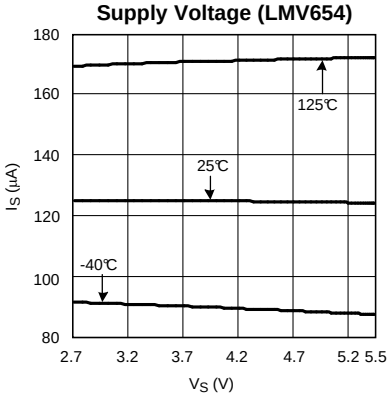
Supply Current vs. Supply Voltage (LMV651)



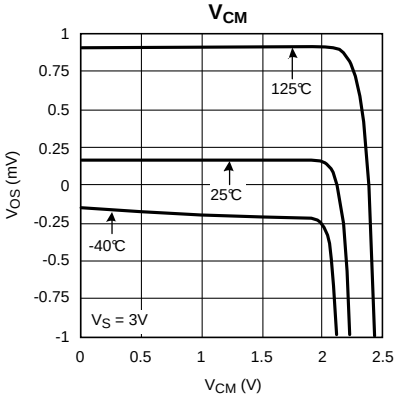
Supply Current per Channel vs. Supply Voltage (LMV652)



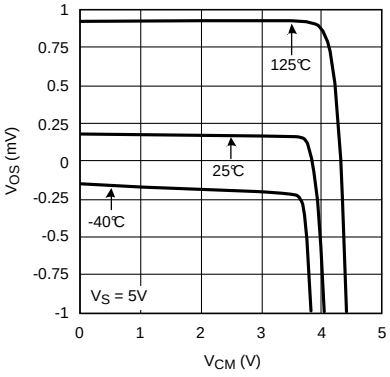
Supply Current per Channel vs. Supply Voltage (LMV654)



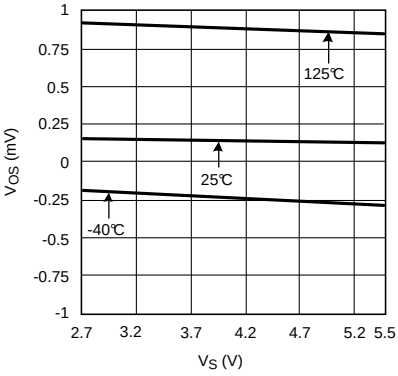
V_{OS} vs. V_{CM}



V_{OS} vs. V_{CM}



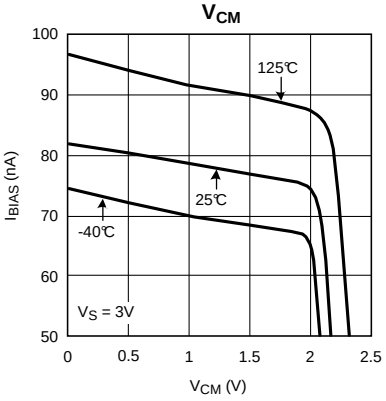
V_{OS} vs. Supply Voltage



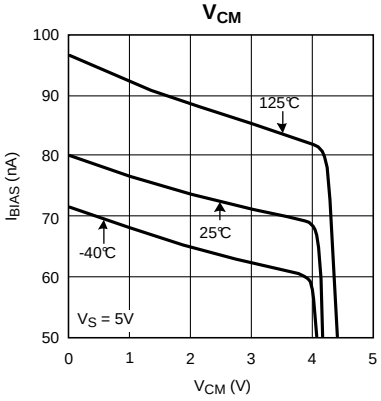
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5V, V^+= 5V, V^-= 0V, V_{CM}= V_S/2

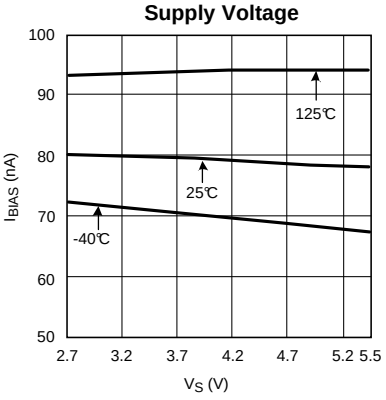
I_{BIAS} vs. V_{CM}



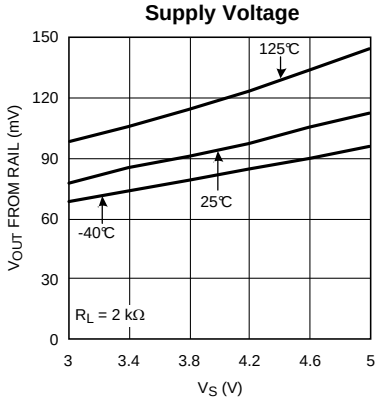
I_{BIAS} vs. V_{CM}



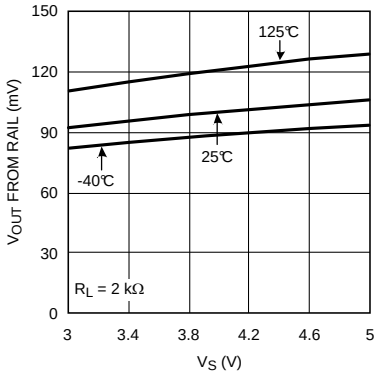
I_{BIAS} vs. Supply Voltage



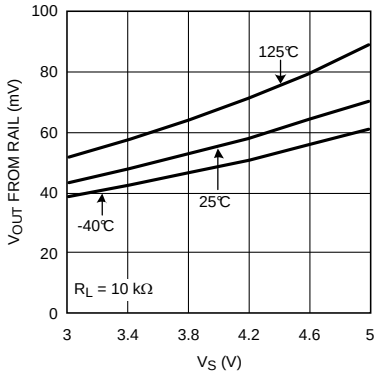
Positive Output Swing vs. Supply Voltage



Negative Output Swing vs. Supply Voltage



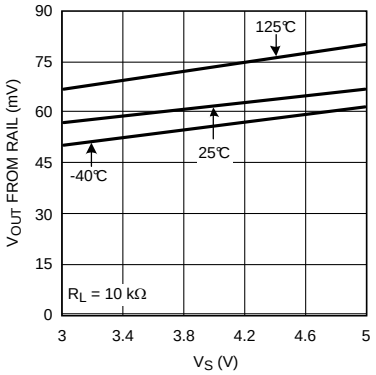
Positive Output Swing vs. Supply Voltage



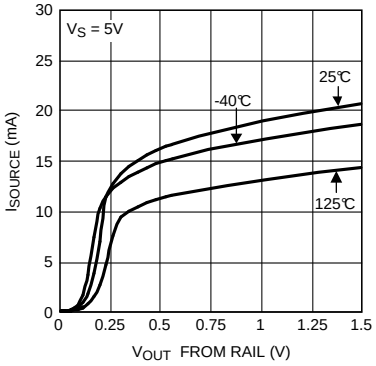
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5V, V^+= 5V, V^-= 0V, V_{CM}= V_S/2

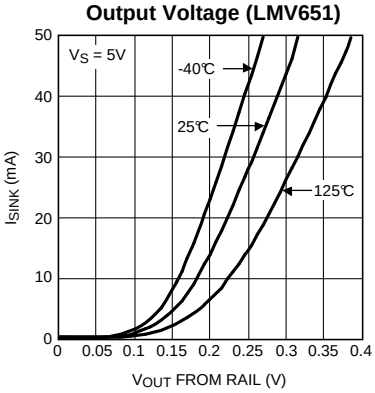
Negative Output Swing vs. Supply Voltage



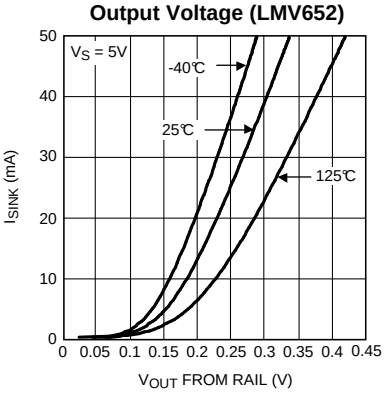
Sourcing Current vs. Output Voltage



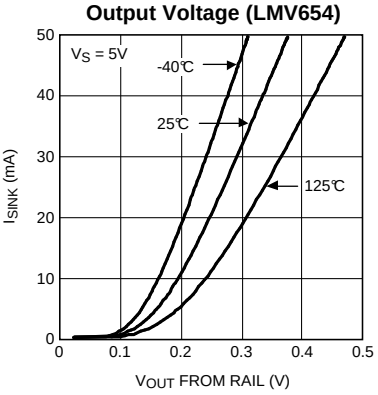
Sinking Current vs. Output Voltage (LMV651)



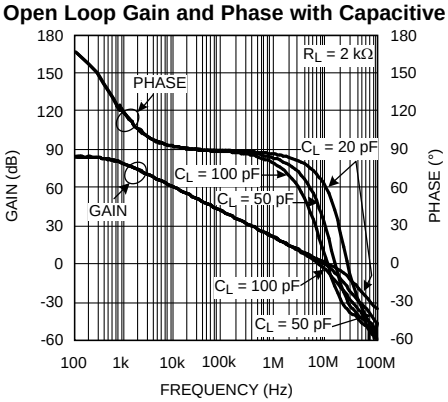
Sinking Current vs. Output Voltage (LMV652)



Sinking Current vs. Output Voltage (LMV654)



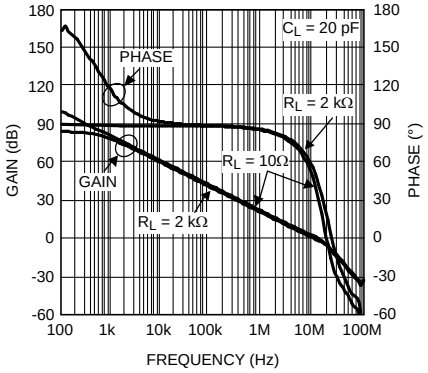
Open Loop Gain and Phase with Capacitive Load



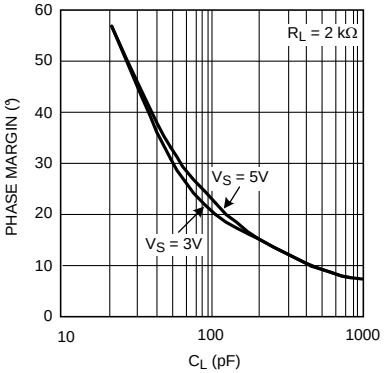
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5V, V^+= 5V, V^-= 0V, V_{CM}= V_S/2

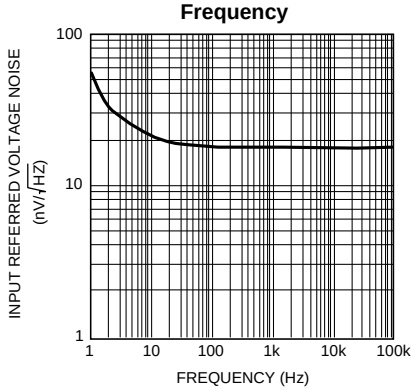
Open Loop Gain and Phase with Resistive Load



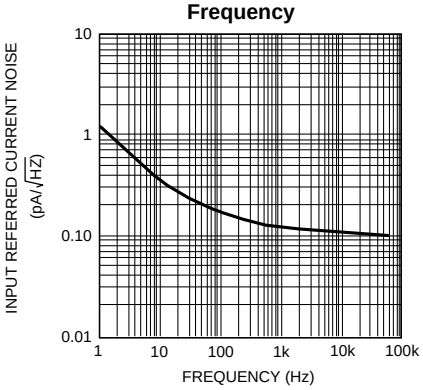
Phase Margin vs. Capacitive Load (Stability)



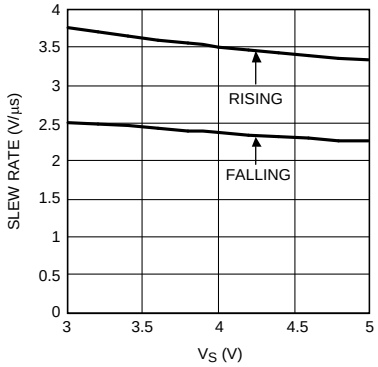
Input Referred Voltage Noise vs. Frequency



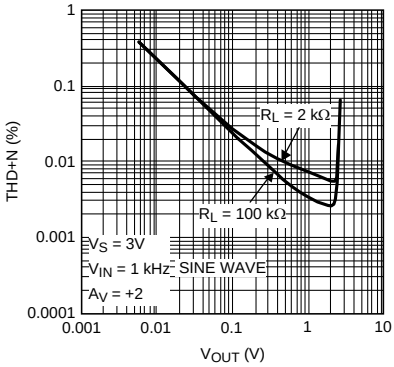
Input Referred Current Noise vs. Frequency



Slew Rate vs. Supply Voltage



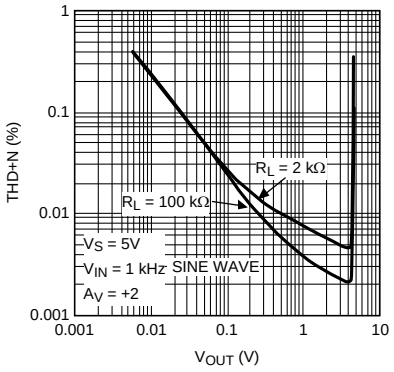
THD+N vs. V_{OUT}



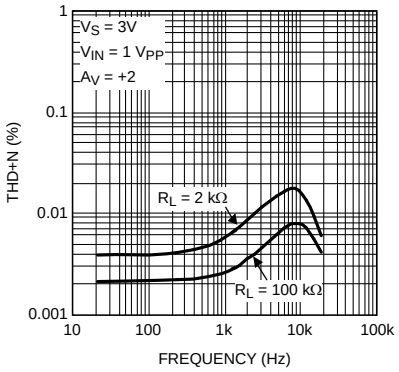
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5V, V^+= 5V, V^-= 0V, V_{CM}= V_S/2

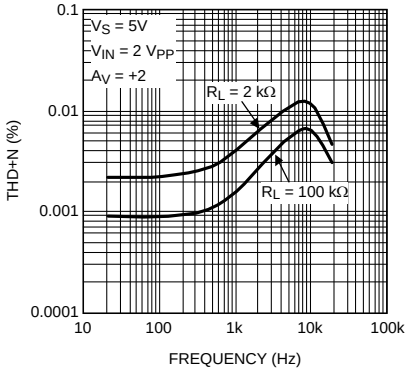
THD+N vs. V_{OUT}



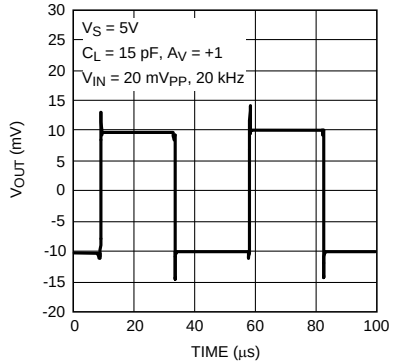
THD+N vs. Frequency



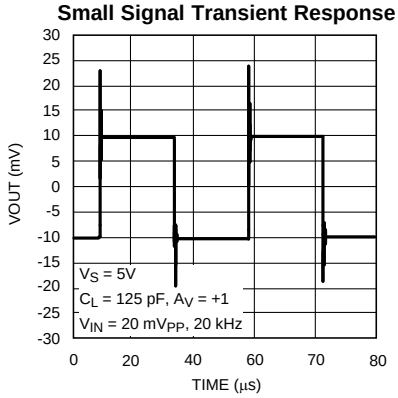
THD+N vs. Frequency



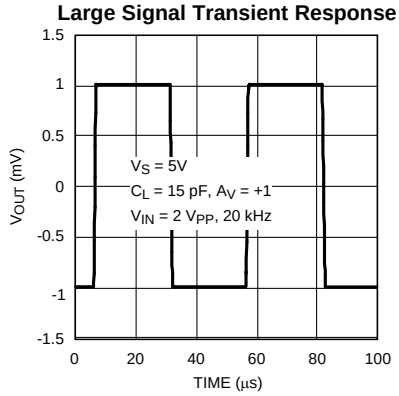
Small Signal Transient Response



Small Signal Transient Response



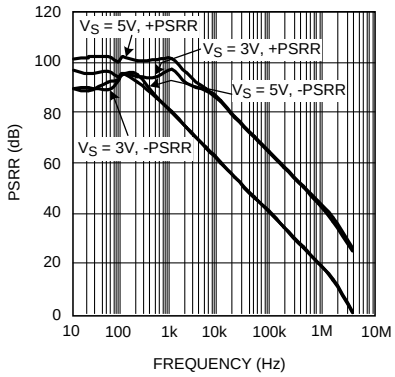
Large Signal Transient Response



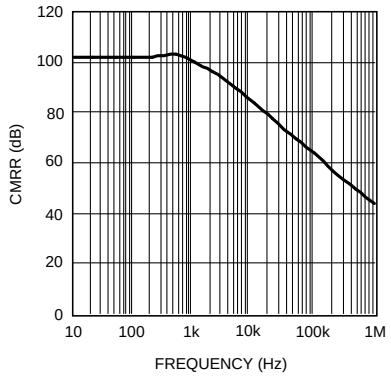
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A= 25°C, V_S= 5V, V^+= 5V, V^-= 0V, V_{CM}= V_S/2

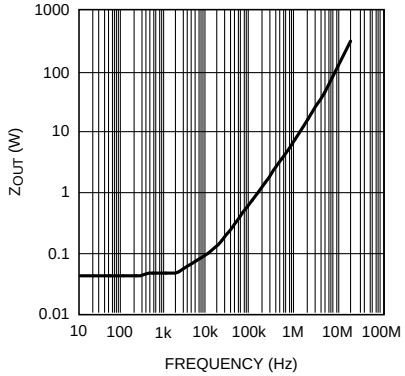
PSRR vs. Frequency



CMRR vs. Frequency



Closed Loop Output Impedance vs. Frequency



Application Information

ADVANTAGES OF THE LMV651/LMV652/LMV654

Low Voltage and Low Power Operation

The LMV651/LMV652/LMV654 have performance guaranteed at supply voltages of 3V and 5V. These parts are guaranteed to be operational at all supply voltages between 2.7V and 5.5V. The LMV651 draws a low supply current of 116 µA, the LMV652 draws 118 µA/channel and the LMV654 draws 122 µA/channel. This family of op amps provides the low voltage and low power amplification which is essential for portable applications.

Wide Bandwidth

Despite drawing the very low supply current of 116 µA, the LMV651/LMV652/LMV654 manage to provide a wide unity gain bandwidth of 12 MHz. This is easily one of the best bandwidth to power ratios ever achieved, and allows these op amps to provide wideband amplification while using the minimum amount of power. This makes this family of parts ideal for low power signal processing applications such as portable media players and other accessories.

Low Input Referred Noise

The LMV651/LMV652/LMV654 provide a flatband input referred voltage noise density of 17 nV/$\sqrt{\text{Hz}}$, which is significantly better than the noise performance expected from a low power op amp. These op amps also feature exceptionally low 1/f noise, with a very low 1/f noise corner frequency of 4 Hz. This makes these parts ideal for low power applications which require decent noise performance, such as PDAs and portable sensors.

Ground Sensing and Rail-to-Rail Output

The LMV651/LMV652/LMV654 each have a rail-to-rail output stage, which provides the maximum possible output dynamic range. This is especially important for applications requiring a large output swing. The input common mode range of this family of devices includes the negative supply rail which allows direct sensing at ground in a single supply operation.

Small Size

The small footprint of the packages for the LMV651/LMV652/LMH654 saves space on printed circuit boards, and enables the design of smaller and more compact electronic products. Long traces between the signal source and the op amp make the signal path susceptible to noise. By using a physically smaller package, these op amps can be placed closer to the signal source, reducing noise pickup and enhancing signal integrity.

STABILITY OF OP AMP CIRCUITS

Stability and Capacitive Loading

If the phase margin of the LMV651/LMV652/LMV654 is plotted with respect to the capacitive load (C_L) at its output, it is seen that the phase margin reduces significantly if C_L is increased beyond 100 pF. This is because the op amp is designed to provide the maximum bandwidth possible for a low supply current. Stabilizing it for higher capacitive loads would have required either a drastic increase in supply current, or a large internal compensation capacitance, which would have reduced the bandwidth of the op amp. Hence, if these devices are to be used for driving higher capacitive loads, they would have to be externally compensated.

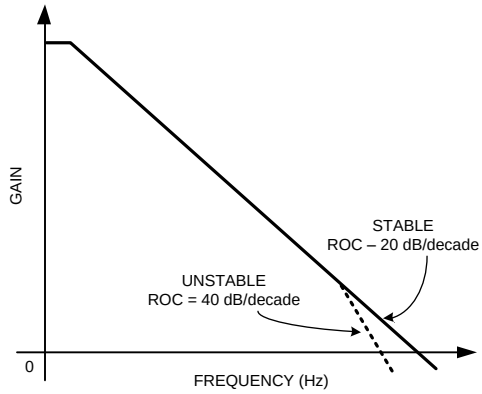


Figure 6. Gain vs. Frequency for an Op Amp

An op amp, ideally, has a dominant pole close to DC, which causes its gain to decay at the rate of 20 dB/decade with respect to frequency. If this rate of decay, also known as the rate of closure (ROC), remains the same until the op amp's unity gain bandwidth, the op amp is stable. If, however, a large capacitance is added to the output of the op amp, it combines with the output impedance of the op amp to create another pole in its frequency response before its unity gain frequency (Figure 6). This increases the ROC to 40 dB/decade and causes instability.

In such a case a number of techniques can be used to restore stability to the circuit. The idea behind all these schemes is to modify the frequency response such that it can be restored to an ROC of 20 dB/decade, which ensures stability.

In The Loop Compensation

Figure 7 illustrates a compensation technique, known as ‘in the loop’ compensation, that employs an RC feedback circuit within the feedback loop to stabilize a non-inverting amplifier configuration. A small series resistance, R_S, is used to isolate the amplifier output from the load capacitance, C_L, and a small capacitance, C_F, is inserted across the feedback resistor to bypass C_L at higher frequencies.

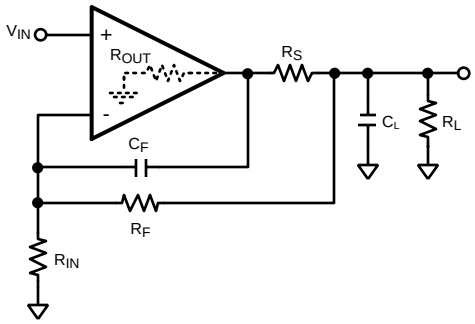


Figure 7. In the Loop Compensation

The values for R_S and C_F are decided by ensuring that the zero attributed to C_F lies at the same frequency as the pole attributed to C_L. This ensures that the effect of the second pole on the transfer function is compensated for by the presence of the zero, and that the ROC is maintained at 20 dB/decade. For the circuit shown in Figure 7 the values of R_S and C_F are given by Equation 1. Values of R_S and C_F required for maintaining stability for different values of C_L, as well as the phase margins obtained, are shown in Table 1. R_F and R_{IN} are taken to be 10 kΩ, R_L is 2 kΩ, while R_{OUT} is taken as 340Ω.

$$R_S = \frac{R_{OUT} R_{IN}}{R_F}$$

$$C_F = \left(\frac{R_F + 2R_{IN}}{R_F^2} \right) C_L R_{OUT} \quad (1)$$

Table 1.

C_L (pF)	R_S (Ω)	C_F (pF)	Phase Margin (°)
150	340	15	39.4
200	340	20	34.6
250	340	25	31.1

Although this methodology provides circuit stability for any load capacitance, it does so at the price of bandwidth. The closed loop bandwidth of the circuit is now limited by R_F and C_F.

Compensation By External Resistor

In some applications it is essential to drive a capacitive load without sacrificing bandwidth. In such a case, in the loop compensation is not viable. A simpler scheme for compensation is shown in Figure 8. A resistor, R_{ISO}, is placed in series between the load capacitance and the output. This introduces a zero in the circuit transfer function, which counteracts the effect of the pole formed by the load capacitance, and ensures stability. The value of R_{ISO} to be used should be decided depending on the size of C_L and the level of performance desired. Values ranging from 5Ω to 50Ω are usually sufficient to ensure stability. A larger value of R_{ISO} will result in a system with lesser ringing and overshoot, but will also limit the output swing and the short circuit current of the circuit.

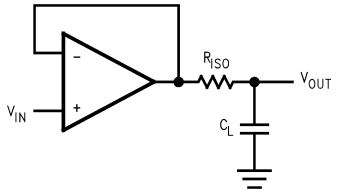


Figure 8. Compensation by Isolation Resistor

Typical Applications

HIGH GAIN LOW POWER AMPLIFIERS

With a low supply current, low power operation, and low harmonic distortion, the LMV651/LMV652/LMV654 are ideal for wide-bandwidth, high gain amplification. The wide unity gain bandwidth allows these parts to provide large gain over a wide frequency range, while driving loads as low as 2 kΩ with less than 0.003% distortion. Two amplifier circuits are shown in Figure 9 and Figure 10. Figure 9 is an inverting amplifier, with a 100 kΩ feedback resistor, R_2, and a 1 kΩ input resistor, R_1, and provides a gain of −100. With the LMV651/LMV652/LMV654 these circuits can provide gain of −100 with a −3 dB bandwidth of 120 kHz, for a quiescent current as low as 116 µA. Similarly, the circuit in Figure 10, a non-inverting amplifier with a gain of 1001, can provide that gain with a −3 dB bandwidth of 12 kHz, for a similar low quiescent power dissipation. Coupling capacitors C_{C1} and C_{C2} can be added to isolate the circuit from DC voltages, while R_{B1} and R_{B2} provide DC biasing. A feedback capacitor C_F can also be added to improve compensation.

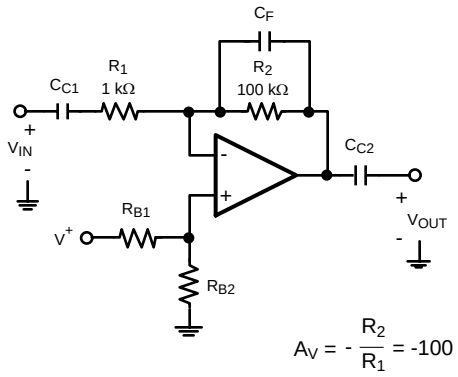


Figure 9. High Gain Inverting Amplifier

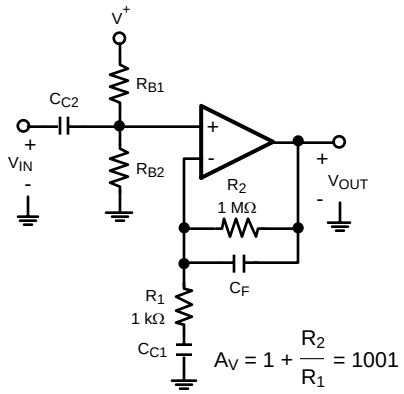


Figure 10. High Gain Non-Inverting Amplifier

ACTIVE FILTERS

With a wide unity gain bandwidth of 12 MHz, low input referred noise density and a low power supply current, the LMV651/LMV652/LMV654 are well suited for low-power filtering applications. Active filter topologies, like the Sallen-Key low pass filter shown in Figure 11, are very versatile, and can be used to design a wide variety of filters (Chebyshev, Butterworth or Bessel). The Sallen-Key topology, in particular, can be used to attain a wide range of Q, by using positive feedback to reject the undesired frequency range.

In the circuit shown in Figure 11, the two capacitors appear as open circuits at lower frequencies and the signal is simply buffered to the output. At high frequencies the capacitors appear as short circuits and the signal is shunted to ground by one of the capacitors before it can be amplified. Near the cut-off frequency, where the impedance of the capacitances is on the same order as R_g and R_f, positive feedback through the other capacitor allows the circuit to attain the desired Q. The ratio of the two resistors, m^2, provides a knob to control the value of Q obtained.

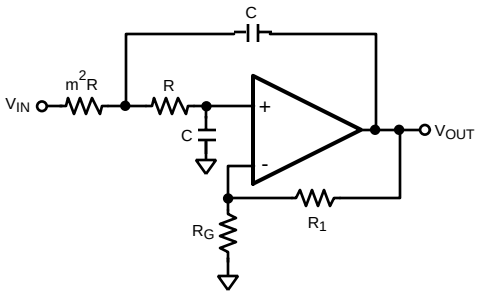


Figure 11. Sallen-Key Low Pass Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV651MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AY2A	Samples
LMV651MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AY2A	Samples
LMV651MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A93	Samples
LMV651MGX	ACTIVE	SC70	DCK	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	A93	Samples
LMV651MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A93	Samples
LMV652MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AB3A	Samples
LMV652MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AB3A	Samples
LMV654MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV654MT	Samples
LMV654MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV654MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

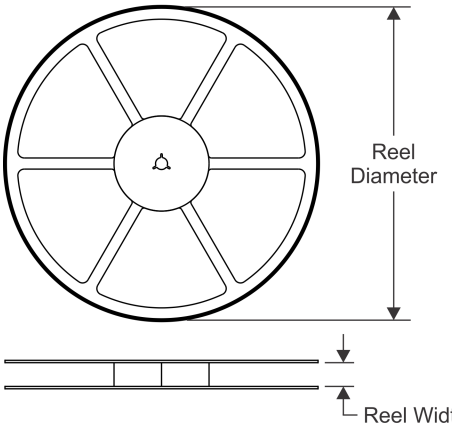
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

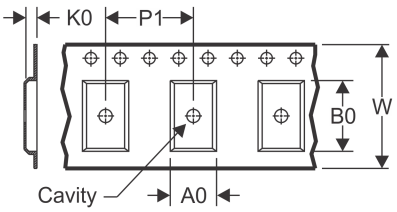
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

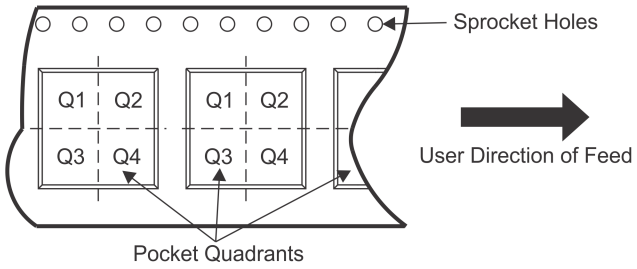


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

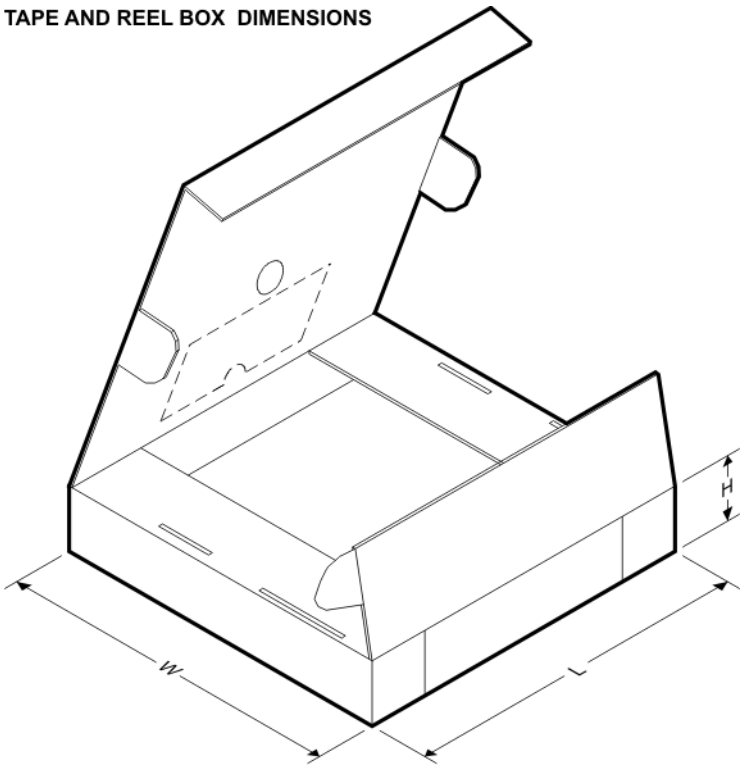
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV651MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV651MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV651MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV651MGX	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV651MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV652MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV652MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV654MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

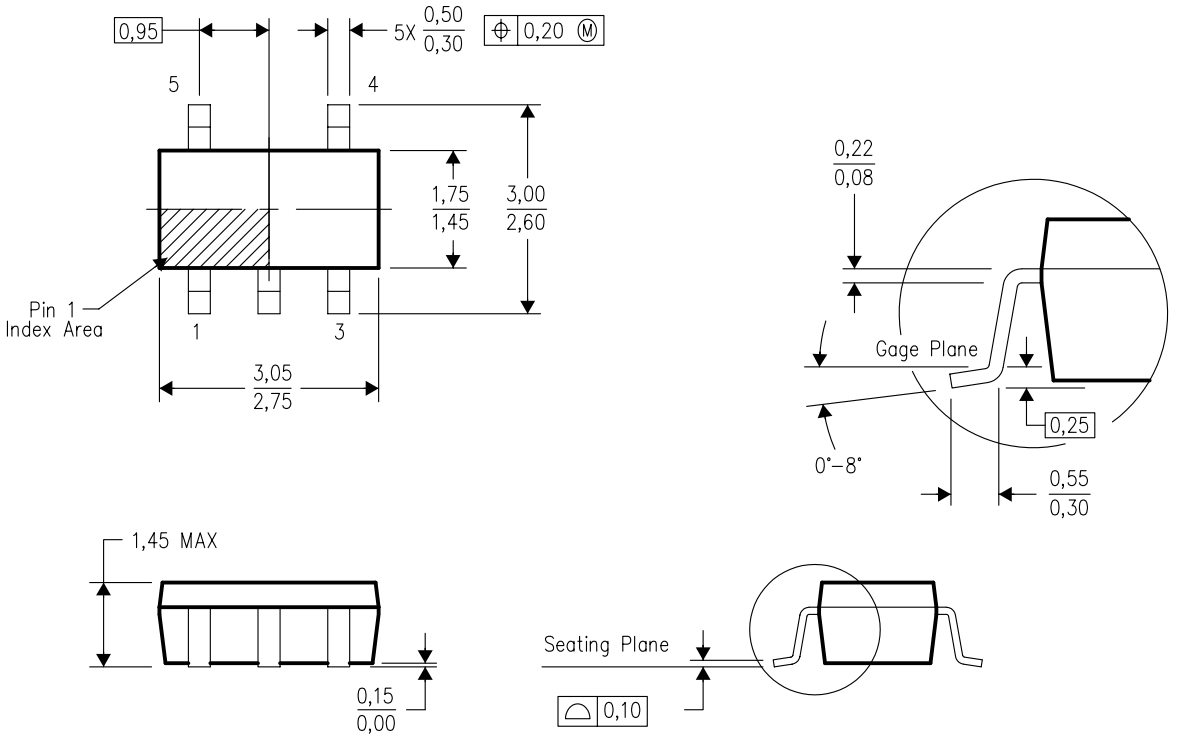
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV651MF/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV651MFX/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV651MG/NOPB	SC70	DCK	5	1000	203.0	190.0	41.0
LMV651MGX	SC70	DCK	5	3000	206.0	191.0	90.0
LMV651MGX/NOPB	SC70	DCK	5	3000	206.0	191.0	90.0
LMV652MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV652MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV654MTX/NOPB	TSSOP	PW	14	2500	349.0	337.0	45.0

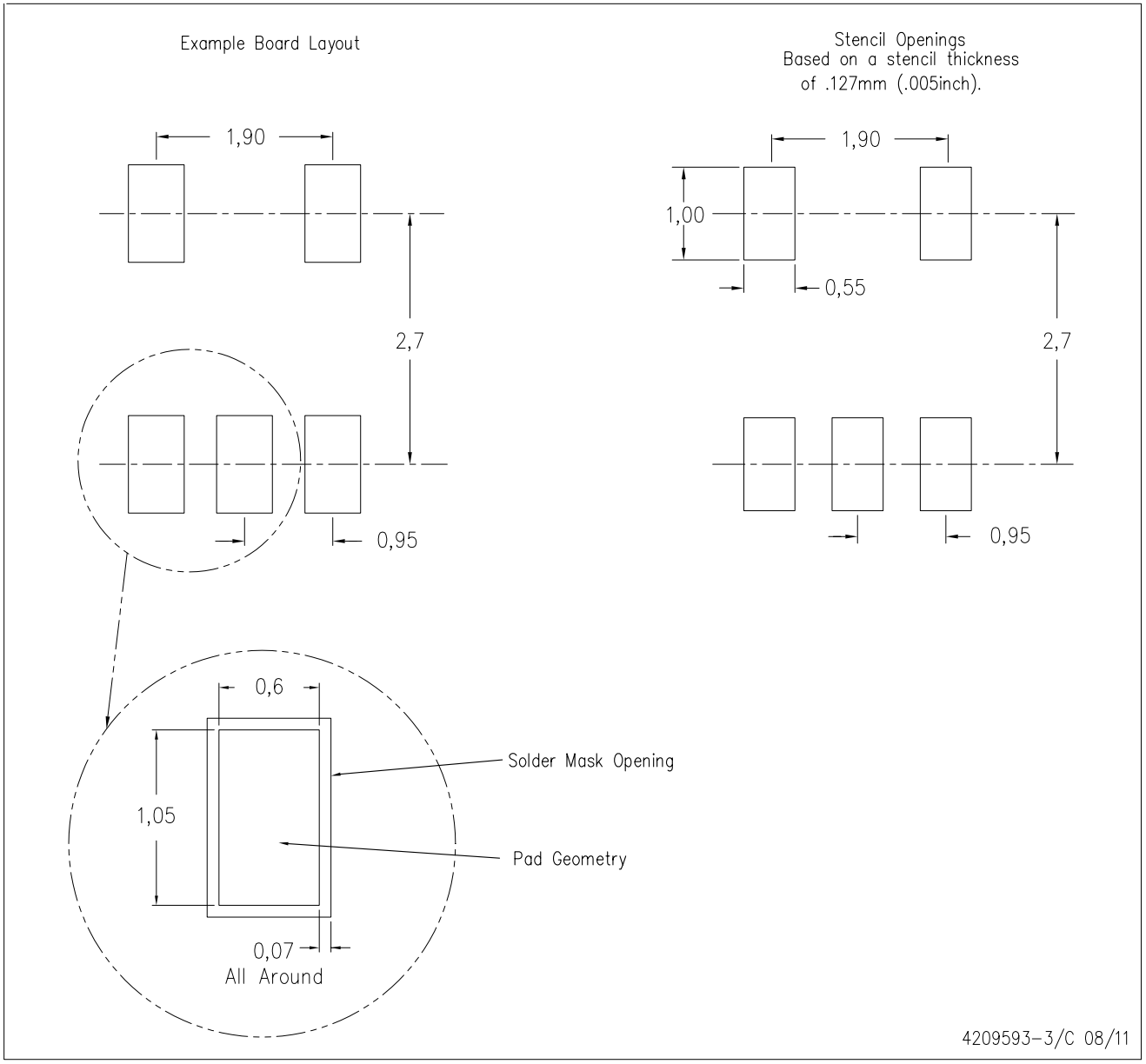
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

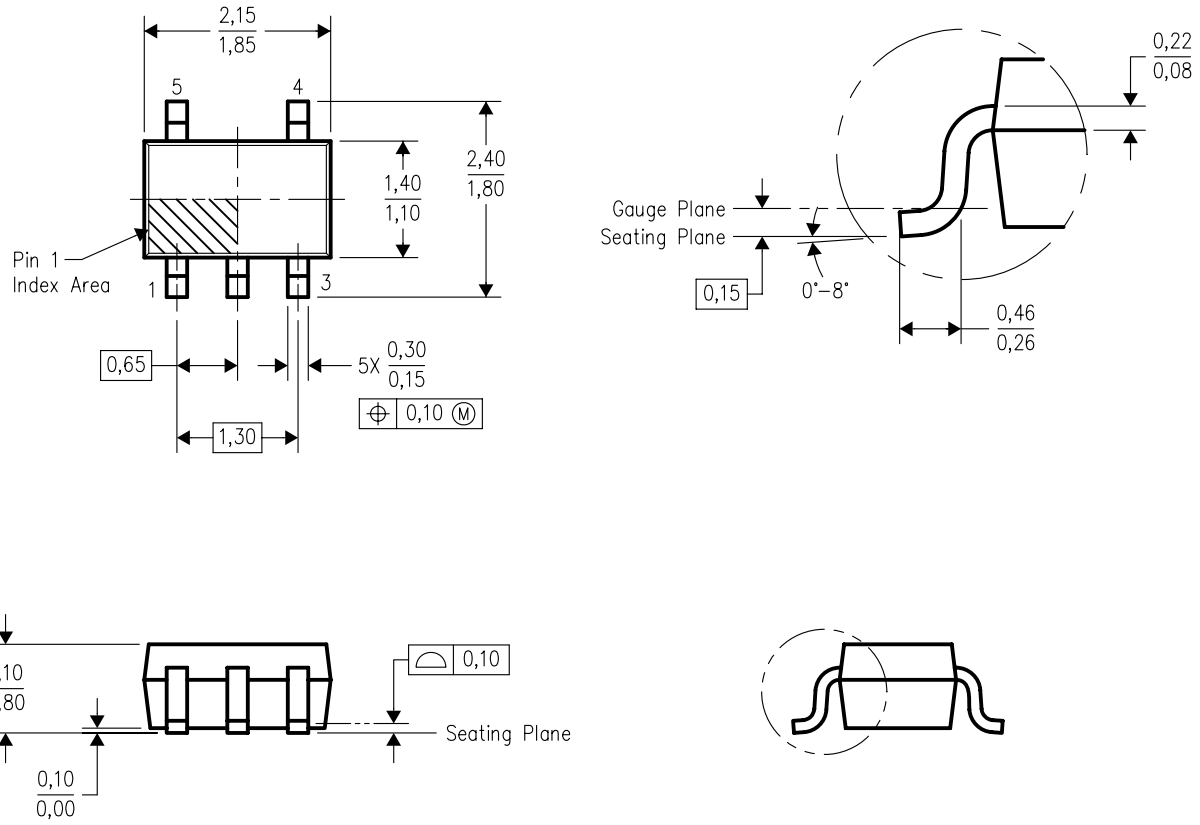
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

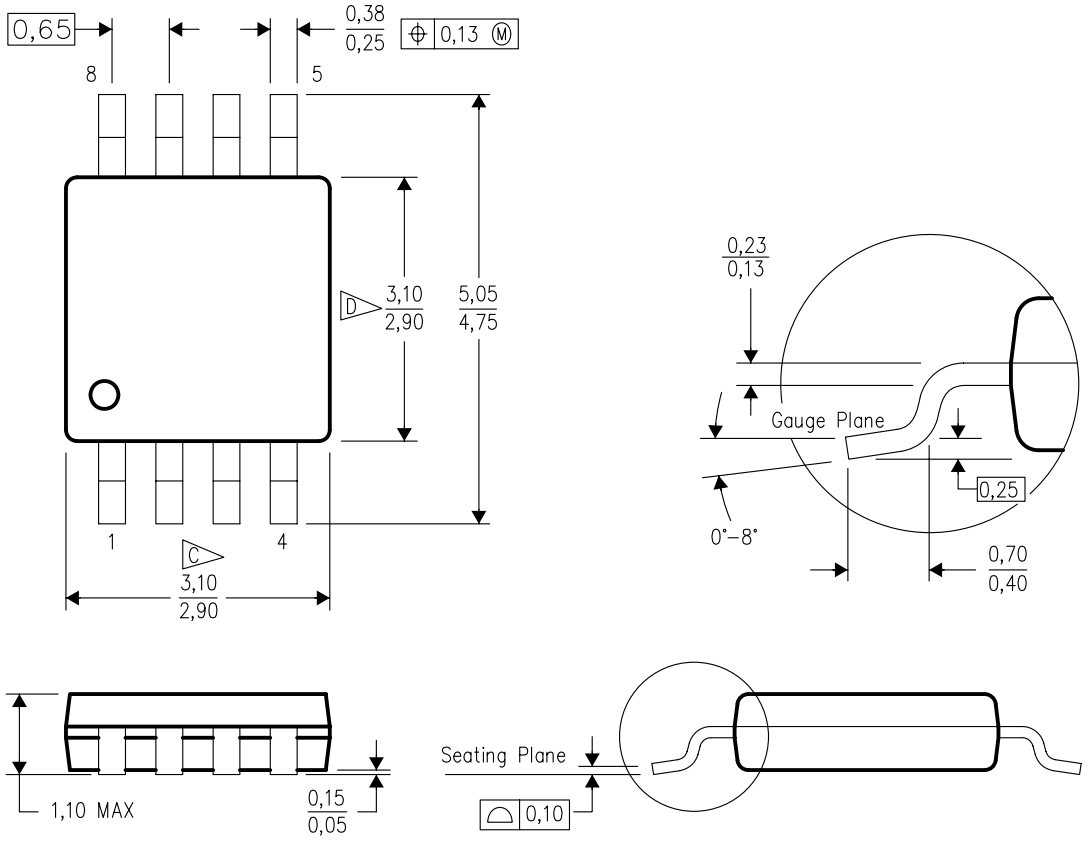
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

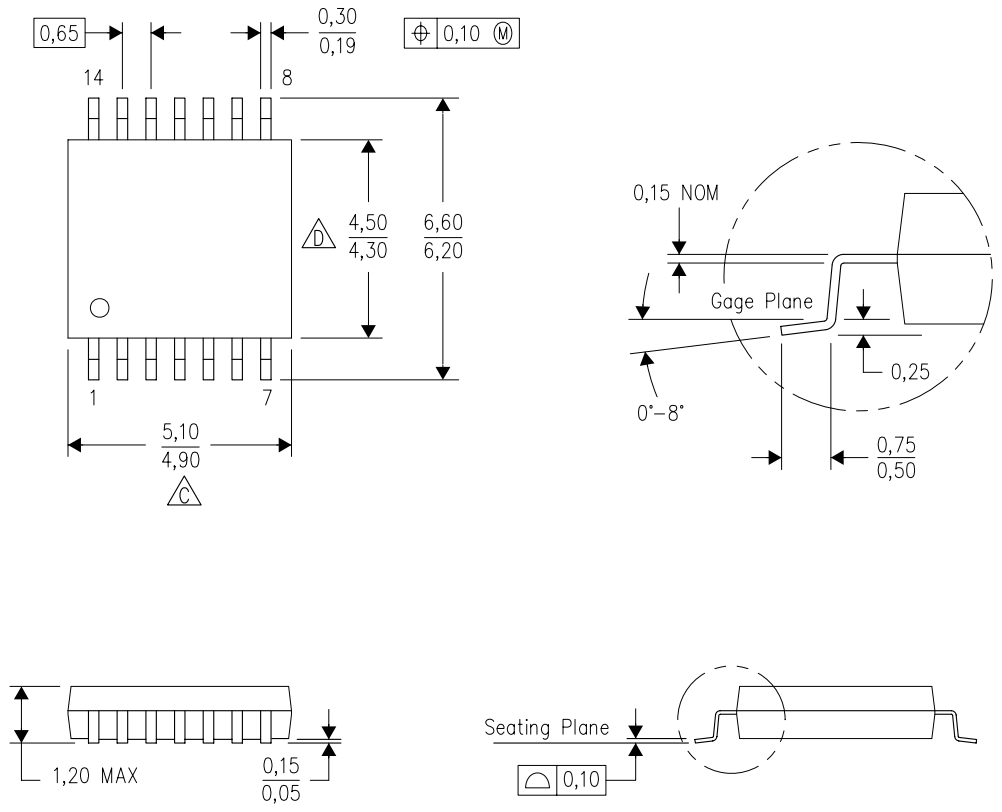
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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