LMV710/LMV711/LMV715 Low Power, RRIO Operational Amplifiers with High Output Current Drive and Shutdown Option

Check for Samples: LMV710-N, LMV711-N, LMV715-N

FEATURES

- **(For 5V supply, typical unless otherwise noted).**
- **Low offset voltage 3 mV, max**
- **Gain-bandwidth product 5 MHz, typ**
- **Slew rate 5 V/µs, typ**
- **Space saving packages 5-Pin and 6-Pin SOT23**
- **Turn on time from shutdown <10 µs**
- **Industrial temperature range −40°C to +85°C**
- **Supply current in shutdown mode 0.2 µA, typ**
- **Guaranteed 2.7V and 5V performance**
- **Unity gain stable**
- **Rail-to-rail input and output**
- **Capable of driving 600Ω load**

APPLICATIONS

- **Wireless phones**
- **GSM/TDMA/CDMA power amp control**
- **AGC, RF power detector**
- **Temperature compensation**
- **Wireless LAN**
- **Bluetooth**
- **HomeRF**

DESCRIPTION

The LMV710/LMV711/LMV715 are BiCMOS operational amplifiers with a CMOS input stage. These devices have greater than RR input common mode voltage range, rail-to-rail output and high output current drive. They offer a bandwidth of 5 MHz and a slew rate of 5 V/µs.

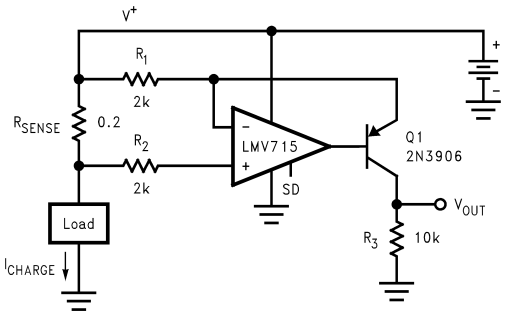
On the LMV711/LMV715, a separate shutdown pin can be used to disable the device and reduces the supply current to 0.2 µA (typical). They also feature a turn on time of less than 10 µs. It is an ideal solution for power sensitive applications, such as cellular phone, pager, palm computer, etc. In addition, once the LMV715 is in shutdown the output will be “Tri-stated”.

The LMV710 is offered in the space saving 5-Pin SOT23 Tiny package. The LMV711/LMV715 are offered in the space saving 6-Pin SOT23 Tiny package.

The LMV710/LMV711/LMV715 are designed to meet the demands of low power, low cost, and small size required by cellular phones and similar battery powered portable electronics.

Typical Application

Figure 1. High Side Current Sensing



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\Omega \bullet I_{Charge}$$

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Machine Model	100V
Human Body Model	2000V
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	(V^+) + 0.4V (V^-) − 0.4V
Supply Voltage $(V^+ - V^-)$	5.5V
Output Short Circuit to V^+	(3)
Output Short Circuit to V^-	(4)
Current at Input Pin	± 10 mA
Mounting Temp.	
Infrared or Convection (20 sec)	235°C
Storage Temperature Range	−65°C to 150°C
Junction Temperature (T_{JMAX}) (5)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Human body model, 1.5 kΩ in series with 100 pF. Machine model, 0Ω in series with 100 pF.
(3) Shorting circuit output to V^+ will adversely affect reliability.
(4) Shorting circuit output to V^- will adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings (1)

Supply Voltage	2.7V to 5.0V
Temperature Range	−40°C to 85°C
Thermal Resistance (θ_{JA})	
MF05A Package, 5-Pin SOT23	265 °C/W
MF06A package, 6-Pin SOT23	265 °C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	Limits (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.85V and V_{CM} = 1.85V	0.4	3 **3.2**	mV max
I_B	Input Bias Current		4		pA
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 2.7V	75	50 **45**	dB min
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V_{CM} = 0.85V	110	70 **68**	dB min
		2.7V ≤ V^+ ≤ 5V, V_{CM} = 1.85V	95	70 **68**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	-0.3	-0.2	V
			3	2.9	
I_{SC}	Output Short Circuit Current	Sourcing V_O = 0V	28	15 **12**	mA min
		Sinking V_O = 2.7V	40	25 **22**	mA min
V_O	Output Swing	R_L = 10 kΩ to 1.35V	2.68	2.62 **2.60**	V min
			0.01	0.12 **0.15**	V max
		R_L = 600Ω to 1.35V	2.55	2.52 **2.50**	V min
			0.05	0.23 **0.30**	V max
V_O (SD)	Output Voltage Level in Shutdown Mode (LMV711 only)		50	200	mV
I_O (SD)	Output Leakage Current in Shutdown Mode (LMV715 Only)		1		pA
C_O (SD)	Output Capacitance in Shutdown Mode (LMV715 Only)		32		pF
I_S	Supply Current	On Mode	1.22	1.7 **1.9**	mA max
		Shutdown Mode, V_{SD} = 0V	0.002	10	µA
A_V	Large Signal Voltage	Sourcing R_L = 10 kΩ V_O = 1.35V to 2.3V	115	80 **76**	dB min
		Sinking R_L = 10 kΩ V_O = 0.4V to 1.35V	113	80 **76**	dB min
		Sourcing R_L = 600Ω V_O = 1.35V to 2.2V	110	80 **76**	dB min
		Sinking R_L = 600Ω V_O = 0.5V to 1.35V	100	80 **76**	dB min
SR	Slew Rate	(3)	5		V/µs
GBWP	Gain-Bandwidth Product		5		MHz
φ_m	Phase Margin		60		Deg
T_{ON}	Turn-on Time from Shutdown		<10		µs

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Number specified is the slower of the positive and negative slew rates.

2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	Limits (2)	Units
V_{SD}	Shutdown Pin Voltage Range	On Mode	1.5 to 2.7	2.4 to 2.7	V
		Shutdown Mode	0 to 1	0 to 0.8	V
e_n	Input-Referred Voltage Noise	f = 1 kHz	20		$\frac{nV}{\sqrt{Hz}}$

3.2V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 3.2V, V^- = 0V, V_{CM} = 1.6V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
V_O	Output Swing	I_O = 6.5 mA	3.0	2.95 **2.92**	V min
			0.01	0.18 **0.25**	V max

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	Limits (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.85V and V_{CM} = 1.85V	0.4	3 **3.2**	mV max
I_B	Input Bias Current		4		pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	70	50 **48**	dB min
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V_{CM} = 0.85V	110	70 **68**	dB min
		2.7V ≤ V^+ ≤ 5V, V_{CM} = 1.85V	95	70 **68**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	-0.3	−0.2	V
			5.3	5.2	
I_{SC}	Output Short Circuit Current	Sourcing V_O = 0V	35	25 **21**	mA min
		Sinking V_O = 5V	40	25 **21**	mA min
V_O	Output Swing	R_L = 10 kΩ to 2.5V	4.98	4.92 **4.90**	V min
			0.01	0.12 **0.15**	V max
		R_L = 600Ω to 2.5V	4.85	4.82 **4.80**	V min
			0.05	0.23 **0.3**	V max
V_O (SD)	Output Voltage Level in Shutdown Mode (LMV711 only)		50	200	mV
I_O (SD)	Output Leakage Current in Shutdown Mode (LMV715 Only)		1		pA
C_O (SD)	Output Capacitance in shutdown Mode (LMV715 Only)		32		pF
I_S	Supply Current	On Mode	1.17	1.7 **1.9**	mA max
		Shutdown Mode	0.2	10	µA
A_V	Large Signal Voltage Gain	Sourcing R_L = 10 kΩ V_O = 2.5V to 4.6V	123	80 **76**	dB min
		Sinking R_L = 10 kΩ V_O = 0.4V to 2.5V	120	80 **76**	dB min
		Sourcing R_L = 600Ω V_O = 2.5V to 4.5V	110	80 **76**	dB min
		Sinking R_L = 600Ω V_O = 0.5V to 2.5V	118	80 **76**	dB min
SR	Slew Rate	(3)	5		V/µs
GBWP	Gain-Bandwidth Product		5		MHz
φ_m	Phase Margin		60		Deg
T_{ON}	Turn-on Time from Shutdown		<10		µs

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Number specified is the slower of the positive and negative slew rates.

5V Electrical Characteristics (continued)

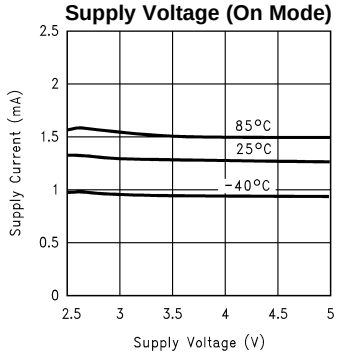
Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (1)	Limits (2)	Units
V_{SD}	Shutdown Pin Voltage Range	On Mode	2 to 5	2.4 to 5	V
		Shutdown Mode	0 to 1.5	0 to 0.8	
e_n	Input-Referred Voltage Noise	f = 1 kHz	20		$\frac{nV}{\sqrt{Hz}}$

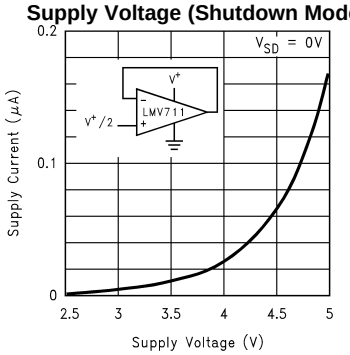
Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

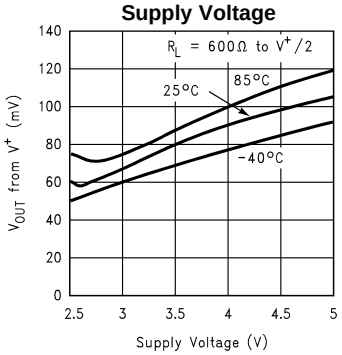
Supply Current vs. Supply Voltage (On Mode)



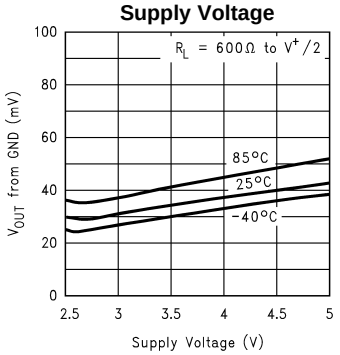
LMV711/LMV715 Supply Current vs. Supply Voltage (Shutdown Mode)



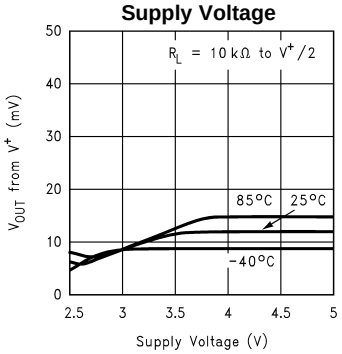
Output Positive Swing vs. Supply Voltage



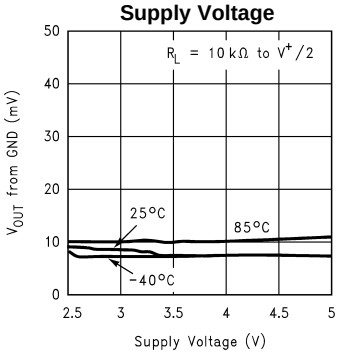
Output Negative Swing vs. Supply Voltage



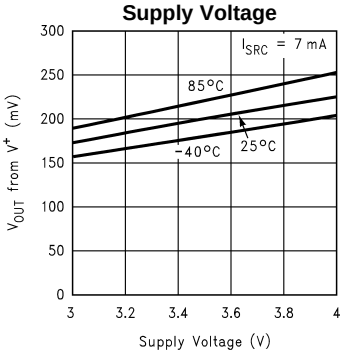
Output Positive Swing vs. Supply Voltage



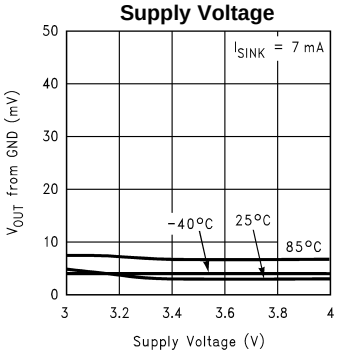
Output Negative Swing vs. Supply Voltage



Output Positive Swing vs. Supply Voltage



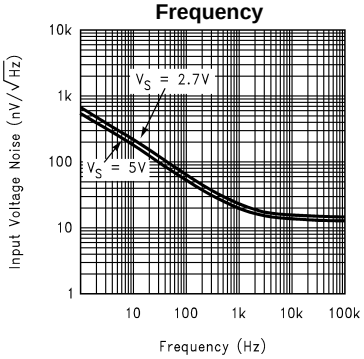
Output Negative Swing vs. Supply Voltage



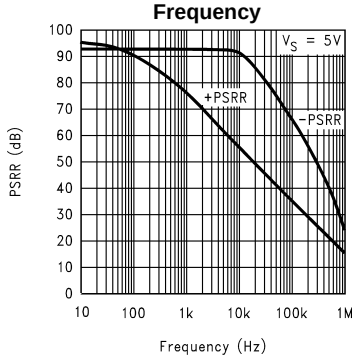
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

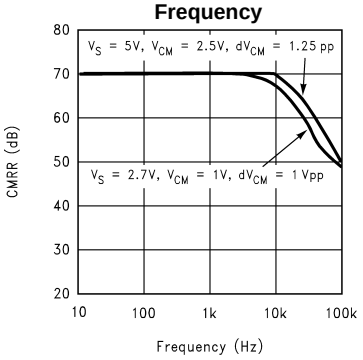
Input Voltage Noise vs. Frequency



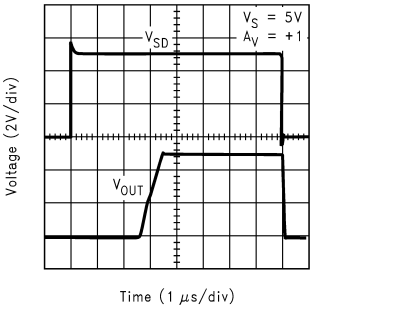
PSRR vs. Frequency



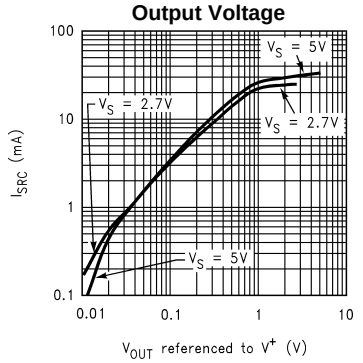
CMRR vs. Frequency



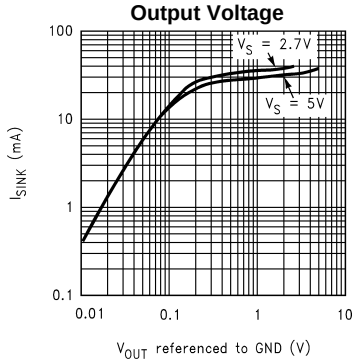
LMV711/LMV715 Turn On Characteristics



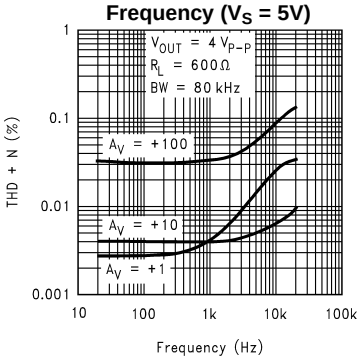
Sourcing Current vs. Output Voltage



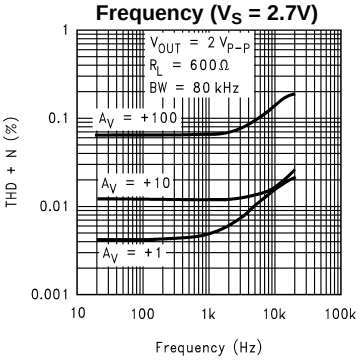
Sinking Current vs. Output Voltage



THD+N vs. Frequency (V_S = 5V)



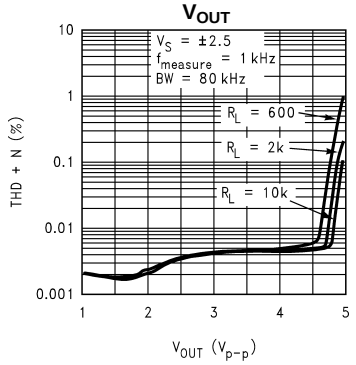
THD+N vs. Frequency (V_S = 2.7V)



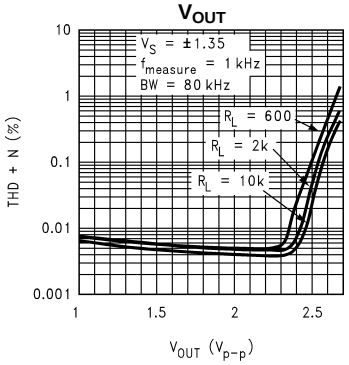
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

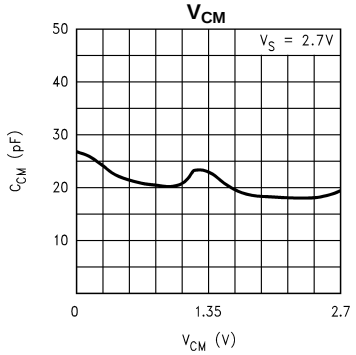
THD+N vs. V_{OUT}



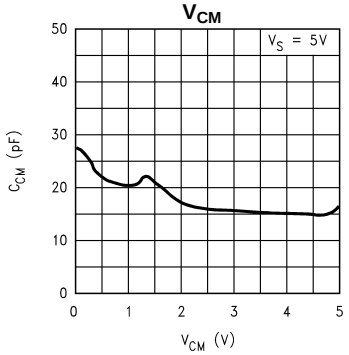
THD+N vs. V_{OUT}



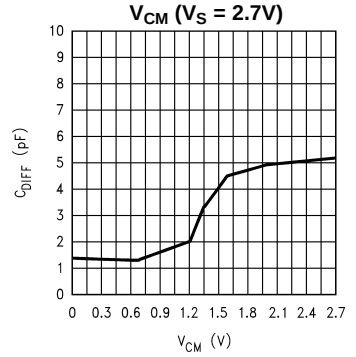
C_{CM} vs. V_{CM}



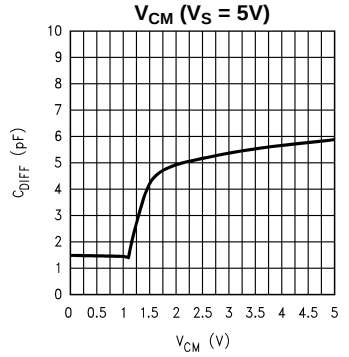
C_{CM} vs. V_{CM}



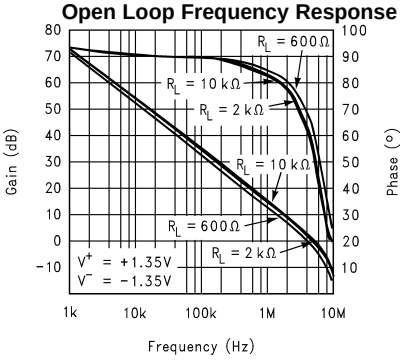
C_{DIFF} vs. V_{CM} (V_S = 2.7V)



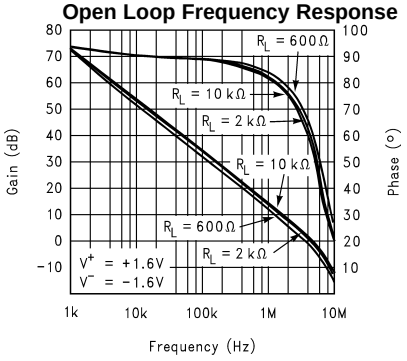
C_{DIFF} vs. V_{CM} (V_S = 5V)



Open Loop Frequency Response



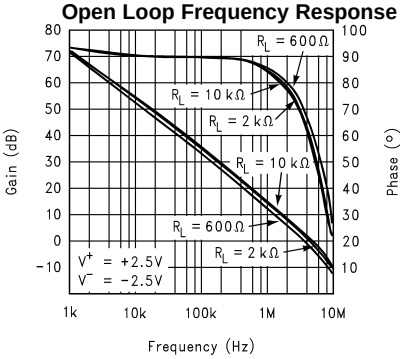
Open Loop Frequency Response



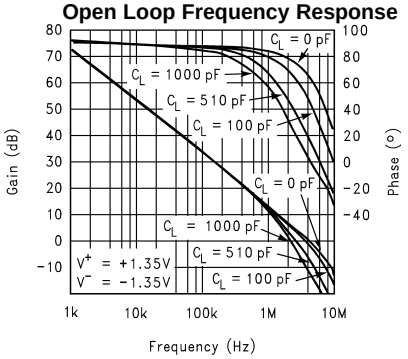
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

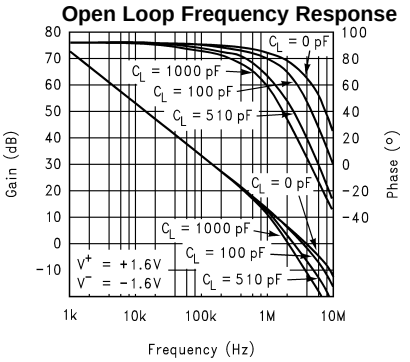
Open Loop Frequency Response



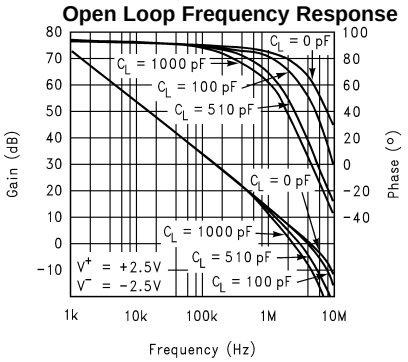
Open Loop Frequency Response



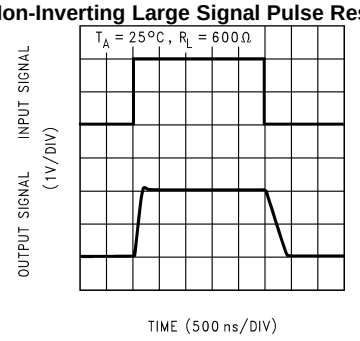
Open Loop Frequency Response



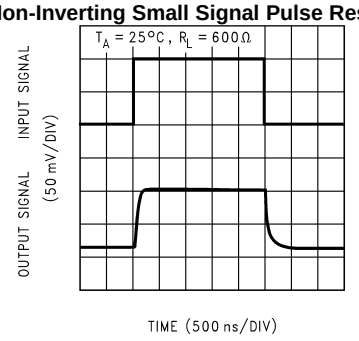
Open Loop Frequency Response



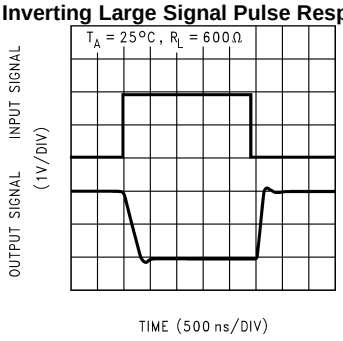
Non-Inverting Large Signal Pulse Response



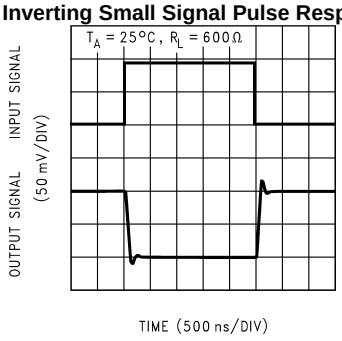
Non-Inverting Small Signal Pulse Response



Inverting Large Signal Pulse Response



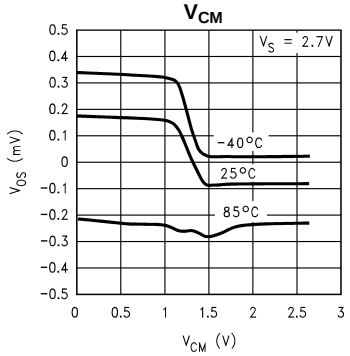
Inverting Small Signal Pulse Response



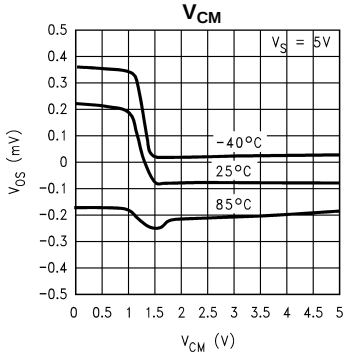
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

V_{OS} vs. V_{CM}



V_{OS} vs. V_{CM}



Application Information

SUPPLY BYPASSING

The application circuits in this datasheet do not show the power supply connections and the associated bypass capacitors for simplification. When the circuits are built, it is always required to have bypass capacitors. Ceramic disc capacitors (0.1 µF) or solid tantalum (1 µF) with short leads, and located close to the IC are usually necessary to prevent interstage coupling through the power supply internal impedance. Inadequate bypassing will manifest itself by a low frequency oscillation or by high frequency instabilities. Sometimes, a 10 µF (or larger) capacitor is used to absorb low frequency variations and a smaller 0.1 µF disc is paralleled across it to prevent any high frequency feedback through the power supply lines.

SHUTDOWN MODE

The LMV711/LMV715 have a shutdown pin. To conserve battery life in portable applications, they can be disabled when the shutdown pin voltage is pulled low. For LMV711 during shutdown mode, the output stays at about 50 mV from the lower rail, and the current drawn from the power supply is 0.2 µA (typical). This makes the LMV711 an ideal solution for power sensitive applications. For the LMV715 during shutdown mode, the output will be “Tri-stated”.

The shutdown pin should never be left unconnected. In applications where shutdown operation is not needed and the LMV711 or LMV715 is used, the shutdown pin should be connected to V^+. Leaving the shutdown pin floating will result in an undefined operation mode and the device may oscillate between shutdown and active modes.

RAIL-TO-RAIL INPUT

The rail-to-rail input is achieved by using paralleled PMOS and NMOS differential input stages. (See Simplified Schematics in this datasheet). When the common mode input voltage changes from ground to the positive rail, the input stage goes through three modes. First, the NMOS pair is cutoff and the PMOS pair is active. At around 1.4V, both PMOS and NMOS pairs operate, and finally the PMOS pair is cutoff and NMOS pair is active. Since both input stages have their own offset voltage (V_{OS}), the offset of the amplifier becomes a function of the common-mode input voltage. See curves for V_{OS} vs. V_{CM} in curve section.

As shown in the curve, the V_{OS} has a crossover point at 1.4V above V^-. Proper design must be done in both DC and AC coupled applications to avoid problems. For large input signals that include the V_{OS} crossover point in their dynamic range, it will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover point. For example, in a unity gain buffer configuration and with V_S = 5V, a 3V peak-to-peak signal center at 2.5V will contain input-crossover distortion. To avoid this, the input signal should be centered at 3.5V instead. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier. See Figure 2. In this circuit, the common mode DC voltage (V_{CM}) can be set at a level away from the V_{OS} crossover point.

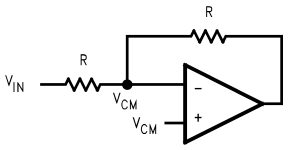


Figure 2.

When the input is a small signal and this small signal falls inside the V_{OS} transition range, the gain, CMRR and some other parameters will be degraded. To resolve this problem, the small signal should be placed such that it avoids the V_{OS} crossover point.

To achieve maximum output swing, the output should be biased at mid-supply. This is normally done by biasing the input at mid-supply. But with supply voltage range from 2V to 3.4V, the input of the op amp should not be biased at mid-supply because of the transition of the V_{OS}. Figure 3 shows an example of how to get away from the V_{OS} crossover point and maintain a maximum swing with a 2.7V supply. Figure 4 shows the waveforms of V_{IN} and V_{OUT}.

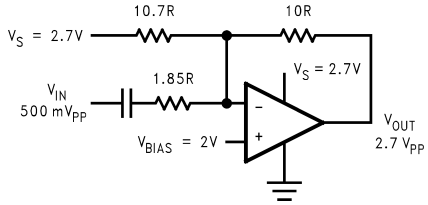


Figure 3.

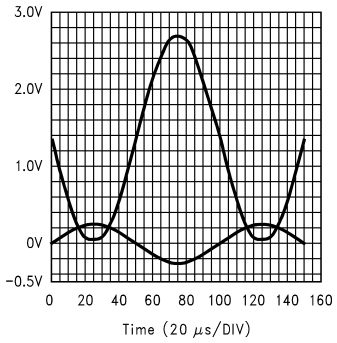


Figure 4.

The inputs can be driven 300 mV beyond the supply rails without causing phase reversal at the output. However, the inputs should not be allowed to exceed the maximum ratings.

COMPENSATION OF INPUT CAPACITANCE

In the application (Figure 5) where a large feedback resistor is used, the feedback resistor can react with the input capacitance of the op amp and introduce an additional pole to the close loop frequency response.

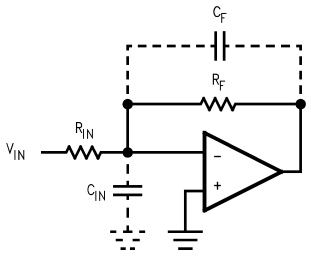


Figure 5. Cancelling the Effect of Input Capacitance

This pole occurs at frequency f_p , where

$$f_P = \frac{1}{2\pi(R_{IN}||R_F)C_{IN}} \quad (1)$$

Any stray capacitance due to external circuit board layout, any source capacitance from transducer or photodiode connected to the summing node will also be added to the input capacitance. If f_p is less than or close to the unity-gain bandwidth (5 MHz) of the op amp, the phase margin of the loop is reduced and can cause the system to be unstable.

To avoid this problem, make sure that f_p occurs at least 2 octaves beyond the expected −3 dB frequency corner of the close loop frequency response. If not, a feedback capacitor C_F can be placed in parallel with R_F such that

$$\frac{1}{2\pi R_F C_F} = \frac{1}{2\pi(R_{IN}||R_F)(C_F + C_{IN})} \quad (2)$$

The paralleled R_F and C_F introduce a zero, which cancels the effect from the pole.

CAPACITIVE LOAD TOLERANCE

The LMV710/LMV711/ LMV715 can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, circuit in Figure 6 can be used.

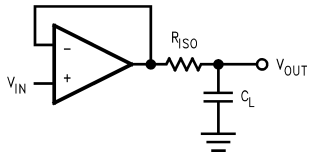


Figure 6. Indirectly Driving A Capacitive Load using Resistive Isolation

In Figure 6, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. But the DC accuracy is not great when the R_{ISO} gets bigger. If there were a load resistor in Figure 6, the output would be voltage divided by R_{ISO} and the load resistor.

The circuit in Figure 7 is an improvement to the one in Figure 6 because it provides DC accuracy as well as AC stability. In this circuit, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F . This in turn will slow down the pulse response.

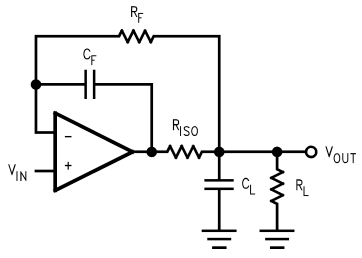


Figure 7. Indirectly Driving A Capacitive A Load with DC Accuracy

APPLICATION CIRCUITS
PEAK DETECTOR

Peak detectors are used in many applications, such as test equipment, measurement instrumentation, ultrasonic alarm systems, etc. Figure 8 shows the schematic diagram of a peak detector using LMV710 or LMV711 or LMV715. This peak detector basically consists of a clipper, a parallel RC network, and a voltage follower.

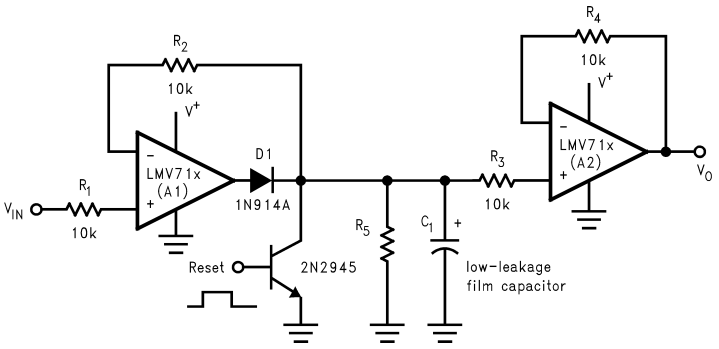


Figure 8. Peak Detector

The capacitor C_1 is first discharged by applying a positive pulse to the reset transistor. When a positive voltage V_{IN} is applied to the input, the input voltage is higher than the voltage across C_1. The output of the op amp goes high and forward biases the diode D_1. The capacitor C_1 is charged to V_{IN}. When the input becomes less than the current capacitor voltage, the output of the op amp A1 goes low and the diode D_1 is reverse biased. This isolates the C_1 and leaves it with the charge equivalent to the peak of the input voltage. The follower prevents unintentional discharging of C_1 by loading from the following circuit.

R_5 and C_1 are properly selected so that the capacitor is charged rapidly to V_{IN}. During the holding period, the capacitor slowly discharge through C_1, via leakage of the capacitor and the reverse-biased diode, or op amp bias currents. In any cases the discharging time constant is much larger than the charge time constant. And the capacitor can hold its voltage long enough to minimize the output ripple.

Resistors R_2 and R_3 limit the current into the inverting input of A1 and the non-inverting input of A2 when power is disconnected from the circuit. The discharging current from C_1 during power off may damage the input circuitry of the op amps.

The peak detector can be reset by applying a positive pulse to the reset transistor. The charge on the capacitor is dumped into ground, and the detector is ready for another cycle.

The maximum input voltage to this detector should be less than (V^+ - V_D), where V_D is the forward voltage drop of the diode. Otherwise, the input voltage should be scaled down before applying to the circuit.

HIGH SIDE CURRENT SENSING

The high side current sensing circuit (Figure 9) is commonly used in a battery charger to monitor charging current to prevent over-charging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV710/LMV711/LMV715 are ideal for this application because its common mode input range can go beyond the positive rail.

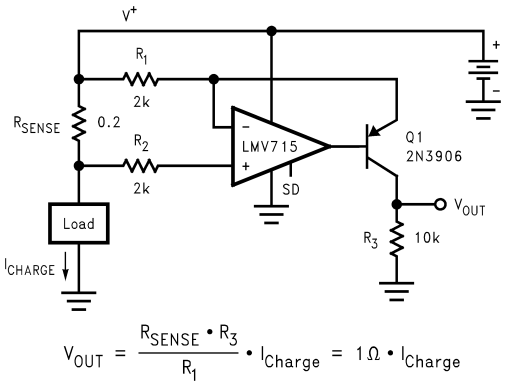


Figure 9. High Side Current Sensing

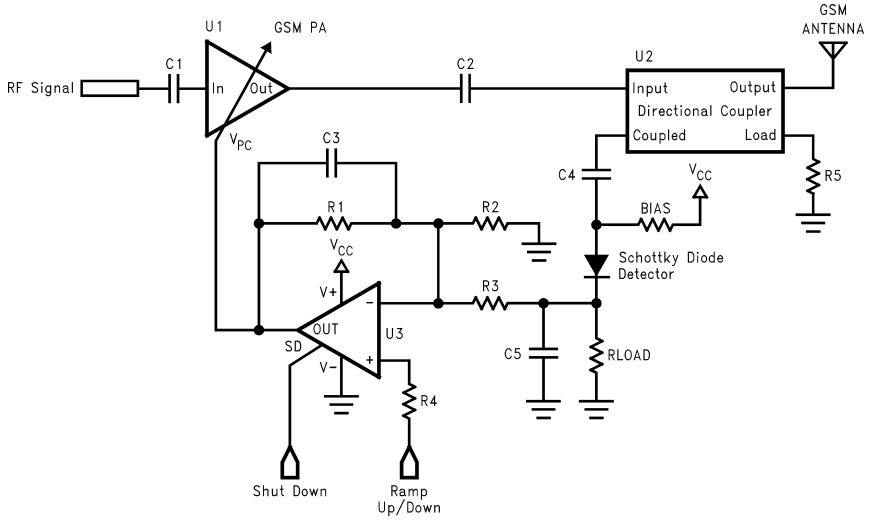


Figure 10. Typical of GSM P.A. Control Loop

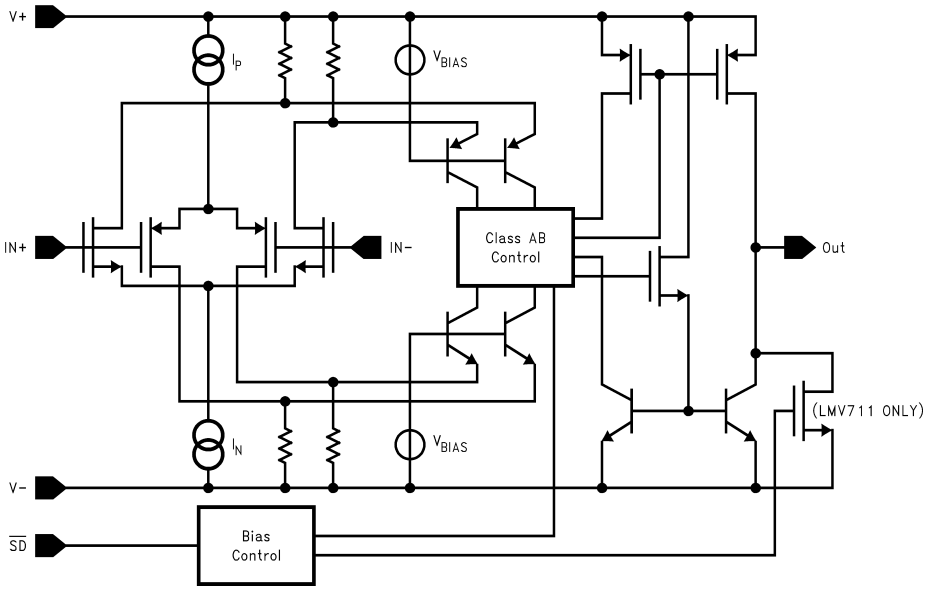
GSM POWER AMPLIFIER CONTROL LOOP

There are four critical sections in the GSM Power Amplifier Control Loop. The class-C R_F power amplifier provides amplification of the R_F signal. A directional coupler couples small amount of R_F energy from the output of the R_F P. A. to an envelope detector diode. The detector diode senses the signal level and rectifies it to a DC level to indicate the signal strength at the antenna. An op amp is used as an error amplifier to process the diode voltage and ramping voltage. This loop control the power amplifier gain via the op amp and forces the detector diode voltage and ramping voltage to be equal. Power control is accomplished by changing the ramping voltage.

The LMV710/LMV711/LMV715 are well suited as an error amplifier in this application. The LMV711/LMV715 have an extra shutdown pin to switch the op amp to shutdown mode. In shutdown mode, the LMV711/LMV715 consume very low current. The LMV711 provides a ground voltage to the power amplifier control pin V_{PC}. Therefore, the power amplifier can be turned off to save battery life. The LMV715 output will be “tri-stated” when in shutdown.

Simplified Schematic

Figure 11. LMV711



Connection Diagram

5-Pin SOT23
LMV710

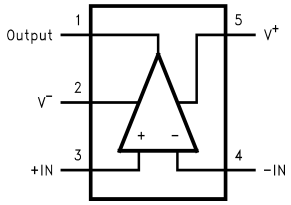


Figure 12. Top View

6-Pin SOT23
LMV711 and LMV715

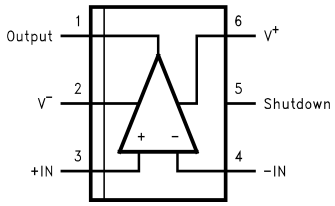


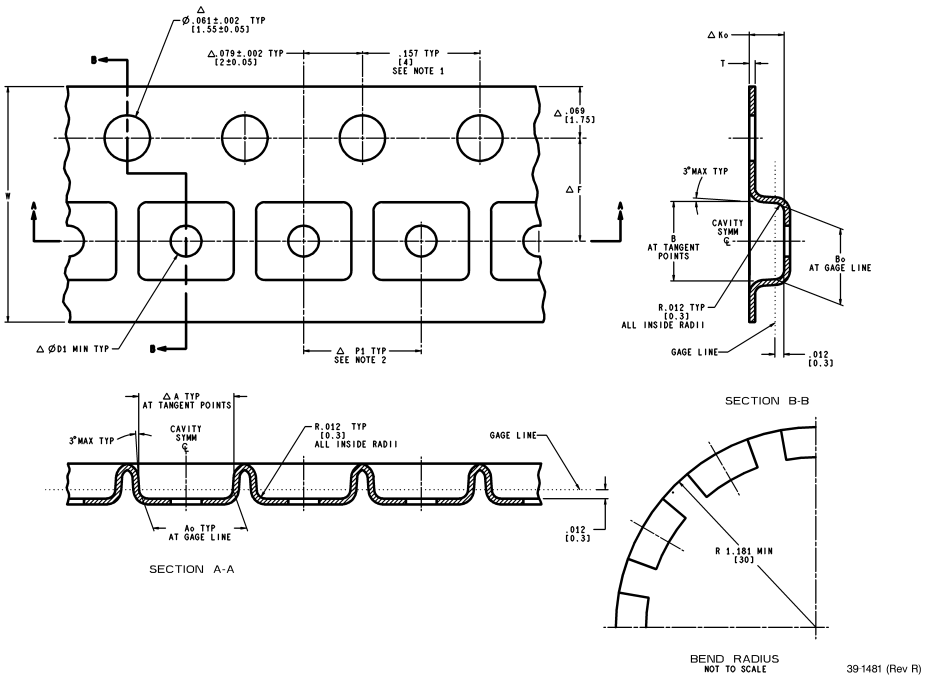
Figure 13. Top View

SOT-23 Tape and Reel Specification

Table 1. Tape Format

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	1000	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

Tape Dimensions



TAPE SIZE	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM T	DIM W
8 mm	.130 (3.3)	.124 (3.15)	.130 (3.3)	.126 (3.2)	.138 ± .002 (3.5 ± 0.05)	.055 ± .004 (1.4 ± 0.1)	.157 (4)	.008 ± .004 (0.2 ± 0.1)	.315 ± .012 (8 ± 0.3)

NOTE

UNLESS OTHERWISE SPECIFIED

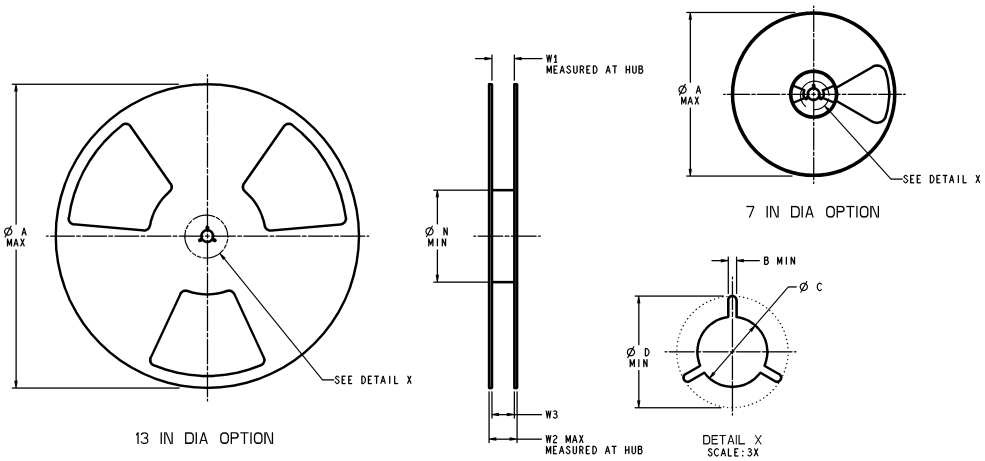
1. CUMULATIVE PITCH TOLERANCE FOR FEEDING HOLES AND CAVITIES (CHIP POCKETS) NOT TO EXCEED .008 IN / 0.2mm OVER 10 PITCH SPAN.

2. THRU HOLE INSIDE CAVITY IS CENTERED WITHIN CAVITY.

3. SMALLEST ALLOWABLE TAPE BENDING RADIUS: 1.181 IN/ 30mm.

4. DIMENSIONS WITH Δ ARE CRITICAL. DIMENSIONS TO BE ABSOLUTELY INSPECTED.

Reel Dimensions



TAPE SIZE	DIM A	DIM B	DIM C	DIM D	DIM N	DIM W1	DIM W2	DIM W3 (LSL-USL)
8 mm	7.00 (177.8)	.059 (1.5)	.512 + .020/−.008 (13 +0.5/−0.2)	.795 (20.2)	2.165 (55)	.331 + .059/−.000 (8.4 + 1.5/0)	.567 (14.4)	.311 - .429 (7.9 - 10.9)

NOTE

UNLESS OTHERWISE SPECIFIED

1. MATERIAL:

   POLYSTYRENE/PVC (WITH ANTISTATIC COATING).

   OR POLYSTYRENE/PVC, ANTISTATIC

   OR POLYSTYRENE/PVC, CONDUCTIVE.

2. CONTROLLING DIMENSION IS MILLIMETER, DIMENSIONS IN INCHES ROUNDED.

3. SURFACE RESISTIVITY: 10^{10} OHM/SQ MAXIMUM.

4. ALL OUTPUT REELS SHALL BE UNIFORM IN SHADE.

5. PACKING OF REELS IN CONTAINERS MUST ENSURE NO DAMAGE TO THE REEL.

6. SURFACE FINISH OF THE FLANGES SHALL BE SMOOTH, MATTE FINISH PREFERRED.

7. ALL EDGES, ESPECIALLY THE TAPE ENTRY EDGES, MUST BE FREE OF BURRS.

8. THE REEL SHOULD NOT WARP IN THE STORAGE TEMPERATURE OF 67°C MAXIMUM.

9. GLASS TRANSITION TEMPERATURE (T_g) OF THE PLASTIC REEL SHALL BE LOWER THAN −20°C.

10. ALL GATING FROM THE MOLD MUST BE PROPERLY REMOVED.

11. NO FLASHES ARE TO BE PRESENT ALONG THE PARTING LINES.

12. ALLOWABLE RADIUS FOR CORNERS AND EDGES IS .012 INCHES/0.3 MILLIMETERS MINIMUM.

13. SINK MARKS THAT WILL CAUSE A CHANGE TO THE SPECIFIED DIMENSIONS OR SHAPE OF THE REELS ARE NOT ALLOWED.

14. MOLDED REELS SHALL BE FREE OF COSMETIC DEFECTS SUCH AS VOIDS. FLASHING, EXCESSIVE FLOW MARKS, ETC.

15. THERE MUST BE NO MISMATCH BETWEEN MATING PARTS.

16. MOLDED REELS SHALL BE ANTISTATIC COATED OR BLENDED.

17. THE SOT23-5L AND SOT23-6L PACKAGE USE THE 7-INCH REEL.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV710M5	ACTIVE	SOT-23	DBV	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A48A	Samples
LMV710M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A48A	Samples
LMV710M5X	ACTIVE	SOT-23	DBV	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A48A	Samples
LMV710M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A48A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

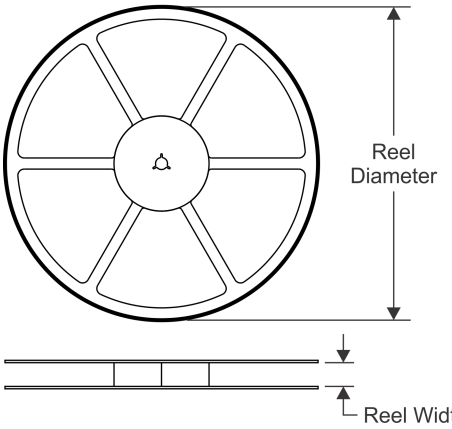
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

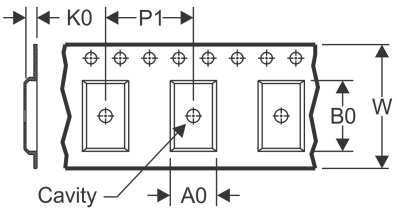
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

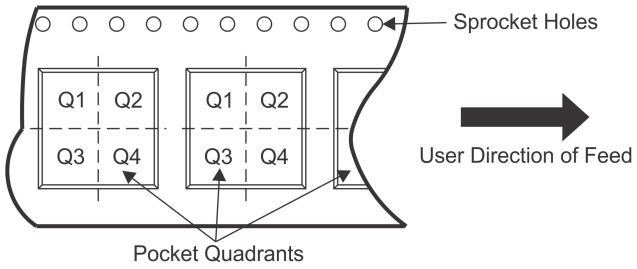


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

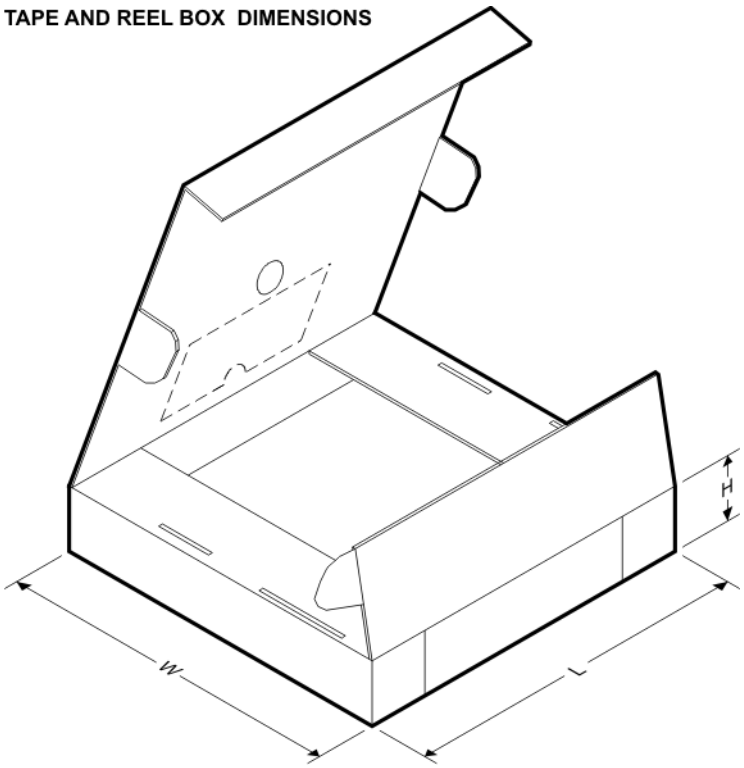
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV710M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV710M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV710M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV710M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

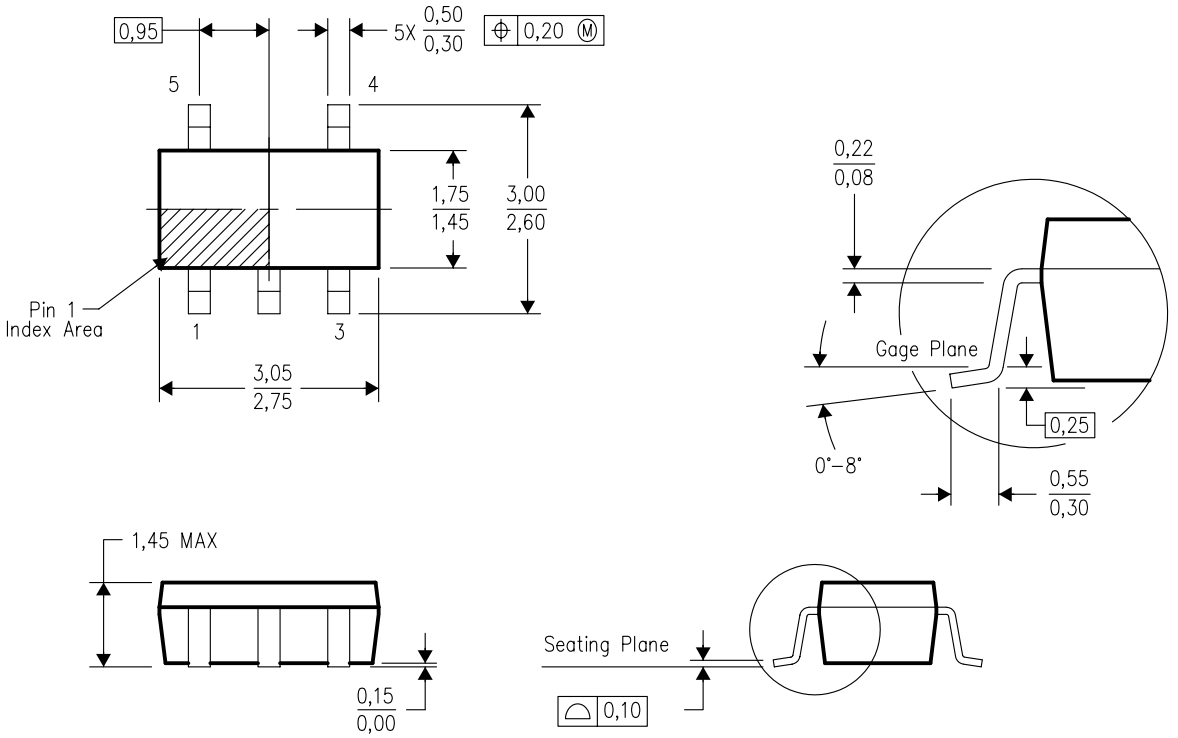
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV710M5	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV710M5/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV710M5X	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV710M5X/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0

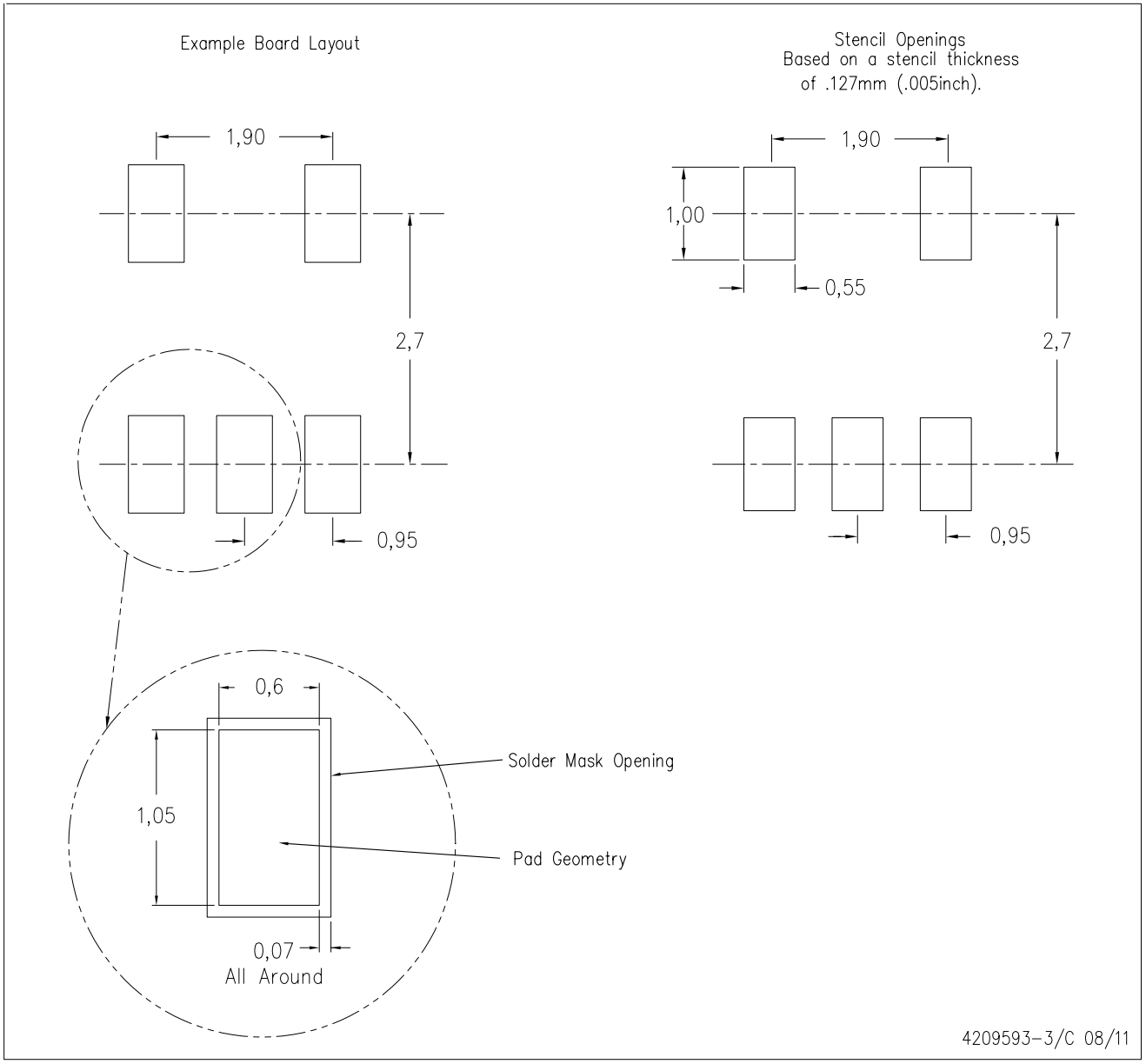
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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