LMV7219 7 nsec, 2.7V to 5V Comparator with Rail-to-Rail Output

Check for Samples: LMV7219

FEATURES

- **(V_S = 5V, T_A = 25°C, Typical values unless specified)**
- **Propagation delay 7ns**
- **Low supply current 1.1mA**
- **Input common mode voltage range extends 200mv below ground**
- **Ideal for 2.7V and 5V single supply applications**
- **Internal hysteresis ensures clean switching**
- **Fast rise and fall time 1.3ns**
- **Available in space-saving packages: 5-pin SC70-5 and SOT23-5**

APPLICATIONS

- **Portable and battery-powered systems**
- **Scanners**
- **Set top boxes**
- **High speed differential line receiver**
- **Window comparators**
- **Zero-crossing detectors**
- **High-speed sampling circuits**

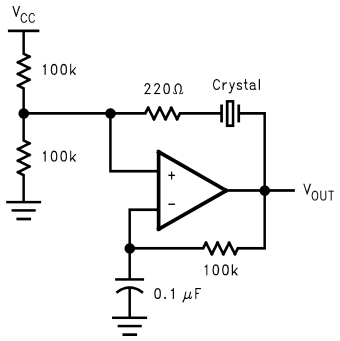
DESCRIPTION

The LMV7219 is a low-power, high-speed comparator with internal hysteresis. The LMV7219 operating voltage ranges from 2.7V to 5V with push/pull rail-to-rail output. This device achieves a 7ns propagation delay while consuming only 1.1mA of supply current at 5V.

The LMV7219 inputs have a common mode voltage range that extends 200mV below ground, allowing ground sensing. The internal hysteresis ensures clean output transitions even with slow-moving inputs signals.

The LMV7219 is available in the SC70-5 and SOT23-5 packages, which are ideal for systems where small size and low power are critical.

Typical Application



Connection Diagram

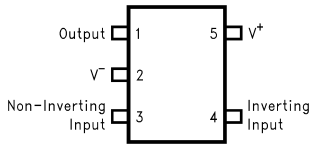
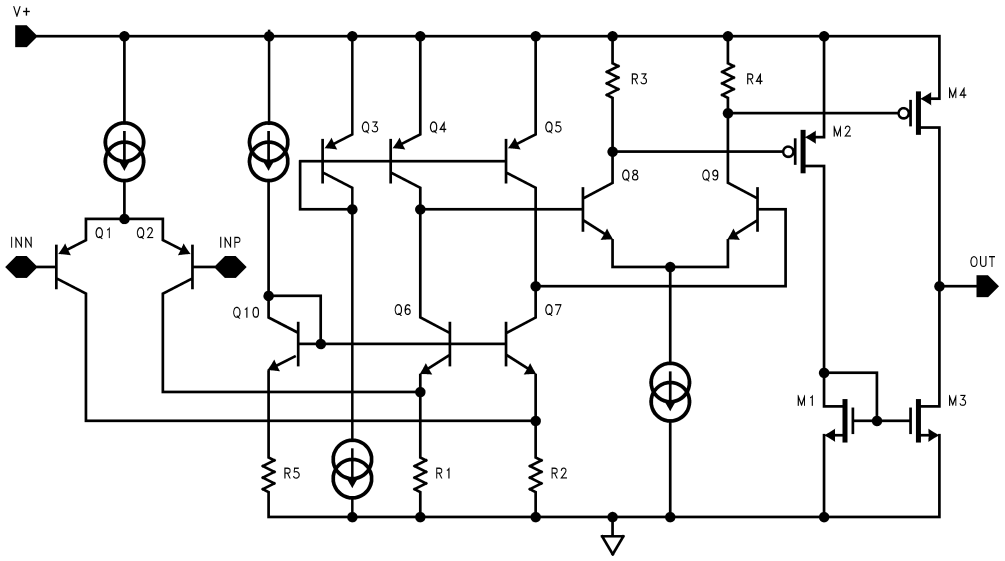


Figure 1. SC70-5/SOT23-5 (Top View)

Simplified Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)		
	Machine Body	150V
	Human Model Body	2000V
Differential Input Voltage		± Supply Voltage
Output Short Circuit Duration		(3)
Supply Voltage (V^+ - V^-)		5.5V
Soldering Information		
Infrared or Convection (20 sec)		235°C
Wave Soldering (10 sec)		260°C (lead temp)
Voltage at Input/Output pins		(V^+) + 0.4V (V^-) − 0.4V
Current at Input Pin (4)		±10mA
Maximum Junction Temperature		150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.
(2) Human body model, 1.5 kΩ in series with 100 pF. Machine model, 200Ω in series with 100 pF.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(4) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Operating Ratings

Supply voltages (V^+ - V^-)	2.7V to 5V
Operating Temperature Range (1)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Thermal Resistance	
SC70-5	478°C/W
SOT23-5	265°C/W

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_{CM} = V^+/2, V^+ = 2.7V, V^- = 0V, C_L = 10 pF and R_L > 1 MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage		1	6 **8**	mV max
I_B	Input Bias Current		450	950 **2000**	nA max
I_{OS}	Input Offset Current		50	200 **400**	nA max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 1.50V	85	62 **55**	dB min
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	85	65 **55**	dB min
V_{CM}	Input Common-Voltage Range	CMRR > 50 dB	V_{CC} −1	V_{CC} −1.2 **V_{CC} −1.3**	V min
			−0.2	−0.1 **0**	V max
V_O	Output Swing High	I_L = 4 mA, V_{ID} = 500 mV	V_{CC} −0.22	V_{CC} −0.3 **V_{CC} −0.4**	V min
		I_L = 0.4 mA, V_{ID} = 500 mV	V_{CC} −0.02	V_{CC} −0.05 **V_{CC} −0.15**	
	Output Swing Low	I_L = −4 mA, V_{ID} = −500 mV	130	200 **300**	mV max
		I_L = −0.4 mA, V_{ID} = −500 mV	15	50 **150**	
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (3)	20		mA
		Sinking, V_O = 2.7V (3)	20		
I_S	Supply Current	No Load	0.9	1.6 **2.2**	mA max
V_{HYST}	Input Hysteresis Voltage	(4)	7		mV
V_{TRIP^+}	Input Referred Positive Trip Point	(see Figure 2)	3	8	mV max
V_{TRIP^-}	Input Referred Negative Trip Point	(see Figure 2)	−4	−8	mV min
t_{PD}	Propagation Delay	Overdrive = 5 mV V_{CM} = 0V (5)	12		ns max
		Overdrive = 15 mV V_{CM} = 0V (5)	11		
		Overdrive = 50 mV V_{CM} = 0V (5)	10	20	
t_{SKEW}	Propagation Delay Skew	(6)	1		ns
t_r	Output Rise Time	10% to 90%	2.5		ns
t_f	Output Fall Time	90% to 10%	2		ns

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(4) The LMV7219 comparator has internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{trip^+} and V_{trip^-}, while the hysteresis voltage is the difference of these two.
(5) Propagation delay measurements made with 100 mV steps. Overdrive is measure relative to V_{Trip}.
(6) Propagation Delay Skew is defined as absolute value of the difference between t_{PDLH} and t_{PDHL}.

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_{CM} = V^+/2, V^+ = 5V, V^- = 0V, C_L = 10 pF and R_L > 1 MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage		1	6 **8**	mV max
I_B	Input Bias Current		500	950 **2000**	nA max
I_{OS}	Input Offset Current		50	200 **400**	nA max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 3.8V	85	65 **55**	dB min
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	85	65 **55**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50 dB	V_{CC} −1	V_{CC} −1.2 V_{CC} −1.3	V min
			−0.2	−0.1 0	V max
V_O	Output Swing High	I_L = 4 mA, V_{ID} = 500 mV	V_{CC} −0.13	V_{CC} −0.2 V_{CC} −0.3	V min
		I_L = 0.4 mA, V_{ID} = 500 mV	V_{CC} −0.02	V_{CC} −0.05 V_{CC} −0.15	
	Output Swing Low	I_L = −4 mA, V_{ID} = −500 mV	80	180 **280**	mV max
		I_L = −0.4 mA, V_{ID} = −500 mV	10	50 **150**	
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (3)	68	30 **20**	mA min
		Sinking, V_O = 5V (3)	65	30 **20**	
I_S	Supply Current	No Load	1.1	1.8 **2.4**	mA max
V_{HYST}	Input Hysteresis Voltage	(4)	7.5		mV
V_{Trip^+}	Input Referred Positive Trip Point	(See figure 1)	3.5	8	mV max
V_{Trip^-}	Input Referred Negative Trip Point	(See figure 1)	−4	−8	mV min
t_{PD}	Propagation Delay	Overdrive = 5 mV V_{CM} = 0V (5)	9		ns max
		Overdrive = 15mV V_{CM} = 0V (5)	8	20	
		Overdrive = 50 mV V_{CM} = 0V (5)	7	19	
t_{SKEW}	Propagation Delay Skew	(6)	0.4		ns
t_r	Output Rise Time	10% to 90%	1.3		ns
t_f	Output Fall Time	90% to 10%	1.25		ns

(1) Typical Values represent the most likely parametric norm.
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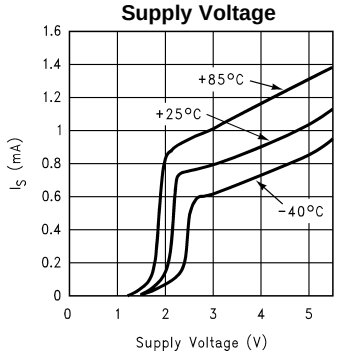
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(4) The LMV7219 comparator has internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{trip^+} and V_{trip^-}, while the hysteresis voltage is the difference of these two.
(5) Propagation delay measurements made with 100 mV steps. Overdrive is measure relative to V_{Trip}.
(6) Propagation Delay Skew is defined as absolute value of the difference between t_{PDLH} and t_{PDHL}.

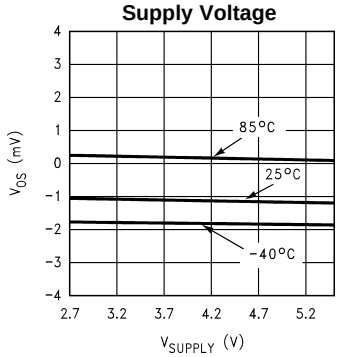
Typical Performance Characteristics

Unless otherwise specified, V_S = 5V, C_L = 10 pF, T_A = 25°C

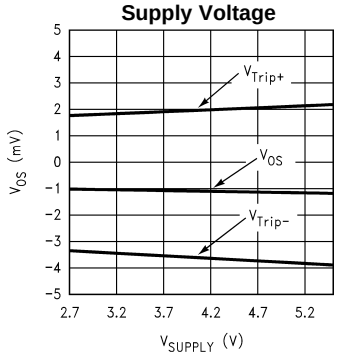
Supply Current vs. Supply Voltage



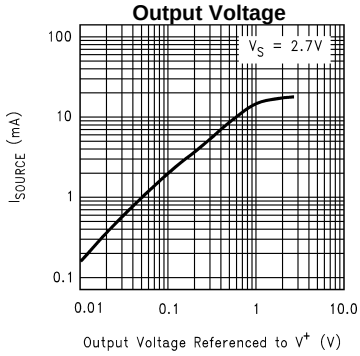
V_{OS} vs. Supply Voltage



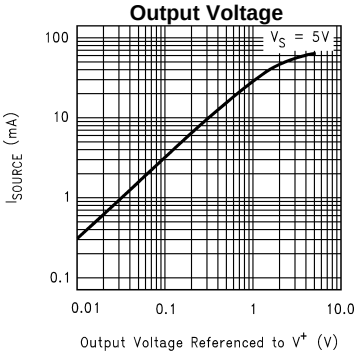
Input Offset and Trip Voltage vs. Supply Voltage



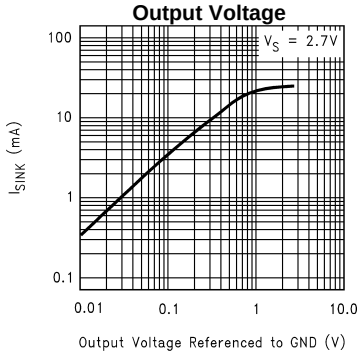
Sourcing Current vs. Output Voltage



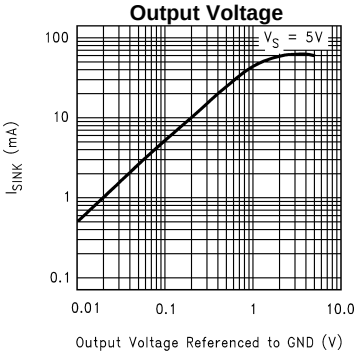
Sourcing Current vs. Output Voltage



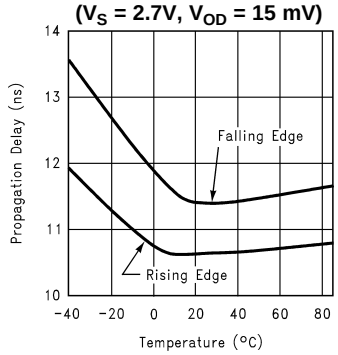
Sinking Current vs. Output Voltage



Sinking Current vs. Output Voltage



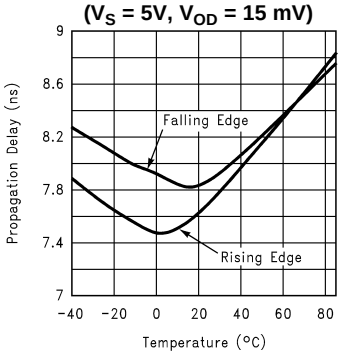
Propagation Delay vs. Temperature (V_S = 2.7V, V_{OD} = 15 mV)



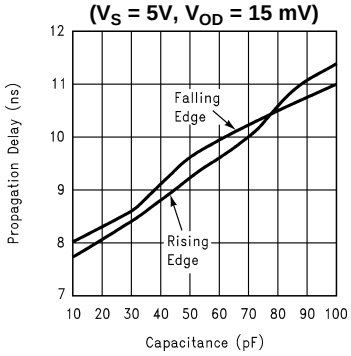
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = 5V, C_L = 10 pF, T_A = 25°C

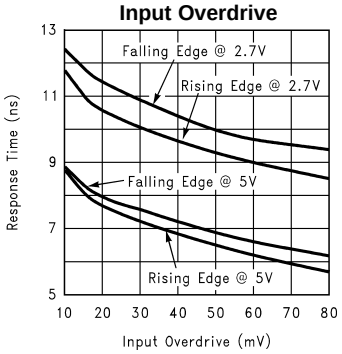
Propagation Delay vs. Temperature (V_S = 5V, V_{OD} = 15 mV)



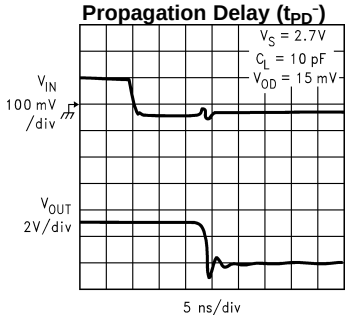
Propagation Delay vs. Capacitive Load (V_S = 5V, V_{OD} = 15 mV)



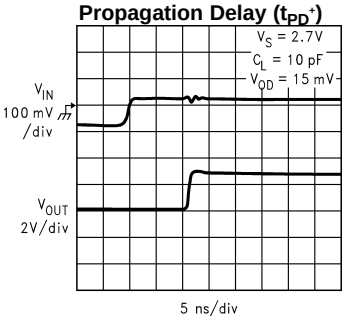
Propagation Delay vs. Input Overdrive



Propagation Delay (t_{PD}^-)



Propagation Delay (t_{PD}^+)



Application Section

LMV7219 is a single supply comparator with internal hysteresis, 7ns of propagation delay and only 1.1mA of supply current.

The LMV7219 has a typical input common mode voltage range of −0.2V below the ground to 1V below V_{CC}. The differential input stage is a pair of PNP transistors, therefore, the input bias current flows out of the device. If either of the input signals falls below the negative common mode limit, the parasitic PN junction formed by the substrate and the base of the PNP will turn on, resulting in an increase of input bias current.

If one of the inputs goes above the positive common mode limit, the output will still maintain the correct logic level as long as the other input stays within the common mode range. However, the propagation delay will increase. When both inputs are outside the common mode voltage range, current saturation occurs in the input stage, and the output becomes unpredictable.

The propagation delay does not increase significantly with large differential input voltages. However, large differential voltages greater than the supply voltage should be avoided to prevent damages to the input stage.

The LMV7219 has a push pull output. When the output switches, there is a direct path between V_{CC} and ground, causing high output sinking or sourcing current during the transition. After the transition, the output current decreases and the supply current settles back to about 1.1mA at 5V, thus conserving power consumption.

Most high-speed comparators oscillate when the voltage of one of the inputs is close to or equal to the voltage on the other input due to noise or undesirable feedback. The LMV7219 have 7mV of internal hysteresis to counter parasitic effects and noise. The hysteresis does not change significantly with the supply voltages and the common mode input voltages as reflected in the specification table.

The internal hysteresis creates two trip points, one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. With internal hysteresis, when the comparator's input voltages are equal, the hysteresis effectively causes one comparator-input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The fixed internal hysteresis eliminates these resistors.

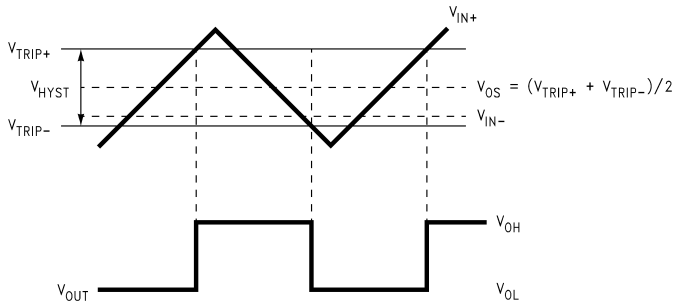


Figure 2. Input and Output Waveforms, Non-Inverting Input Varied

Additional Hysteresis

If additional hysteresis is desired, this can be done with the addition of three resistors using positive feedback, as shown in Figure 3. The positive feedback method slows the comparator response time. Calculate the resistor values as follows:

1) Select R3. The current through R3 should be greater than the input bias current to minimize errors. The current through R3 (I_F) at the trip point is (V_{REF} - V_{OUT}) /R3. Consider the two possible output states when solving for R3, and use the smaller of the two resulting resistor values. The two formulas are:

$R3 = V_{REF}/I_F$ (when $V_{OUT} = 0$)

$R3 = V_{CC} - V_{REF} /I_F$ ($V_{OUT} = V_{CC}$)

2) Choose a hysteresis band required (V_{HB}).

3) Calculate R1, where R1 = R3 X(V_{HB}/V_{CC})

4) Choose the trip point for V_{IN} rising. This is the threshold voltage (V_{THR}) at which the comparator switches from low to high as V_{IN} rises about the trip point.

5) Calculate R2 as follows:

$$R_2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R_1}\right) - \frac{1}{R_1} - \frac{1}{R_3}} \quad (1)$$

6) Verify the trip voltage and hysteresis as follows:

$$V_{IN} \text{ rising: } V_{THR} = V_{REF} \times R_1 \times \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)$$

$$V_{IN} \text{ falling: } V_{THF} = V_{THR} - \left(\frac{R_1 \times V_{CC}}{R_3}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF} \quad (2)$$

This method is recommended for additional hysteresis of up to a few hundred millivolts. Beyond that, the impedance of R3 is low enough to affect the bias string and adjustment of R1 may be also required.

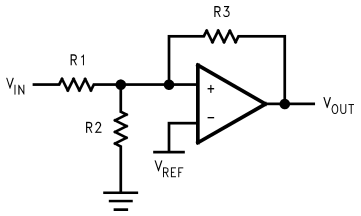


Figure 3. Additional Hysteresis

Circuit Layout and Bypassing

The LMV7219 requires high-speed layout. Follow these layout guidelines:

1. Power supply bypassing is critical, and will improve stability and transient response. A decoupling capacitor such as 0.1µF ceramic should be placed as close as possible to V^+ pin. An additional 2.2µF tantalum capacitor may be required for extra noise reduction.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize unwanted parasitic feedback around the comparator.
3. The device should be soldered directly to the PC board instead of using a socket.
4. Use a PC board with a good, unbroken low inductance ground plane. Make sure ground paths are low-impedance, especially were heavier currents are flowing.
5. Input traces should be kept away from output traces. This can be achieved by running a topside ground plane between the output and inputs.
6. Run the ground trace under the device up to the bypass capacitor to shield the inputs from the outputs.
7. To prevent parasitic feedback when input signals are slow-moving, a small capacitor of 1000pF or less can be placed between the inputs. It can also help eliminate oscillations in the transition region. However, this capacitor can cause some degradation to tpd when the source impedance is low.

Zero-Crossing Detector

The inverting input is connected to ground and the non-inverting input is connected to 100mVp-p signal. As the signal at the non-inverting input crosses 0V, the comparator's output Changes State.

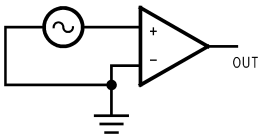


Figure 4. Zero-Crossing Detector

Threshold Detector

Instead of tying the inverting input to 0V, the inverting input can be tied to a reference voltage. The non-inverting input is connected to the input. As the input passes the V_{REF} threshold, the comparator's output changes state.

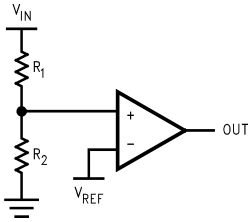


Figure 5. Threshold Detector

Crystal Oscillator

A simple crystal oscillator using the LMV7219 is shown below. Resistors R1 and R2 set the bias point at the comparator's non-inverting input. Resistors R3, R4 and C1 sets the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator offset.

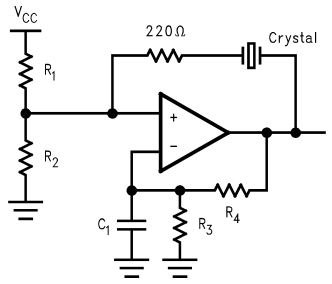


Figure 6. Crystal Oscillator

IR Receiver

The LMV7219 is an ideal candidate to be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across RD. When this voltage level cross the voltage applied by the voltage divider to the inverting input, the output transitions.

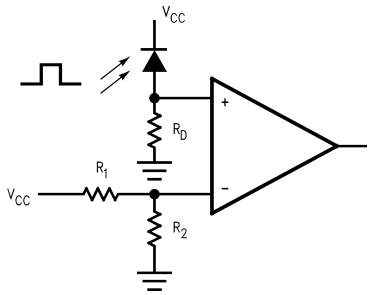


Figure 7. IR Receiver

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV7219M5	ACTIVE	SOT-23	DBV	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	C14A	Samples
LMV7219M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C14A	Samples
LMV7219M5X	ACTIVE	SOT-23	DBV	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	C14A	Samples
LMV7219M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C14A	Samples
LMV7219M7	ACTIVE	SC70	DCK	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	C15	Samples
LMV7219M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C15	Samples
LMV7219M7X	ACTIVE	SC70	DCK	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	C15	Samples
LMV7219M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C15	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

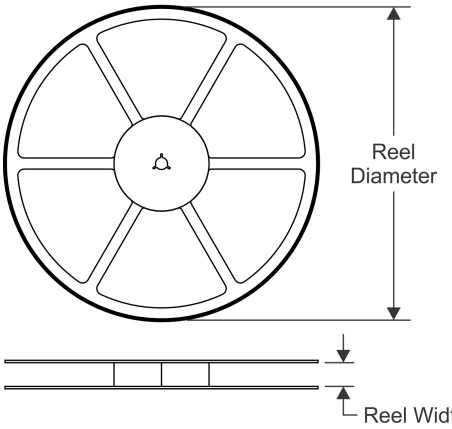
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

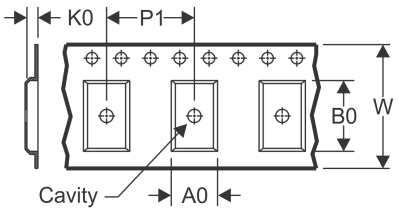
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

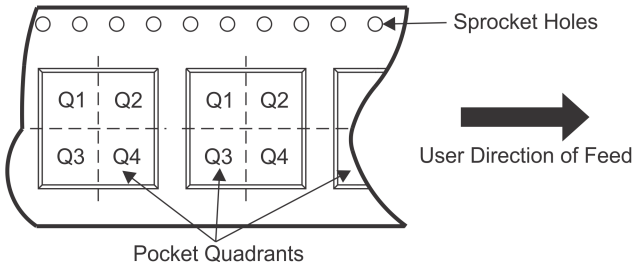


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

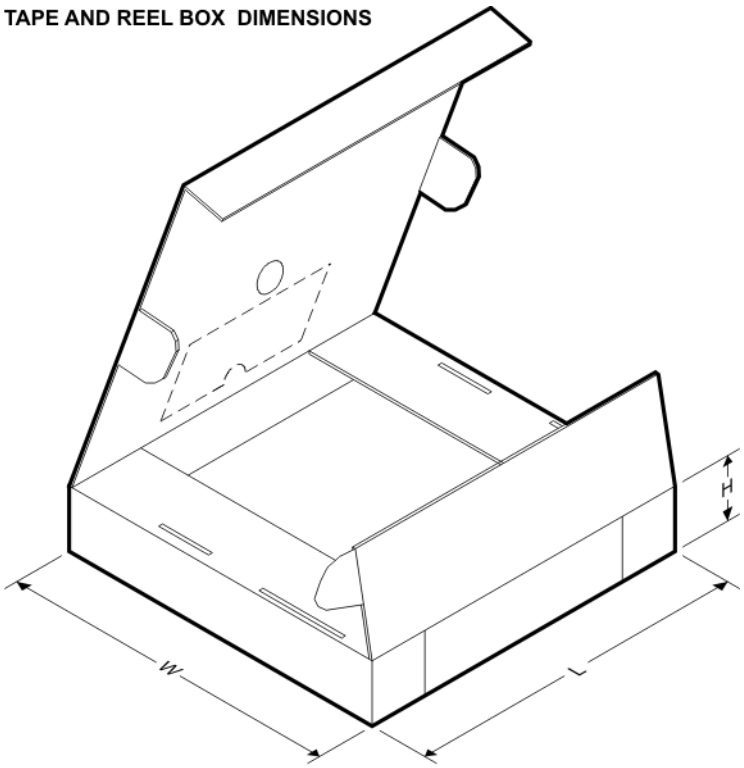
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7219M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7219M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7219M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7219M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

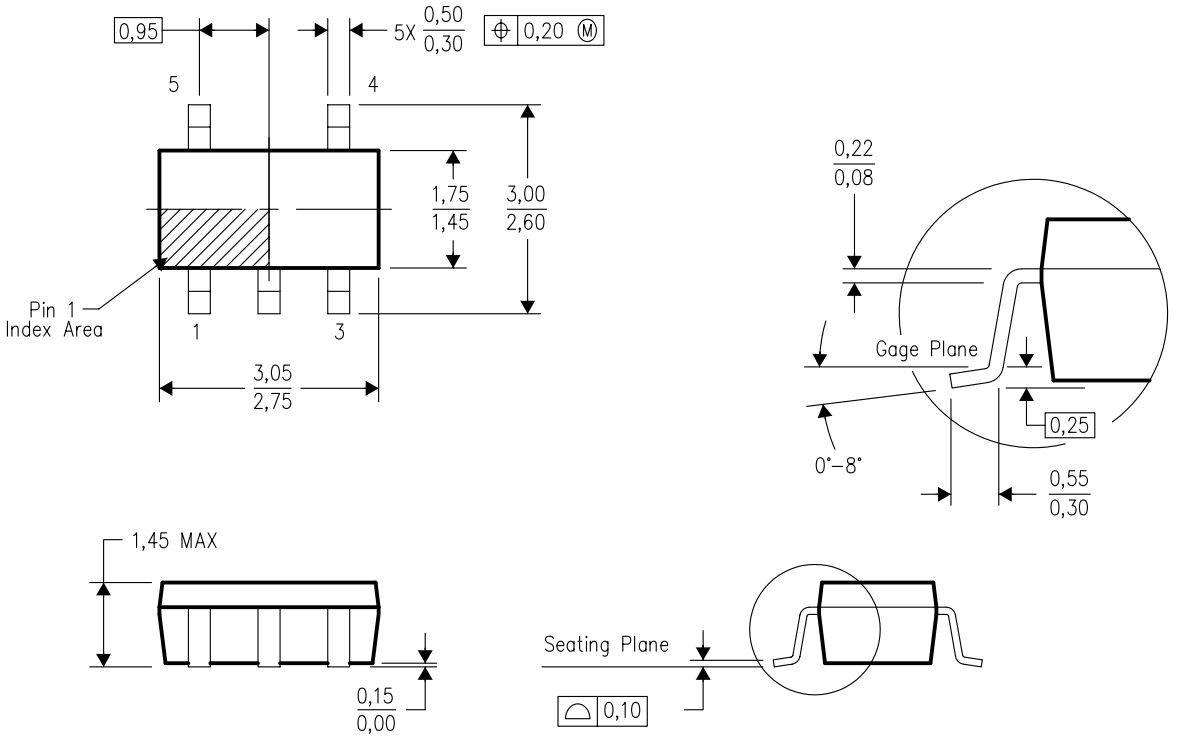
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7219M5	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV7219M5/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV7219M5X	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV7219M5X/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV7219M7	SC70	DCK	5	1000	203.0	190.0	41.0
LMV7219M7/NOPB	SC70	DCK	5	1000	203.0	190.0	41.0
LMV7219M7X	SC70	DCK	5	3000	206.0	191.0	90.0
LMV7219M7X/NOPB	SC70	DCK	5	3000	206.0	191.0	90.0

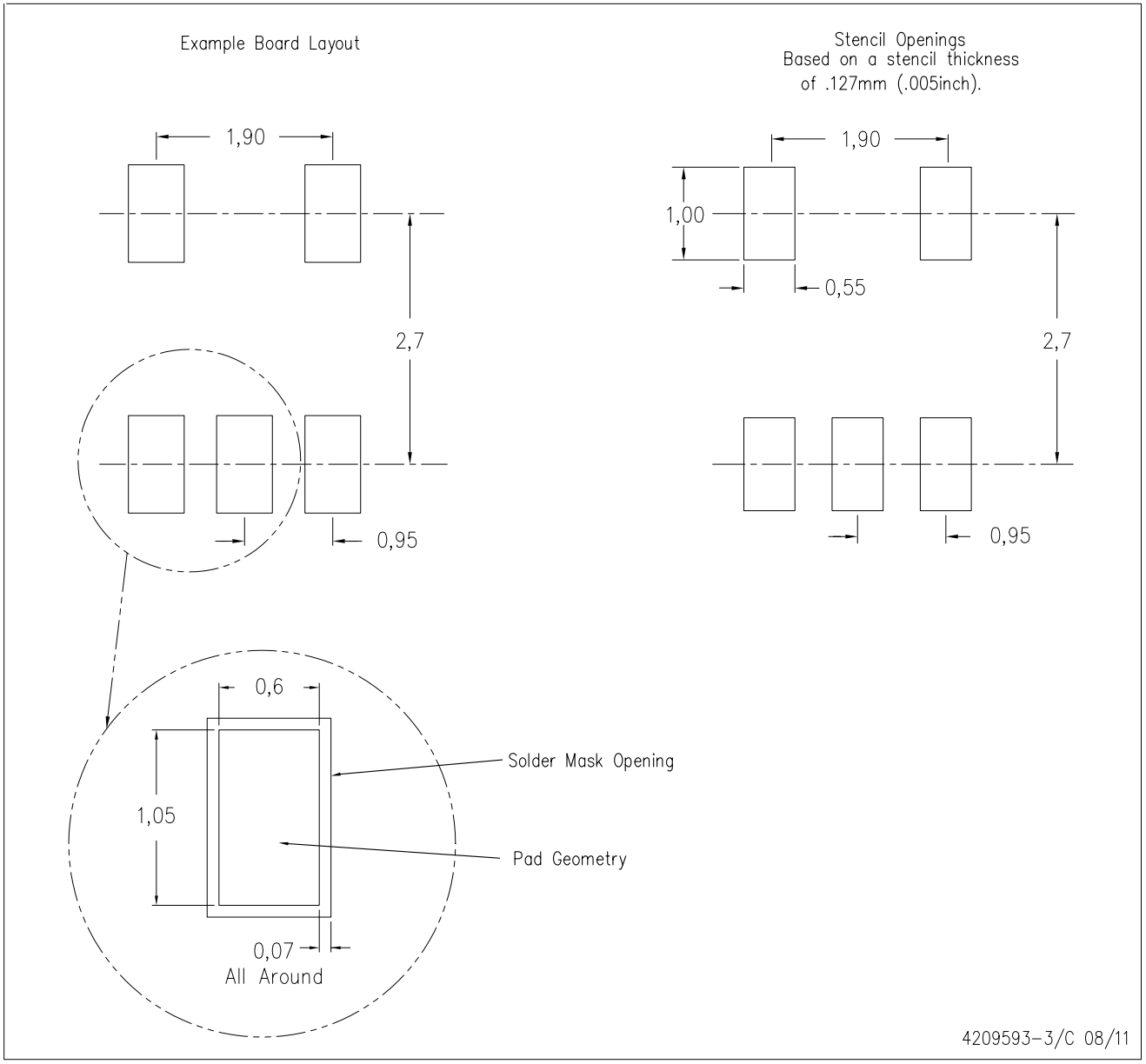
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

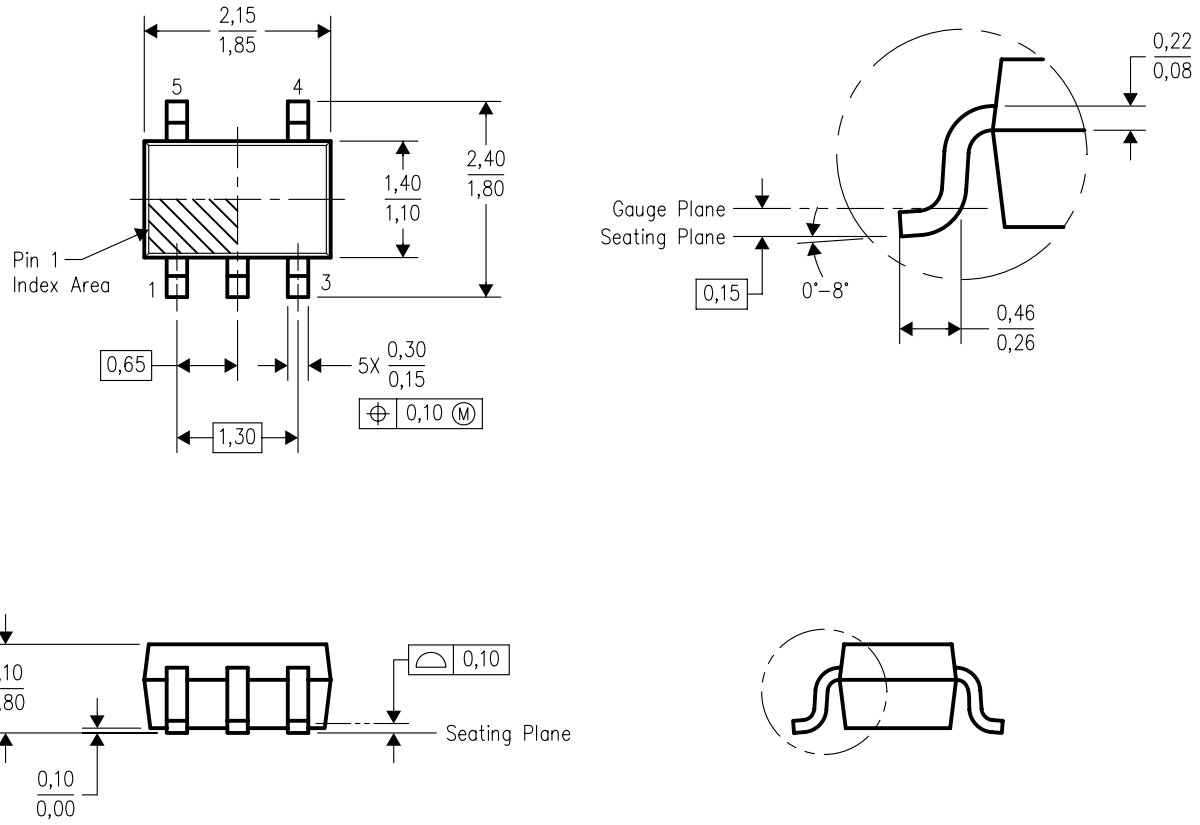
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

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