LMX3161

LMX3161 Single Chip Radio Transceiver

Literature Number: SNOS871

National Semiconductor

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Single Chip Radio Transceiver

General Description

The LMX3161 Single Chip Radio Transceiver is a monolithic, integrated radio transceiver optimized for use in a Digital Enhanced Cordless Telecommunications (DECT) system. It is fabricated using National's ABiC V BiCMOS process (f_T = 18 GHz).

The LMX3161 contains phase locked loop (PLL), transmit and receive functions. The 1.1 GHz PLL block is shared between transmit and receive section. The transmitter includes a frequency doubler, and a high frequency buffer. The receiver consists of a 2.0 GHz low noise mixer, an intermediate frequency (IF) amplifier, a high gain limiting amplifier, a frequency discriminator, a received signal strength indicator (RSSI), and an analog DC compensation loop. The PLL, doubler, and buffers can be used to implement open loop modulation along with an external VCO and loop filter. The circuit features on-chip voltage regulation to allow supply voltages ranging from 3.0V to 5.5V. Two additional voltage regulators provide a stable supply source to external discrete stages in the Tx and Rx chains.

The IF amplifier, high gain limiting amplifier, and discriminator are optimized for 110 MHz operation, with a total IF gain of 85 dB. The single conversion receiver architecture provides a low cost, high performance solution for communications systems. The RSSI output may be used for channel quality monitoring.

The Single Chip Radio Transceiver is available in a 48-pin 7mm X 7mm X 1.4mm PQFP surface mount plastic package.

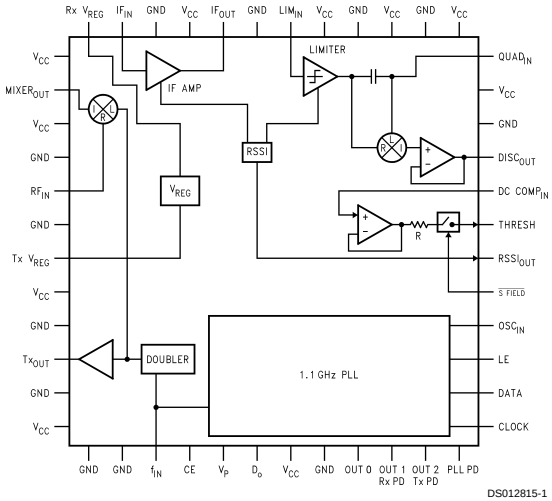
Features

- Single chip solution for DECT RF transceiver
- RF sensitivity to −93 dBm; RSSI sensitivity to −100 dBm
- Two regulated voltage outputs for discrete amplifiers
- High gain (85 dB) intermediate frequency strip
- Allows unregulated 3.0V–5.5V supply voltage
- Power down mode for increased current savings
- System noise figure 6.5 dB (typ)

Applications

- Digital Enhanced Cordless Telecommunications (DECT)
- Personal wireless communications (PCS/PCN)
- Wireless local area networks (WLANs)
- Other wireless communications systems

Block Diagram



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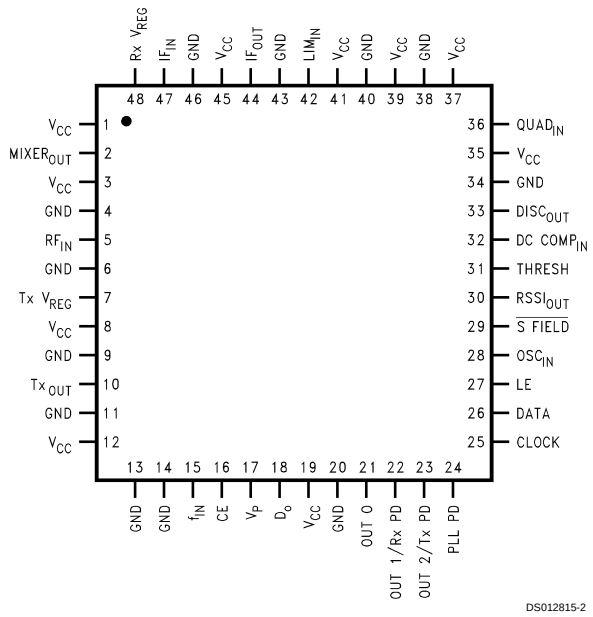
LMX3161 Pin Diagram



Top View
Order Number LMX3161VBH or LMX3161VBHX
See NS Package Number VBH48A

LMX3161 Pin Diagram (Continued)

Pin No.	Pin Name	I/O	Description
1	V_{CC}	—	Power supply for CMOS section of PLL and ESD bussing.
2	$MIXER_{OUT}$	O	IF output from the mixer.
3	V_{CC}	—	Power supply for mixer section.
4	GND	—	Ground.
5	RF_{IN}	I	RF input to the mixer.
6	GND	—	Ground.
7	Tx V_{REG}	—	Regulated power supply for external PA gain stage.
8	V_{CC}	—	Power supply for analog sections of PLL and doubler.
9	GND	—	Ground.
10	Tx_{OUT}	O	Frequency doubler output.
11	GND	—	Ground.
12	V_{CC}	—	Power supply for analog sections of PLL and doubler.
13	GND	—	Ground.
14	GND	—	Ground.
15	f_{IN}	I	RF Input to PLL and frequency doubler.
16	CE	I	Chip Enable. Pulling LOW powers down entire chip. Taking CE HIGH powers up the appropriate functional blocks depending on the state of bits F6, F7, F11, and F12 programmed in F-latch. It is necessary to initialize the internal registers once, after the power up reset. The registers' contents are kept even in power-down condition.
17	V_P	—	Power supply for charge pump.
18	D_o	O	Charge pump output. For connection to a loop filter for driving the input of an external VCO.
19	V_{CC}	—	Power supply for CMOS section of PLL and ESD bussing.
20	GND	—	Ground.
21	OUT 0	O	Programmable CMOS output. Refer to Function Register Programming Description section for details.
22	Rx PD/OUT 1	I/O	Receiver power down control input or programmable CMOS output. Refer to Function Register Programming Description section for details.
23	Tx PD/OUT 2	I/O	Transmitter power down control input or programmable CMOS output. Refer to Function Register Programming Description section for details.
24	PLL PD	I	PLL power down control input. LOW for PLL normal operations, and HIGH for PLL power saving.
25	CLOCK	I	MICROWIRE™ clock input. High impedance CMOS input with Schmitt Trigger.
26	DATA	I	MICROWIRE data input. High impedance CMOS input with Schmitt Trigger.
27	LE	I	MICROWIRE load enable input. High impedance CMOS input with Schmitt Trigger.
28	OSC_{IN}	I	Oscillator input. High impedance CMOS input with feedback.
29	$\overline{S\ FIELD}$	I	DC compensation circuit enable. While LOW, the DC compensation circuit is enabled and the threshold is updated through the DC compensation loop. While HIGH, the switch is opened, and the comparator threshold is held by the external capacitor.
30	$RSSI_{OUT}$	O	Received signal strength indicator (RSSI) output.
31	THRESH	O	Threshold level to external comparator.
32	DC $COMP_{IN}$	I	Input to DC compensation circuit.
33	$DISC_{OUT}$	O	Demodulated output of discriminator.
34	GND	—	Ground.
35	V_{CC}	—	Power supply for the discriminator circuit.
36	$QUAD_{IN}$	I	Quadrature input for tank circuit.
37	V_{CC}	—	Power supply for limiter output stage.
38	GND	—	Ground.
39	V_{CC}	—	Power supply for limiter gain stages.
40	GND	—	Ground.
41	V_{CC}	—	Power supply for IF amplifier gain stages.

LMX3161 Pin Diagram (Continued)

Pin No.	Pin Name	I/O	Description
42	LIM_{IN}	I	IF input to the limiter.
43	GND	—	Ground.
44	IF_{OUT}	O	IF output from IF amplifier.
45	V_{CC}	—	Power supply for IF amplifier output.
46	GND	—	Ground.
47	IF_{IN}	I	IF input to IF amplifier.
48	Rx V_{REG}	—	Regulated power supply for external LNA stages.

Absolute Maximum Ratings (Notes 1, 2)

Power Supply Voltage (V_{CC})	−0.3V to +6.5V
V_P	−0.3V to +6.5V
Voltage on Any Pin with GND = 0V (V_I)	−0.3V to V_{CC} +0.3V
Storage Temperature Range (T_S)	−65˚C to +150˚C
Lead Temp. (solder, 4 sec)(T_L)	+260˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 5.5V
(V_P)	V_{CC} to 5.5V
Operating Temperature (T_A)	−10˚C to +70˚C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section. The guaranteed specifications apply only for the test conditions listed.

Note 2: This device is a high performance RF integrated circuit with an ESD rating < KeV and is ESD sensitive. Handling and assembly of this device should only be done at ESD work stations.

Electrical Characteristics

The following specifications are guaranteed for V_{CC} = 3.6V and T_A = 25˚C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Current Consumption					
$I_{DD, RX}$	-Open-Loop Receive Mode	PLL & TX chain powered down	—	50	60	mA
$I_{DD, TX}$	-Open-Loop Transmit Mode	PLL & RX chain powered down	—	27	37	mA
$I_{DD, PLL}$	-Closed-Loop PLL Mode	RX & TX chain powered down	—	6	8	mA
I_{PD}	-Power Down Mode		—	—	70	µA
MIXER		f_{RF} = 1.89 GHz, f_{IF} = 110 MHz, f_{LO} = 1780 MHz (f_{IN} = 890 MHz)				
f_{RF}	RF Frequency Range	(Note 3)	1.7	—	2.0	GHz
f_{IF}	IF Frequency	(Note 4)	—	110	—	MHz
Z_{IN}	Input Impedance, RF_{IN}		—	15-j5	—	Ω
Z_{OUT}	Output Impedance, Mixer Out		—	160-j70	—	Ω
NF	Noise Figure (Single Side Band)	(Notes 5, 6)	—	10	14	dB
G_C	Conversion Gain	(Note 5)	14	17	—	dB
P_{1dB}	Input 1dB Compression Point	(Note 5)	−24	−20	—	dBm
OIP3	Output 3rd Order Intercept Point	(Note 5)	—	7.5	—	dBm
F_{IN}-RF	Fin to RF Isolation	F_{IN}=890 MHz	—	−30	—	dB
		f_{IN}=1780 MHz	—	−10.6	—	dB
		f_{IN}=2670 MHz	—	−30	—	dB
F_{IN}-IF	Fin to IF Isolation	f_{IN}=890 MHz	—	−30	—	dB
		f_{IN}=1780 MHz	—	−30	—	dB
		f_{IN}=2670 MHz	—	−30	—	dB
RF–IF	RF to IF Isolation	P_{IN}=0 to −85 dB	—	−30	—	dB
IF AMPLIFIER		f_{IN} = 110 MHz				
NF	Noise Figure	(Note 7)	—	8	11	dB
A_V	Gain	(Note 7)	15	24	—	dB
Z_{IN}	Input Impedance		—	150–j120	—	Ω
Z_{OUT}	Output Impedance		—	190–j20	—	Ω
IF LIMITER		f_{IN} = 110 MHz				
Sens	Limiter/Discriminator Sensitivity	BER=10^{-3}	—	−65	—	dBm
IF_{IN}	IF Limiter Input Impedance		—	100–j300	—	Ω
DISCRIMINATOR		f_{IN} = 110 MHz				
	Disc Gain	1X Mode	—	10	—	mV/˚
	(mV/˚ of Phase Shift from Tank Circuit)	3X Mode	—	33	—	mV/˚
V_{OUT}	Discriminator Output Peak to Peak	1X Mode (Note 8)	80	160	—	mV
	Voltage	3X Mode (Note 8)	400	580	—	mV
V_{OS}	Disc. Output DC Voltage	Nominal (Note 10)	1.2		1.82	V
$DISC_{OUT}$	Disc. Output Impedance		—	300	—	Ω

Electrical Characteristics (Continued)

The following specifications are guaranteed for V_{CC} = 3.6V and T_A = 25˚C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RSSI (Note 11)		f_{IN} = 110 MHz				
$RSSI_{out}$	Output Voltage	P_{IN}=−80 dBm@IF_{IN} input pin	0.12	0.2	0.6	V
		P_{IN}=−20 dBm@IF_{IN} input pin	0.9	1.2	—	V
	Slope	P_{IN}= −90 to −30 dBm@LIM_{IN} input pin	11	18	25	mV/dB
RSSI	Dynamic Range	P_{IN} min= −90 dBm@LIM_{IN} input pin	—	60	—	dB
DC COMPENSATION CIRCUIT						
V_{OS}	Input Offset Voltage		−5	—	+5	mV
$V_{I/O}$	Input/Output Voltage Swing	Centered at 1.5V	—	1.0	—	V_{PP}
R_{SH}	Sample and Hold Resistor		2000	3000	3600	Ω
FREQUENCY SYNTHESIZER		P_{IN} = −14 to −9 dBm				
f_{IN}	Input Frequency Range	(Note 9)	500	—	1200	MHz
P_{IN}	Input Signal Level	Z_{IN}=200Ω (Note 15)	—	−11.5	—	dBm
f_{OSC}	Oscillator Frequency Range	(Note 12)	5	—	20	MHz
V_{OSC}	Oscillator Sensitivity	(Note 12)	0.5	1.0	—	V_{pp}
$I_{Do\text{-}source}$	Charge Pump Output Current	V_{do} = V_P/2, I_{cpo} = LOW (Note 14)	—	−1.5	—	mA
$I_{Do\text{-}sink}$		V_{do} = V_P/2, I_{cpo} = LOW (Note 14)	—	1.5	—	mA
$I_{Do\text{-}source}$		V_{do} = V_P/2, I_{cpo} = HIGH (Note 14)	—	−6.0	—	mA
$I_{Do\text{-}sink}$		V_{do} = V_P/2, I_{CPO} = HIGH (Note 14)	—	6.0	—	mA
$I_{Do\text{-}Tri}$		0.5 ≤ V_{do} ≤ V_p − 0.5 T_A = 25˚C	−1.0	—	1.0	nA
FREQUENCY DOUBLER		f_{IN} = 945 MHz, f_{OUT} = 1.89 GHz				
f_{OUT}	Output Frequency Range	(Note 13)	1770	—	1900	MHz
P_{OUT}	Output Signal Level	P_{IN} = −11.5 dBm, f_{OUT} = 1.89 GHz	−10	−3	—	dBm
	Fundamental Output Power	P_{IN} = −11.5 dBm, f_{OUT} = 945 MHz	—	−22	−13.5	dBm
	Harmonic Output Power	P_{IN} = −11.5 dBm, f_{OUT} = 2.835 GHz	—	−24	−15	dBm
Z_{OUT}	Output Impedance	TX chain powered up	—	25+j60	—	Ω
		TX chain powered down	—	15-j30	—	Ω
VOLTAGE REGULATOR						
V_O	Output Voltage	I_{LOAD} = 5 mA	2.55	2.75	2.90	V
DIGITAL INPUT/OUTPUT PINS						
V_{IH}	High Level Input Voltage		2.4	—	V_{CC}	V
V_{IL}	Low Level Input Voltage		0.0	—	0.8	V
I_{IH}	Input Current	GND < V_{IN} < V_{CC}	−10	—	10	µA
V_{OH}	High Level Output Voltage	I_{OH}=−0.5 mA	2.4	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL}=0.5 mA	—	—	0.4	V

Note 3: The mixer section is tested at 1.89 GHz, and it is guaranteed by design to operate within 1.7 — 2.0 GHz range.

Note 4: The IF section of this device is designed for optimum operating performance at 110 MHz to meet the DECT specifications.

Note 5: The matching network used on RF_{IN} consists of a series 3.3 pF capacitance into the pin. The matching circuit used on $MIXER_{OUT}$ consists of a series 100 nH inductance and a shunt 12 pF capacitance into the pin.

Note 6: Noise Figure measurements are made with 890 MHz BPF on the F_{IN} input and matching networks on RF_{IN} and $MIXER_{OUT}$.

Note 7: The matching network used on IF_{IN} consists of a series 33 nH inductance and a shunt 1.8 pF capacitance into the pin.

Note 8: The discriminator is with the DC level centered at 1.5V. The unloaded Q of the tank is 40.

Note 9: The frequency synthesizer section is guaranteed by design to operate within 500 - - 1200 MHz range.

Note 10: Nominal refers to zero DC offsets programmed for the discriminator.

Note 11: It depends on loss of inter-stage filter. These specifications are for an inter-stage filter with a loss of 8 dB.

Note 12: The frequency synthesizer section is guaranteed by design to operate for OSC_{IN} input frequency within 5 — 20 MHz range and minimun amplitude of 0.5 V_{pp}.

Electrical Characteristics (Continued)

Note 13: The doubler section is tested at 1.89 GHz, and it is guaranteed by design to operate within 1.7 — 1.9 GHz range.

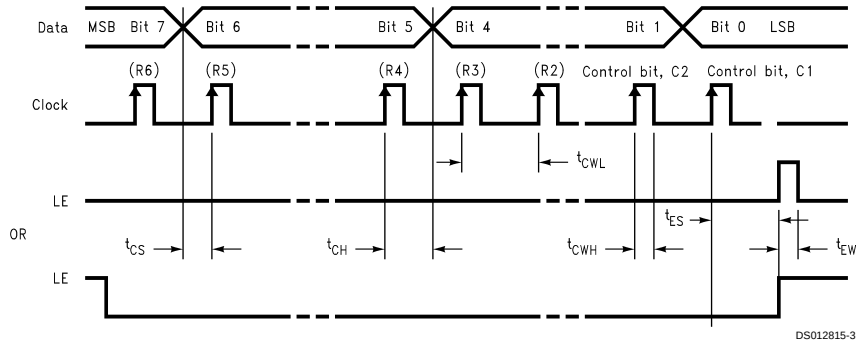
Note 14: See Function Register Programming Description for Icp_o description.

Note 15: Tested in a 50Ω environment.

AC Timing Characteristics

Serial Data Input Timing

TEST CONDITIONS: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an skew rate of 0.6 V / ns.

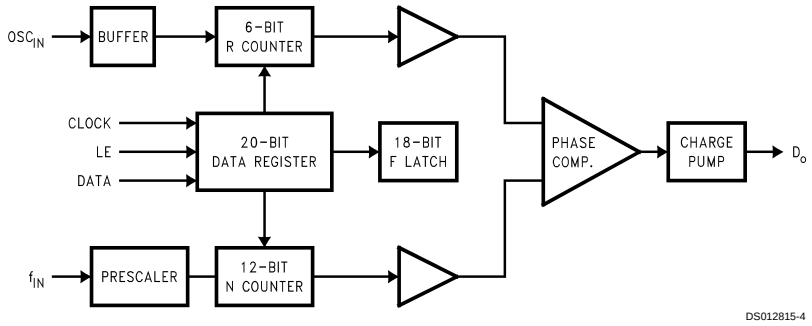


Notes: Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MICROWIRE™ Interface						
t_{CS}	Data to Clock Set Up Time	Refer to Test Condition.	50	—	—	ns
t_{CH}	Data to Clock Hold Time	Refer to Test Condition.	10	—	—	ns
t_{CWH}	Clock Pulse Width High	Refer to Test Condition.	50	—	—	ns
t_{CWL}	Clock Pulse Width Low	Refer to Test Condition.	50	—	—	ns
t_{ES}	Clock to Load Enable Set Up Time	Refer to Test Condition.	50	—	—	ns
t_{EW}	Load Enable Pulse Width	Refer to Test Condition.	50	—	—	ns

PLL Functional Description

The simplified block diagram below shows the building blocks of frequency synthesizer and all internal registers, which are 20-bit data register, 18-bit F-latch, 12-bit N-counter, and 6-bit R-counter.



The DATA stream is clocked into the data register on the rising edge of CLOCK signal, MSB first. The last two bits are the control bits to indicate which register to be written. Upon the rising edge of the LE (Load Enable) signal, the rest of data bits is transferred to the addressed register accordingly. The decoding scheme of the two control bits is as follows:

Control Bits		Register
C2	C1	
0	0	N-Counter
1	0	R-Counter
X	1	F-Latch

Note: X = Don't Care Condition

Programmable Feedback Divider (N-Counter)

The N-counter consists of the 6-bit swallow counter (A-counter) and the 6-bit programmable counter (B-counter). When the control bits are "00", data is transferred from the 20-bit shift register into two 6-bit latches. One latch sets the A-counter while the other sets the B-counter. The serial data format is shown below.

MSB						REGISTER'S BIT MAPPING													LSB
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						***N-COUNTER's Divide Ratio***												***C2***	***C1***
X	X	X	X	X	X	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	0	0

Note: X = Don't Care Condition

Swallow Counter Divide Ratio (A-Counter)

Divide Ratio, A	N6	N5	N4	N3	N2	N1
0	0	0	0	0	0	0
1	0	0	0	0	0	1
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Note: Divide ratio must be from 0 to 63, and B must be ≥ A.

Programmable Counter Divide Ratio (B-Counter)

Divide Ratio, B	N12	N11	N10	N9	N8	N7
3	0	0	0	0	1	1
4	0	0	0	1	0	0
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Note: Divide ratio must be from 3 to 63, and B must be ≥ A.

Programmable Reference Divider (R-Counter)

If the control bits are “10”, data is transferred from the 20-bit shift register into a latch, which sets the 6-bit R-counter. The serial data format is shown below.

MSB							REGISTER'S BIT MAPPING												LSB
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												***R-COUNTER's Divide Ratio***						***C2***	***C1***
X	X	X	X	X	X	X	X	X	X	X	X	R6	R5	R4	R3	R2	R1	1	0

Note: X = Don't Care Condition

Reference Counter Divide Ratio (R-Counter)

Divide Ratio, R	R6	R5	R4	R3	R2	R1
3	0	0	0	0	1	1
4	0	0	0	1	0	0
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Note: Divide ratio must be from 3 to 63.

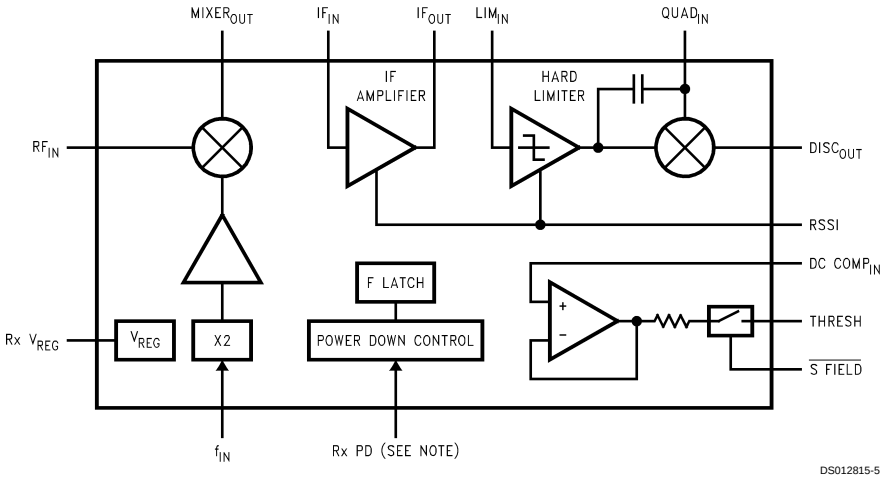
Pulse Swallow Function

$$f_{vco} = \frac{[(P \bullet B) + A] \bullet f_{osc}}{R}$$

f_{vco}: Output frequency of external voltage controlled oscillator (VCO)
B: Preset divide ratio of binary 6-bit programmable counter (3 to 63)
A: Preset divide ratio of binary 6-bit swallow counter ($0 \le A \le P$, $A \le B$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 6-bit programmable reference counter (3 to 63)
P: Preset modulus of dual modulus prescaler (32 or 64)

Receiver Functional Description

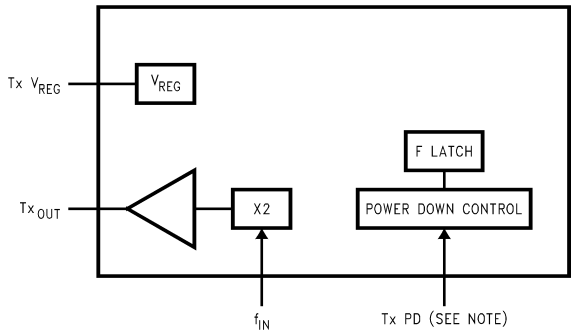
The simplified block diagram below shows the mixer, IF amplifier, limiter, and discriminator. In addition, the DC compensation circuit, doubler, and voltage regulator for an external LNA stage are shown.



Note: The receiver can be powered down, either by hardware through the Rx PD pin, or by software through the programming of F6 bit in F-Latch. The power down control method is determined by the settings of F11 and F12 in F-Latch. (Refer to Function Register Programming Description section for details.)

Transmitter Functional Description

The simplified block diagram below shows the doubler and voltage regulator for an external transmit gain stage.



Note: The transmitter can be powered down, either by hardware through the Tx PD pin, or by software through the programming of F7 bith in F-Latch. The power down control method is determined by the settings of F11 and F12 in F-Latch. (Refer to Function Register Programming Description section for details.)

Function Register Programming Description (F-Latch)

If the control bits are "1X", data is transferred from the 20-bit shift register into the 18-bit F-latch. Serial data format is shown below.

MSB							**REGISTER'S BIT MAPPING**											**LSB**	
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODE CONTROL WORD																		***C2***	***C1***
F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	X	1

Note: X = Don't Care Condition

Various modes of operation can be programmed with the function register bits F1–F18, including the phase detector polarity, charge pump TRI-STATE® and CMOS outputs. In addition, software or hardwire power down modes can be specified with bits F11 and F12.

Mode Control Bit	**Model Control Description**	**Setting to "0" to Select**	**Setting to "1" to Select**
F1	**Prescaler modules select.**	32/33	64/65
F2	**Phase detector polarity.** It is used to reverse the polarity of the phase detector according to the VCO characteristics.	Negative VCO Characteristics	Positive VCO Characteristics
F3	**Charge pump current gain select.**	LOW Charge Pump Current (1X I_{cpo}).	HIGH Charge Pump Current (4X I_{cpo}).
F4	**TRI-STATE charge pump output.**	Normal Operation	Force to TRI-STATE
F5	**Reserved.** Setting to "0" always.	—	—
F6	**Receive chain power down control.** Software power down can only be activated when both F11 and F12 are set to "0".	Power Up RX Chain	Power Down RX Chain
F7	**Transmit chain power down control.** Software power down can only be activated when both F11 and F12 are set to "0".	Power Up TX Chain	Power Down TX Chain
F8	**Out 0 CMOS output.**	OUT 0 = LOW	OUT 0 = HIGH
F9	**Out 1 CMOS output.** Functions only in software power down mode, when both F11 and F12 are set to "0".	OUT 1 = LOW	OUT 1 = HIGH
F10	**Out 2 CMOS output.** Functions only in software power down mode, when both F11 and F12 are set to "0".	OUT 2 = LOW	OUT 2 = HIGH
F11 F12	**Power down mode select.** Set both F11 and F12 to "0" for software power down mode. Set both F11 and F12 to "1" for hardwire power down mode. Other combinations are reserved for test mode.	Software Power Down	Hardware Power Down
F13	**Demodulator gain select**	1X Gain Mode	3X Gain Mode
F14	**Demodulator DC level shift +/− level shifting polarity**	Set Negative Polarity	Set Positive Polarity

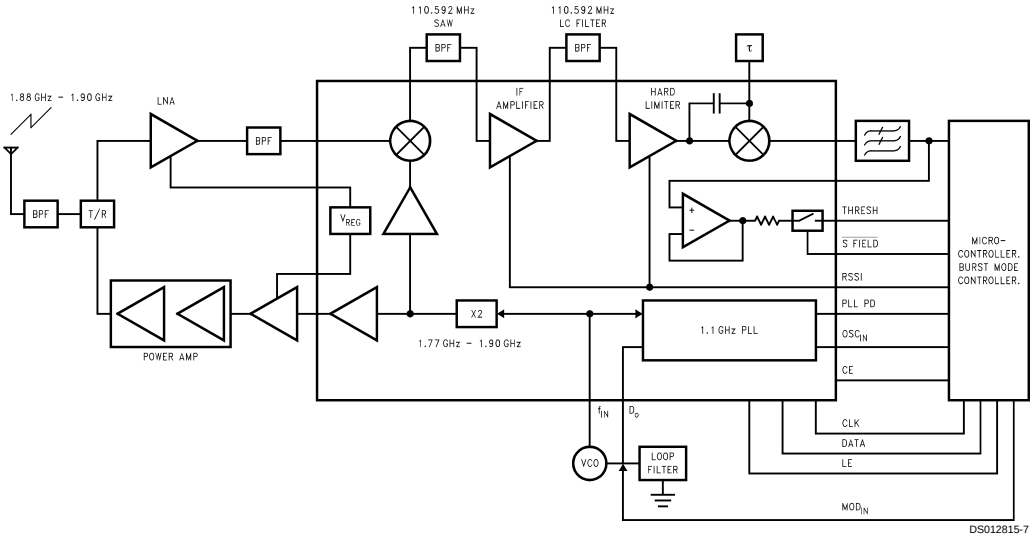
Function Register Programming Description (F-Latch) (Continued)

Mode Control Bit	Model Control Description	Setting to "0" to Select	Setting to "1" to Select
F15	**Demodulator DC level shift of 1.000V**	No Shift	Shift the DC Level by 1.000V
F16	**Demodulator DC level shift of 0.500V**	No Shift	Shift the DC Level by 0.500V
F17	**Demodulator DC level shift of 0.250V**	No Shift	Shift the DC Level by 0.250V
F18	**Demodulator DC level shift of 0.125V**	No Shift	Shift the DC Level by 0.125V

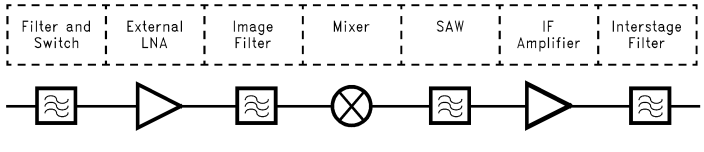
Power Down Mode/Control Table

Software Power Down Mode (F11=F12=0)			Hardwire Power Down Mode (F11=F12=1)		
Pin/Bit	Setting to "0" means	Setting to "1" means	Pin/Bit	Setting to "0" means	Setting to "1" means
F6	Receiver ON	Receiver OFF	Rx PD	Receiver OFF	Receiver ON
F7	Transmitter ON	Transmitter OFF	Tx PD	Transmitter OFF	Transmitter ON
PLL PD	PLL ON	PLL OFF	PLL PD	PLL ON	PLL OFF
CE	LMX3161 OFF	LMX3161 ON	CE	LMX3161 OFF	LMX3161 ON

Typical Application



DECT System Calculation for 3.6V Operation



	Filter and Switch	External LNA	Image Filter	Mixer	SAW	IF Amplifier	Interstage Filter	Cascade Total
NF (dB)	2	2	1.5	10	11	8	8	6.21
Gain (dB)	−2	12	−1.5	15	−11	25	−8	29.50
OIP3 (dBm)	100	7	100	5	100	50	100	10.88
P_{OUT} (dBm)	−95.0	−83.0	−84.5	−69.5	−80.5	−55.5	−63.5	
NF+ (dB)		1.09	0.04	1.58	0.05	0.32	0.00	
OIP3+ (dBm)	0.00	0.12	0.00	15.50	0.00	0.00		

Input Power (dBm) −93.00 Eb/No (dB) 14.77 Input IP3 (dBm) −18.62

DS012815-11

Note: Assumes 50 dB attenuation of interferer by the SAW filter and 8 dB attenuation by the LC filter. Cascaded totals in Input IP3 are calculated at the output of the interstage filter.

Loop Filter Design Consideration

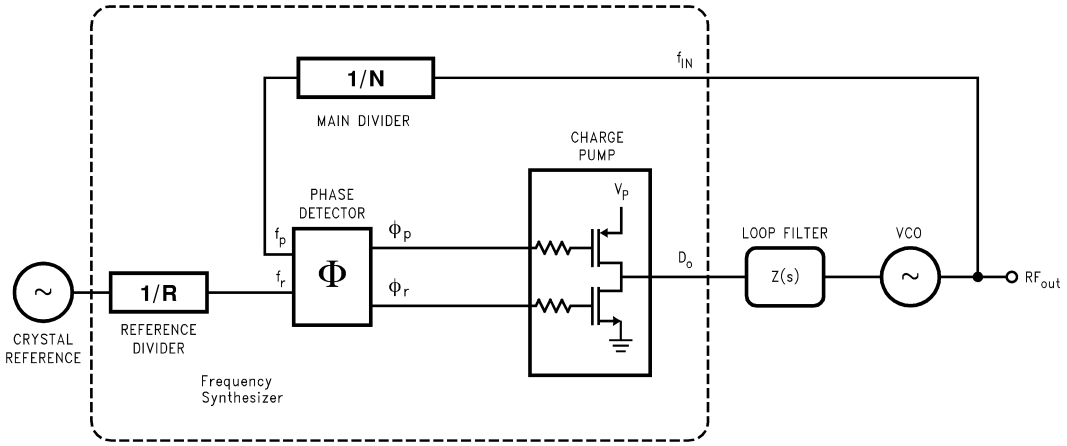


FIGURE 1. Conventional PLL Architecture

Loop Gain Equations

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2*. The open loop gain is the product of the phase comparator gain (K_ϕ), the VCO gain (K_{vco}/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3*, while the complex impedance of the filter is given in *Equation (2)*.

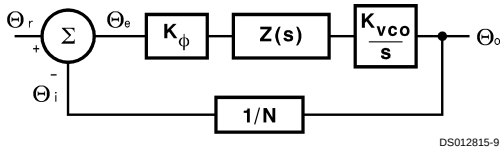


FIGURE 2. PLL Linear Model

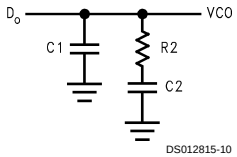


FIGURE 3. Passive Loop Filter

PASSIVE LOOP FILTER

$$\text{Open loop gain} = H(s)\,G(s) = \theta i/\theta e = K_\phi\, Z(s) K_{VCO}/Ns \quad (1)$$

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2(C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (2)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (3)$$

and

$$T2 = R2 \bullet C2 \quad (4)$$

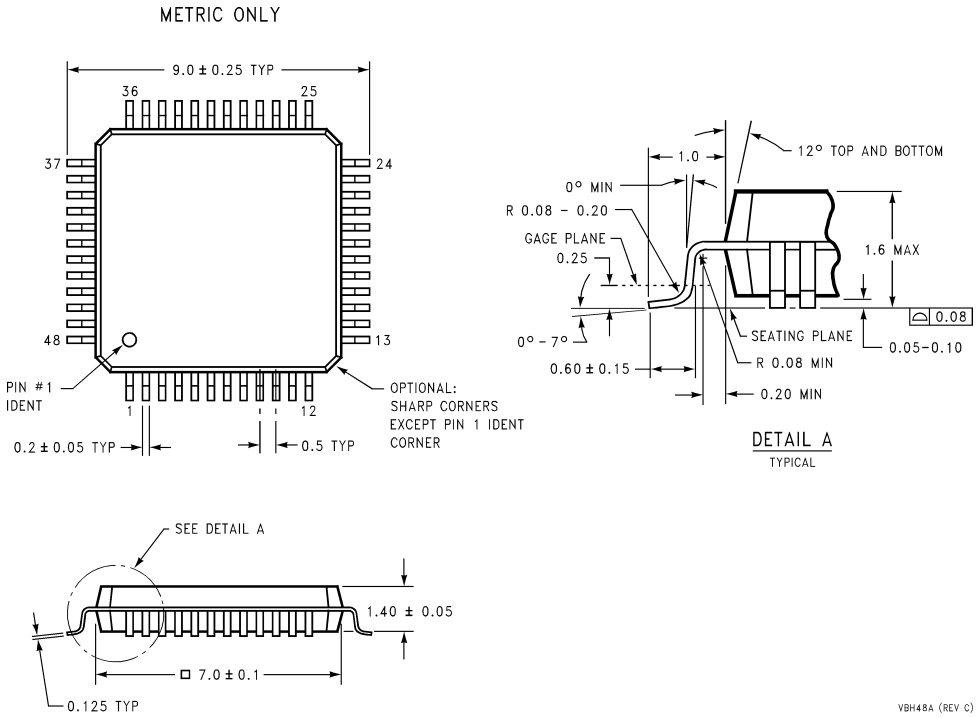
The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants K_ϕ, K_{vco}, and N.

$$G(S) \bullet H(S)\Big|_{S = j\bullet\omega} \frac{-K_\phi \bullet K_{vco}(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (5)$$

From *Equations (3), (4)* we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in *Equation (6)*.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180^\circ \quad (6)$$

Physical Dimensions inches (millimeters) unless otherwise noted



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