LMX3305

LMX3305 Triple Phase Locked Loop for RF Personal Communications



Literature Number: SNOS533B



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Triple Phase Locked Loop for RF Personal Communications

General Description

The LMX3305 contains three Phase Locked Loops (PLL) on a single chip. It has a RF PLL, an IF Rx PLL and an IF Tx PLL for CDMA applications. The RF fractional-N PLL uses a 16/17/20/21 quadruple modulus prescaler for PCS application and a 8/9/12/13 quadruple modulus prescaler for cellular application. Both quadruple modulus prescalers offer modulo 1 through 16 fractional compensation circuitry. The RF fractional-N PLL can be programmed to operate from 800 MHz to 1400MHz in cellular band and 1200MHz to 2300 MHz in PCS band. The IF Rx PLL and the IF Tx PLL are integer-N frequency synthesizers that operate from 45 MHz to 600 MHz with 8/9 dual modulus prescalers. Serial data is transferred into the LMX3305 via a microwire interface (Clock, Data, & LF)

The RF PLL provides a fastlock feature allowing the loop bandwidth to be increased by 3X during initial lock-on.

The supply voltage of the LMX3305 ranges from 2.7V to 3.6V. It typically consumes 9 mA of supply current and is packaged in a 24-pin CSP package.

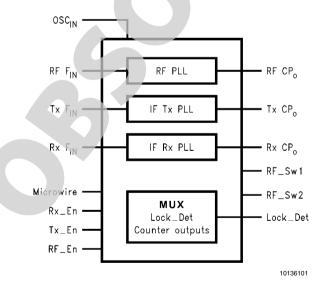
Features

- Three PLLs integrated on a single chip
- RF PLL fractional-N counter
- 16/17/20/21 RF quadruple modulus prescaler for PCS application
- 8/9/12/13 RF quadruple modulus prescaler for cellular application
- 2.7V to 3.6V operation
- Low current consumption: I = 9 mA (typ) at 3.0V
- Programmable or logical power down mode: I_{CC} = 10 μA (typ) at 3.0V
- RF PLL Fastlock feature with timeout counter
- Digital lock detect
- Microwire Interface with data preset
- 24-pin CSP package

Applications

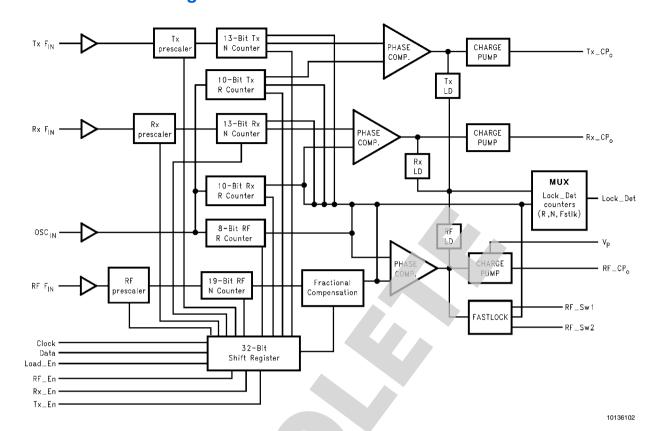
■ CDMA Cellular telephone systems

Block Diagram

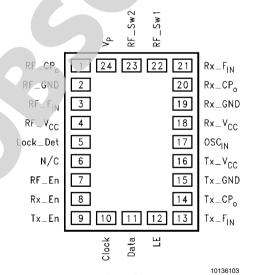


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Functional Block Diagram



Connection Diagram



Top View Order Number LMX3305SLBX See NS Package Number SLB24A

Pin Descriptions

Pin No.	Pin Name	1/0	Description
1	RF_CP _o	0	Charge pump output for RF PLL. For connection to a loop filter for driving the input of an external VCO.
2	RF_GND	PWR	RF PLL ground.
3	RF_F _{IN}	ı	RF prescaler input. Small signal input from the RF Cellular or PCS VCO.
4	RF_V _{CC}	PWR	RF PLL power supply voltage. Input may range from 2.7V to 3.6V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. Tx $V_{CC} = Rx V_{CC} = RF V_{CC}$.
5	Lock_Det	0	Multiplexed output of the RF, Rx, and Tx PLL's analog or digital lock detects. The outputs from the R, N and Fastlock counters can also be selected for test purposes. Refer to Section 2.3.4 for more detail.
6	N/C		No Connect.
7	RF_En	I	RF PLL enable pin. A LOW on RF En powers down the RF PLL and TRI-STATE®s the RF PLL charge pump.
8	Rx_En	I	Rx PLL enable pin. A LOW on Rx En powers down the Rx PLL and TRI-STATEs the Rx PLL charge pump.
9	Tx_En	I	Tx PLL enable pin. A LOW on Tx En powers down the Tx PLL and TRI-STATEs the Tx PLL charge pump.
10	Clock	I	High impedance CMOS clock input. Data for the various counters is clocked on the rising edge into the CMOS input.
11	Data	I	Binary serial data input. Data entered MSB first.
12	LE	I	High impedance CMOS input. When LE goes LOW, data is transferred into the shift registers. When LE goes HIGH, data is transferred from the internal registers into the appropriate latches.
13	Tx_F _{IN}	ı	Tx prescaler input. Small signal input from the Tx VCO.
14	Tx_CP _o	0	Charge pump output for Tx PLL. For connection to a loop filter for driving the input of an external VCO.
15	Tx_GND		Tx PLL ground.
16	Tx_V _{CC}	PWR	Tx PLL power supply voltage input. Input may range from 2.7V to 3.6V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. Tx $V_{CC} = Rx \ V_{CC} = RF \ V_{CC}$.
17	OSC _{IN}	I	PLL reference input which has a V _{CC} /2 input threshold and can be driven from an external CMOS or TLL logic gate. The R counter is clocked on the falling edge of the OSC _{IN} signal.
18	Rx_V _{CC}	PWR	Rx PLL power supply voltage. Input ranges from 2.7V to 3.6V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. Tx $V_{CC} = Rx V_{CC} = RF V_{CC}$.
19	Rx_GND	PWR	Rx PLL ground.
20	Rx_CP _o	0	Charge pump output for Rx PLL. For connection to a loop filter for driving the input of an external VCO.
21	Rx_F _{IN}	I	Rx prescaler input. Small signal input from the Rx VCO.
22	RF_Sw1	0	An open drain NMOS output which can be use for bandswitching or Fastlocking the RF PLL. (During Fastlock mode a second loop filter damping resistor can be switched in parallel with the first to ground.) Refer to Section 2.5.3 for more detail.
23	RF_Sw2	0	An open drain NMOS output which can be use for bandswitching or Fastlocking the RF PLL. (During Fastlock mode a second loop filter damping resistor can be switched in parallel with the first to ground.) Refer to Section 2.5.3 for more detail.
24	V _P	0	RF PLL charge pump power supply. An internal voltage doubler can be enabled in 3V applications to allow the RF charge pump to operate over a wider tuning range.

Absolute Maximum Ratings (Notes 1, 2)

Power Supply Voltage (PLL $V_{\rm CC}$)

(Note 3) -0.3V to +6.5VSupply Voltage (V_P) -0.3V to +6.5V

Voltage on any Pin with

GND = 0V (V_I) -0.3V to V_{CC} +0.3V Storage Temperature Range (T_S) -65° C to +150°C Lead Temp. (solder, 4 sec.) (T_L) +240°C ESD - Whole Body Model (Note 2) 2 kV

Recommended Operating Conditions (Note 1)

Power Supply Voltage (PLL V_{CC})

 $\begin{array}{lll} \mbox{(Note 3)} & 2.7 \mbox{ to } 3.6 \mbox{V} \\ \mbox{Supply Voltage (V$_{P}$) (Note 3)} & \mbox{PLL V$_{CC}$ to } 5.5 \mbox{V} \\ \mbox{Operating Temperature (T$_{A}$)} & -30 \mbox{^{\circ}C to } +85 \mbox{^{\circ}C} \\ \end{array}$

Electrical Characteristics

 $(V_{CC} = V_P = 3V, -30^{\circ}C < T_A < 85^{\circ}C$ except as specified)

Cumbal	Parameter	Conditions		Value		Unit
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
GENERAL						
I _{cc}	Power Supply Current	RF = On, Rx = On, Tx = On $2.7V \le V_{CC} \le 3.6V$		9.0	15	mA
I _{CC} -PWDN	Power Down Current			10	75	μA
f _{IN}	PCS Operating Frequency		1200		2300	
	Cellular Operating Frequency		800		1400	MHz
	IF Operating Frequency (Rx, Tx)		45		600	
f _{osc}	Oscillator Frequency			19.68	25	MHz
f_{ϕ}	Phase Detector Frequency				10	MHz
Pf _{IN}	PCS/Cellular/IF Input Sensitivity	2.7V ≤ V _{CC} ≤ 3.6V	-15	1	+0	dBm
Pf _{OSC}	Oscillator Sensitivity		0.5		V _{cc}	V _{PP}
RF PN	RF Phase Noise	F _{OUT} = 1 GHz		-70		ID (1)
IF PN	IF Phase Noise			-70		dBc/Hz
	Fractional Spur @ 10 kHz	1 kHz Loop Filter (Note 4)			-50	dBc
	Fractional Spur Harmonic		1	nuate 6 dE after 10 kF		dBc
Tsw	Switching Speed	1 kHz Loop Filter, 60 MHz Jump to Within 1 kHz			4.0	ms
CHARGE PL	ÜMP					
RF I _{Do} Source	RF Charge Pump Source Current	$V_{Do} = V_P/2 \text{ (Note 5)}$	-22	I _{NOM}	22	%
RF I _{Do} Sink	RF Charge Pump Sink Current	V _{Do} = V _P /2 (Note 5)	-22	I _{NOM}	22	%
IF I _{Do}	IF Charge Pump Source Current	$V_{Do} = V_{CC}/2$ (Note 5)	80	100	120	μΑ
IF I _{Do} Sink	IF Charge Pump Sink Current	V _{Do} = V _{CC} /2 (Note 5)	-80	-100	-120	μΑ
I _{Do} -TRI	Charge Pump TRI-STATE Current	(Note 6)			1000	pA
I _{Do} Sink vs I _{Do} Source	Charge Pump Sink vs Source Mismatch	T _A = 25°C (Note 7)		3	10	%
I _{Do} vs V _{Do}	Charge Pump Current vs Voltage	T _A = 25°C (Note 6)		8	15	%
I _{Do} vs T _A	Charge Pump Current vs Temperature	(Note 7)		5	10	%
DIGITAL INF	PUTS AND OUTPUTS	-			L	
V _{IH}	High-Level Input Voltage	V _{CC} = 2.7V to 3.6V	0.8 V _{CC}			V
V _{IL}	Low-Level Input Voltage	V _{CC} = 2.7V to 3.6V			0.2 V _{CC}	٧
V _{OL}	Low-Level Output Voltage	I _{OL} = 2 mA			0.4	V
I _{IH}	High-Level Input Current	$V_{IH} = V_{CC} = 3.6V$	-1.0		1.0	μA
I _{IL}	Low-Level Input Current	V _{IL} = 0V, V _{CC} = 3.6V	-1.0		1.0	μA
I _{IH}	OSC _{IN} High-Level Input Current	$V_{IH} = V_{CC} = 3.6V$			100	μA

Cumbal	Dovernator	Conditions		Value		I I mit
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$I_{\rm IL}$	OSC _{IN} Low-Level Input Current	$V_{IL} = 0V, V_{CC} = 3.6V$	-100			μA
t _{cs}	Data to Clock Setup Time		50			ns
t _{CH}	Data to Clock Hold Time		10			ns
t _{cwh}	Clock Pulse Width High		50			ns
T _{CWL}	Clock Pulse Width Low		50			ns
t _{ENSL}	Clock to Load_En Setup Time		50			ns
t _{ENW}	Load_En Pulse Width		50			ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should be done on ESD protected workstations.

Note 3: PLL $\rm V_{CC}$ represents RF $\rm V_{CC}, \, Tx \, V_{CC}$ and Rx $\rm V_{CC}$ collectively.

Note 4: Guaranteed by design. Not tested in production.

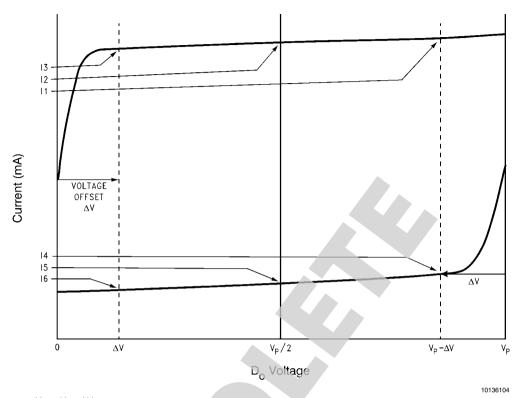
Note 5: I_{NOM} = 100 μ A, 400 μ A, 700 μ A or 900 μ A for RF charge pump.

Note 6: For RF charge pump, 0.5 \leq V_{Do} \leq V_P - 0.5; for IF charge pump, 0.5 \leq V_{Do} \leq V_{CC} - 0.5.

Note 7: For RF charge pump, $V_{Do} = V_{P}/2$, for IF charge pump, $V_{Do} = V_{CC}/2$.



Charge Pump Current Specification Definitions



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I1 = CP sink current at V_{Do} = V_P - \Delta V
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 ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V.

- 1. I_{Do} vs V_{Do} = Charge Pump Output Current magnitude variation vs Voltage =
 - $\left[\frac{1}{2} * \{||1| ||3|\}\right] / \left[\frac{1}{2} * \{||1| + ||3|\}\right] * 100\% \ and \left[\frac{1}{2} * \{||4| ||6|\}\right] / \left[\frac{1}{2} * \{||4| + ||6|\}\right] * 100\%$
- 2. $I_{Do\text{-sink}}$ vs $I_{Do\text{-source}}$ = Charge Pump Output Current Sink vs Source Mismatch = [||2| ||5||] $/ [\frac{1}{2} * {||2| + ||5||}] * 100\%$
- 3. I_{Do} vs T_A = Charge Pump Output Current magnitude variation vs Temperature =

[II2 @ templ - II2 @ 25°Cl] / II2 @ 25°Cl * 100% and [II5 @ templ - II5 @ 25°Cl] / II5 @ 25°Cl * 100%

I2 = CP sink current at $V_{Do} = V_P/2$

I3 = CP sink current at $V_{Do} = \Delta V$

I4 = CP source current at $V_{Do} = V_P - \Delta V$

I5 = CP source current at $V_{Do} = V_P/2$

I6 = CP source current at $V_{Do} = \Delta V$

1.0 Functional Description

The LMX3305 phase-lock-loop (PLL) system configuration consists of a high-stability crystal reference oscillator, three frequency synthesizers, three voltage controlled oscillators (VCO), and three passive loop filters. Each of the frequency synthesizers includes a phase detector, a current mode charge pump, as well as programmable reference [R] and feedback [N] frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the R-counter to obtain a comparison reference frequency. This reference signal (f_B) is then presented to the input of a phase/ frequency detector and compared with the feedback signal (f_N), which is obtained by dividing the VCO frequency down by way of the N-counter, and fractional circuitry. The phase/ frequency detector's current source output pumps charge into the loop filter, which then converts the charge into the VCO's control voltage. The function of phase/frequency comparator is to adjust the voltage presented to the VCO until the feedback signal frequency and phase match that of the reference signal. When the RF PLL is in a "Phase-Locked" condition, the RF VCO frequency will be (N + F) times that of the comparison frequency, where N is the integer divide ratio, and F is the fractional component. The fractional synthesis allows the phase detector frequency to be increased while maintaining the same frequency step size for channel selection. The divider ratio N is thereby reduced giving a lower phase noise referred to the phase detector input, and the comparison frequency is increased allowing faster switching time.

1.1 REFERENCE OSCILLATOR INPUTS

The reference oscillator frequency for the RF and IF PLLs are provided from the external references through the ${\rm OSC_{IN}}$ pin. ${\rm OSC_{IN}}$ input can operate up to 25 MHz with input sensitivity of 0.5 ${\rm V_{PP}}$ minimum and it drives RF, Rx and Tx R-counters. ${\rm OSC_{IN}}$ input has a ${\rm V_{CC}/2}$ input threshold that can be driven from an external CMOS or TTL logic gate. Typically, the ${\rm OSC_{IN}}$ is connected to the output of a crystal oscillator.

1.2 REFERENCE DIVIDERS (R-COUNTERS)

The RF, Rx and Tx R-counters are clocked through the oscillator block. The maximum frequency is 25 MHz. All RF, Rx and Tx R-counters are CMOS design. The RF R-counter is 8-bit in length with programmable divider ratio from 2 to 255. The Rx and Tx R-counters are 10-bit in length with programmable divider ratio from 2 to 1023.

1.3 PRESCALERS

The LMX3305 has a 16/17/20/21 quadruple modulus prescaler for the PCS application and a 8/9/12/13 quadruple modulus prescaler for the cellular application. The Rx and Tx prescalers are dual modulus with 8/9 modulus ratio. Both RF/IF prescalers' outputs drive the subsequent CMOS flip-flop chain comprising the programmable N feedback counters.

1.4 FEEDBACK DIVIDERS (N-COUNTERS)

The RF, Rx and Tx N-counters are clocked by the output of RF, Rx and Tx prescalers respectively. The RF N-counter is composed of two parts: the 15 MSB bits comprise the integer portion and the 4 LSB bits comprise the fractional portion. The RF fractional N divider is fully programmable from 80 to 32767 over the frequency range from 1200 MHz-2300 MHz for PCS application and 40 to 16383 over the frequency range from 800 MHz-1400 MHz for cellular application. The 4-bit fractional portion of the RF counter represents the fraction's numerator. The fraction's denominator base is determined by the four **FRAC_D** register bits.

The Rx and Tx N-counters are each a 13-bit integer divisor, fully programmable from 56 to 8,191 over the frequency range from 45 MHz–600 MHz. The Rx and Tx N-counters do not include fractional compensation.

1.5 FRACTIONAL COMPENSATION

The fractional compensation circuitry of the LMX3305 RF divider allows the user to adjust the VCO tuning resolution in 1/2 through 1/16th increments of the phase detector comparison frequency. A 4-bit denominator register (FRAC_D) selects the fractional modulo base. The integer averaging is accomplished by using a 4-bit accumulator. A variable phase delay stage compensates for the accumulated integer phase error, minimizes the charge pump duty cycle and reduces the spurious levels. This technique eliminates the need for compensation current injection into the loop filter. An overflow signal generated by the accumulator is equivalent to one full RF VCO cycle, and results in a pulse swallow.

1.6 PHASE/FREQUENCY DETECTORS

The RF and IF phase/frequency detectors are driven from their respective N- and R-counter outputs. The maximum frequency at the phase detector inputs is 10 MHz unless limited by the minimum continuous divide ratio of the multi-modulus prescaler. The phase detector output controls the charge pump. The polarity of the pump-up or pump-down control is programmed using RF_PD_POL, Rx_PD_POL, or Tx_PD_POL depending on whether RF or IF VCO characteristics are positive or negative. The phase detector also receives a feedback signal from the charge pump in order to eliminate dead zones.

1.7 CHARGE PUMPS

The phase detector's current source output pumps charge into an external loop filter, which then converts it into the VCO's control voltage. The charge pump steers the charge pump output CP $_{\rm o}$ to V $_{\rm CC}$ (pump-up) or Ground (pump-down). When locked, CP $_{\rm o}$ is primarily in a TRI-STATE mode with small corrections. The IF charge pump output current magnitudes are nominally 100 μA . The RF charge pump output currents can be programmed by the RF_lcpo bits at 100 μA , 400 μA , 700 μA , or 900 μA .

1.8 VOLTAGE DOUBLER (VD)

The V_P pin is normally driven from an external power supply over a range of V_{CC} to 5.5V to provide current for the RF charge pump circuit. An internal voltage doubler circuit connected between the V_{CC} and V_P supply pins alternately allows $V_{CC} = 3V \ (\pm 10\%)$ users to run the RF charge pump circuit at close to twice the V_{CC} power supply voltage. The voltage doubler mode is enabled by setting the V2X bit to a HIGH level. The voltage doubler's charge pump driver originates from the oscillator input. The device will not totally powerdown until the V2X bit is programmed LOW. The average delivery current of the doubler is less than the instantaneous current demand of the RF charge pump when active and is thus not capable of sustaining a continuous out of lock condition. A large external capacitor connected to V_P (=0.1 μ F) is needed to control power supply droop when changing frequencies.

1.9 MICROWIRE INTERFACE

The programmable register set is accessed through the microwire serial interface. The interface is comprised of three signal pins: Clock, Data, and LE. After the LE goes LOW, serial data is clocked into the 32-bit shift register upon the rising edge of Clock MSB first. The last three data bits shifted into the shift register select one of five addresses. When LE goes

HIGH, data is transferred from the shift registers into one of the four register bank latches. Selecting the address <000> presets the data in the four register banks. The synthesizer can be programmed even in the power down (or not enabled) state.

1.10 LOCK DETECT OUTPUTS

The open-drain Lock Detect is available in the LMX3305 to provide a digital or analog lock detect indication for the sum of the active PLLs. In the digital lock detect mode, an internal digital filter produces a logic level HIGH at the lock detect output when the error between the phase detector inputs is less than 15 ns for five consecutive comparison cycles. The lock detect output is LOW when the error between the phase detector inputs is more than 30 ns for one comparison cycle. In the analog lock detect mode, the lock detect pin becomes active low whenever any of the active PLLs are charge pumping. The Lock_Det pin can also be programmed to provide the outputs of the R, N or fastlock timeout counters.

1.11 POWER CONTROL

Each PLL is individually power controlled by the microwire power down bits Rx_PWDN, Tx_PWDN and RF_PWDN. Alternatively, the PLLs can also be power controlled by the Tx_En, Rx_En, and RF_En pins. The enable pins override the power down bits except for the V2X bit. When the respective PLL's enable pin is high, the power down bits determine the state of power control. Activation of any PLL power down modes result in the disabling of the respective N counter and de-biasing of its respective f_{IN} input (to a high impedance state). The R counter functionality also becomes disabled when the power down bit is activated. The reference oscillator block powers down and the OSC_{IN} pin reverts to a high impedance state when all of the enable pins are LOW or all of the power down bits are programmed HIGH, unless V2X bit is HIGH. Power down forces the respective charge pump and phase comparator logic to a TRI-STATE condition. A power down counter reset function resets both N and R counters of the respective PLL. Upon powering up the N counter resumes counting in "close" alignment with the R counter (the maximum error is one prescaler cycle). The microwire control register remains active and capable of loading and latching in data during all of the power down modes.

2.0 Programming Description

2.1 MICROWIRE SERIAL BUS INTERFACE

The LMX3305 uses Clock, Data, and LE signals to accomplish all data transactions. Data is latched into the 32-bit shift register on the rising edge of Clock, MSB first. The last three bits loaded are the address bits that determine which of the four Data register banks the shift register data will be transferred to when LE goes HIGH.

Bit	0	SS	5	0	-		0		-		0	
icant	<u>-</u>	Address	rieia	0	0		-		-		0	
ignif	7	٩	\dashv	0	0	011-11	0	ON - 11	0	011-111	-	ON- III
Least Significant Bit	4				TSA_xA ×	1F_R1 1F_R0	NQW9_xA	IF_N0	TSA_7A XSV	rF_R1 PF_R0	[2:0]	RF_N1
۔ ا	2				109_09_x8			IF_N2	JO9_Q9_3A		Test [2:0]	RF_N2
	9						VA_CN1					
	L					EA_7I	Rx_NA_CNTR [2:0]	EN_AI		ER_AA	RF_PWDN	RF_N3
-	_					₽₽_٦I	<u> </u>	IF_N4	BF_lcpo	PF_R4	PCS	BF_N4
ב ב	8					2H_7I		IE_N5	[(BF_R5	sdq∃	RF_N5
ao O U	6	1			[0:6]	9H_7I		IE_N6	FRAC_CAL [4:0]	9A_7A	[0:	BF_N6
	9				NTR	48_리		∠N_∃I	/\(\)__\	TA_AA	E 0	7N_∃Я
M 01 K	=				Rx_R_CNTR [9:0]	8A_7I	[0:6]	IF_N8	FRA	8A_7A	FRAC_D [3:0]	RF_N8
elle	12				Œ	8년_귀	NTA	6N_∃I		8F_R9		BF_N9
Itans	13					01A_71	Rx_NB_CNTR [9:0]	01N_=	FWSTSH	01A_7A		RF_N10
LOCATION	14			<u>^</u>		IF_R11	ă,	IF_N11	FSTSW2	FF_R11	FRAC_N [3:0]	RF_N11
LOCA LOCA	15			et <000		1F_R12		STN_3	FRIMI	S18_78	'BAC	RF_N12
BISTER 8 BIT	16	פ		Pres dress		E1R13		E_N13	FSTM2	£ŀЯ_∃Я		RF_N13
STE	17	Data Field		ter bits iing ad	[0:E] CT	1F_R14		PLN_AI		PF_R14		PF_N14
Banks the shill reg SHIFT REGISTER	18	Da		All Register bits Preset (Upon LE latching address <000>)	ГР	21A_11	NDW9_XT	arn_al	[0	81A_7A		BF_N15
loaded are the address bits that determine which of the four Data register banks the smit register data will be transferred to when LE goes Filch Most Significant Bit	19			All pon L		IF_R16	5:0]	1F_N16	FSTL_CNTR [6:0]	8F_R16		8F_N16
alsife	20			D)	TSA_xT	TIA FI	Tx_NA CNTR [2:0]	7 t N_ =1	CO	₹18_38		TF_N17
Jala It	2				104_09_XT	IF_R18	Γ δ ————————————————————————————————————	1F_N18	FSTL	81A_7A		8F_N18
inol	22					마 메리		lE_N19		e≀ਸ_ਜਸ	[o:	8F_N19
5	23	1				1F_R20		IF_N20		RF_R20	RF_N_CNTR [14:0]	RF_N20
	24					IF_R21		IF_N21		RF_R21	CN]	RF_N21
<u> </u>	25				[9:0]	IF_R22	[0:6]	IF_N22		RF_R22	Я N_	RF_N22
neie	56				NTR [IF_R23	R T X	IF_N23	[0:2]	RF_R23		RF_N23
) II II	27				Tx_R_CNTR [9:0]	1F_R24	Tx_NB_CNTR [9:0]	IF_N24	RF_R_CNTR [7:0]	PF_R24		RF_N24
t Bit	28				×	1F_R25	<u> </u>	IE_N25	ا ه ^ـ ک	RF_R25		RF_N25
Significant Bit	29					1F_R26		IF_N26	AR.	92A_7A		RF_N26
Sign	30					72A_7I		15_N27		72A_7A		72N_7A
Most	31					82A_7I		1F_N28		85R_7R		85N_7A
2				А	R_R		N_=	II	R_1	4	F_N	8

Note: X denotes don't care bits.

2.2 P REGISTER

P register has the special function of programming all of the registers to a preset known set state shown below. Note that this does not prevent the other four address registers from being programmed after this.

Number 1900 Number 190	15	١.		1	6								1	ì	H	1	-	i											-			i
10 10 10 10 10 10 10 10	ı Sign	ᄅ	ĭ⊦	gant	<u> </u>	+	-	L	ŀ	ŀ				_ <u> </u>		<u> </u>	3	S A	L				L						Leas	st Sign	IIIca	֡֞֝֟֝֟֝֟֝֟֝֟֝֟֝֟֝֟
Pale Field	$\overline{}$	21	$\overline{}$		22	56 ;	$\overline{}$		\dashv	\dashv	21	20	19	18	14	16	-		\dashv	12	Ξ	우	6	8	_	9	2	4	က	7	-	0
Milegister bits Preset Cupon Le latching address Cucon Cupon Le latching address																Data	Field													Add	ress	-ield
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H_3:0]											81HII		IF_R16	81A_31	1F_R14	F_R13	IF_R12	IF_R11	IF_R10	[논_면9	8F_R	7A_7I	9H_7I	IF_R5	IF_R4	IF_R3	SH_7I	1F_R1	0H_AI			
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2.3 IF_R REGISTER

If the ADDRESS [2:0] field is set to 001, data is transferred from the 32-bit shift register into the IF_R register when LE signal goes high. The IF_R register sets the Rx PLL's 10-bit R counter divide ratio and various programmable bits. The divide ratio for both Rx and Tx R counters are from 2 to 1023.

t Bit	0	jeld	-	
ifican	-	ess F	0	
Signi	2	Address Field	0	
Least Significant Bit	ဗ		×	0H_R
	4		TSA_xA	ᄪᆖᆀ
	2			
	9		DOT_DQ_XR	SR_7I
				EA_7I
	7			⊅H_71
	8			2H_7I
	6		[0:6]	9日_리
	10		RTN	78_3I
	11		Rx_R_CNTR [9:0]	8F_7I
	12		ê 	8日_刊
Z	13			01A_7I
ATIO	14			118_71
SHIFT REGISTER BIT LOCATION	15	-ield		S18_7I
ER BI	16	Data Field		F_R13
GIST	41		3:0]	F_R14
FT RE	18 17 16 15 14 13 12 11 10 9		[0:8]	BIA_FI
SHI	19			IF_R16
	20		TSA_xT	₹18_AI
	21		JO9_Q9_XT	81A_4I
	22			F_R19
	23			12.1 1F_R20
	2 25 2 6 4		[0:	IF_R22
	2 2	,	9 H	IF_R23
Bit			CN	F_R24
Most Significant Bit	31 30 29 28 27		Tx_R_CNTR [9:0]	P_R25
nific	59		🖰	92A_7I
Sig	30			72A_7I
/lost	31			82A_7I
_		<u> </u>	R_7I	1

Note: X denotes don't care bit.

2.3.1 10-Bit IF Programming Reference Divider Ratio (Tx R Counter, Rx R Counter)

Divide Ratio			Tx_R_	CNTR	[9:0] o	r Rx_F	CNTI	R [9:0]		
2	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•
1023	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio for both Tx and Rx R counters are from 2 to 1023.

2.3.2 Tx_PD_POL (IF_R[18])

This bit sets the polarity of the Tx phase detector. It is set to one when Tx VCO characteristics are positive. When Tx VCO frequency decreases with increasing control voltage, Tx_PD_POL should be set to zero.

2.3.3 Tx_RST (IF_R[17])

This bit will reset the Tx R and N counters when it is set to one. For normal operation, Tx_RST should be set to zero.

2.3.4 LD (IF_R[16]-[13])

The LD pin is a multiplexed output. When in lock detect mode, LD does ANDing function on the active PLLs. The RF fractional test mode is only intended for factory testing.

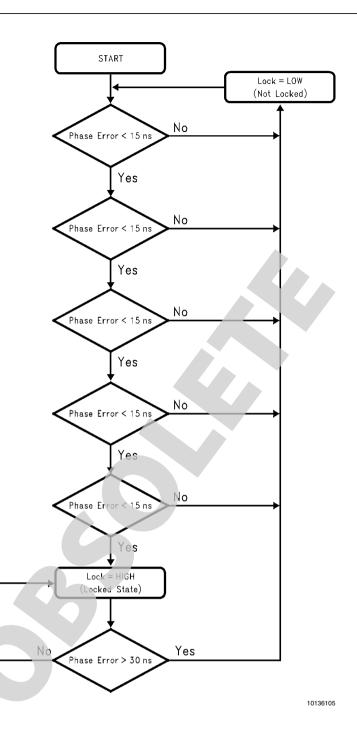
Lock Detect Output Truth Table

	LD [[3:0]		LD Pin Function	Output Format
0	0	0	0	Digital Lock Detect	Open Drain
0	0	0	1	Analog Lock Detect	Open Drain
1	0	0	0	Rx R Counter	CMOS
1	0	0	1	Rx N Counter	CMOS
1	0	1	0	Tx R Counter	CMOS
1	0	1	1	Tx N Counter	CMOS
1	1	0	0	RF R Counter	CMOS
1	1	0	1	RF N Counter	CMOS
1	1	1	0	RF Fastlock Timeout Counter	CMOS
1	1	1	1	RF Fractional Test Mode	Analog

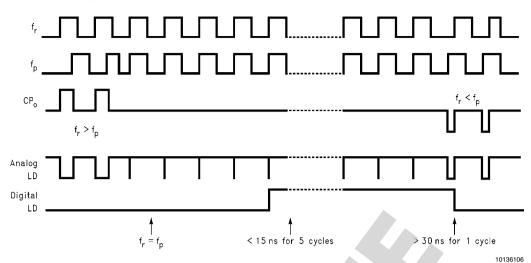
Lock Detect Digital Filter

The Lock Detect Digital Filter compares the difference between the phase of the inputs of the phase detector to a RC generated delay of approximately 15 ris. To enter the locked state (Lock Det = HIGH) the phase error must be less than the 15 ns RC delay for five consecutive reference cycles.

Once in lock (Lock Det = HIGH), the RC delay is changed to approximately 30 ns. To exit the locked state (Lock Det = LOW), the phase error must become greater than the 30 ns RC delay. When the PLL is in the powerdown mode, Lock Det is forced HIGH. A flow chart of the digital filter is shown below.



Typical Lock Detect Timing



2.3.5 Rx_PD_POL (IF_R[2])

This bit sets the polarity of the Rx phase detector. It is set to one when Rx VCO characteristics are positive. When Rx VCO frequency decreases with increasing control voltage, Rx_PD_POL should set to zero.

2.3.6 Rx_RST (IF_R[1])

This bit will reset the Rx R and N counters when it is set to one. For normal operation, Rx_RST should be set to zero.

2.4 IF_N REGISTER

If the ADDRESS [2:0] field is set to 010, data is transferred from the 32-bit shift register into the IF_N register when LE signal goes high. The IF_N register sets the Rx PLL's 13-bit N counter divide ratio and various programmable bits. Both N counters consist of the 3-bit swallow counter (A counter) and the 10-bit programmable counter). N divider continuous integer divide ratio is from 56 to 8191.

ר Bit	0	Address Field	0			
ificar	-	ress	-			
Sign	2	Add	0			
Least Significant Bit	3		×	IE_N0		
	4		NGW9_xA	IF_N1		
	2		::0]	IF_N2		
	9		Rx_NA_ CNTR [2:0]	IF_N3		
	2			IE_N4		
	8			IE_N5		
	6			IE_N6		
	10			LF_N7		
	11		[0:6]	IF_N8		
	12		Rx_NB_CNTR [9:0]	lE [−] N6		
z	13		NB_O	IE_N10		
ATIO	14		Æ,	IF_N11		
COC	15			IF_N12		
R BIT	20 19 18 17 16 15 14 13 12 11 10 9 8	ple		IF_N13		
SHIFT REGISTER BIT LOCATION	17	Data Field		IF_N14		
	18	a	NGW9_xT	IF_N15		
SHIF	19		A_ [2:0]	IF_N16		
	20		Tx_NA_ CNTR [2:0]	TYN_7I		
	21		. 0	IF_N18		
	22					6tN_FI
	23			IF_N20		
	5 24			IF_N21		
	25		[0:6]	IF_N22		
	26		CNTF	IF_N23		
	27		Tx_NB_CNTR [9:0]	IF_N24		
Most Significant Bit	28		<u>\</u>	IE_N25		
nifica	29			IF_N26		
st Sig	30			TSN_7I		
Μŏ	31			1F_N28		

Note: X denotes don't care bit.

2.4.1 3-Bit IF Swallow Counter Divide Ratio (Tx A Counter, Rx A Counter)

Divide Ratio	Tx_NA_CN	ΓR [2:0] or Rx_NA_	_CNTR [2:0]
0	0	0	0
1	0	0	1
•	•	•	•
7	1	1	1

Divide ratio is from 0 to 7

Tx_NB_CNTR ≥ Tx_NA_CNTR and Rx_NB_CNTR ≥ Rx_NA_CNTR

2.4.2 10-Bit IF Programmable Counter Divide Ratio (Tx B Counter, Rx B Counter)

Divide Ratio				Tx_NB_C	NTR [9:0] o	or Rx_NB_C	NTR [9:0]			
3	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	_1	0	0
•	•	•	•	•	•	•		•	•	•
1023	1	1	1	1	1	1	1	1	1	1

Divide ratio is from 3 to 1023 (Divide ratios less than 3 are prohibited)

Tx_NB_CNTR ≥ Tx_NA_CNTR and Rx_NB_CNTR ≥ Rx_NA_CNTR

N = PB + A

B = N div P

 $A = N \mod P$

2.4.3 Tx_PWDN (IF_N[15])

This bit will asynchronously powerdown the Tx PLL when set to one. For normal operation, it should be set to zero.

2.4.4 Rx_PWDN (IF_N[1])

This bit will asynchronously powerdown the Rx PLL when set to one. For normal operation, it should be set to zero.

2.5 RF_R REGISTER

If the ADDRESS [2:0] field is set to 011, data is transferred from the 32-bit shift register into the RF_R register when LE signal goes high. The RF_R register sets the RF PLL's 8-bit R counter divide ratio and various programmable bits. The divide ratio for RF R counter is from 2 to 255.

t Bit	0	ield.	-	
fican	1	ess F	-	
Signi	7	Address Field	0	
Least Significant Bit	3		Λ2X	0H_7R
_	4		TSA_7A	FF_R1
	2		JO9_09_7R	SH_7A
	9			£Я_₹Я
	2		BE_lcbo	PF_R4
	8			2H_7R
	6		[4:0]	9H_7R
	10		_CAL	7A_7A
	11		FRAC_CAL [4:0]	8A_7A
	12		_	6日_국日
_	13		FSTSW1	01A_7A
ATIO	14		SWSTSA	FF_R11
LOC/	15		FSTM1	S1A_7A
R BIT	16	ple	FSTM2	RF_R13
SHIFT REGISTER BIT LOCATION	20 19 18 17 16 15 14 13 12 11 10	Data Field		PF_R14
. REG	18	D	[(81A_7A
SHIFT	19		_CNTR [6:0]	PF_R16
•	20		_CNT	TIA_RA
	21		FSTL	8FH_7F
	22			RF_R19
	26 25 24 23 22 21			RF_R20
	24			RF_R21
	25			RF_R22
	26		[7:0]	RF_R23
	27		NTR	PF_R24
nt Bit	28		RF_R_CNTR [7:0]	RF_R25
Most Significant Bit	30 29		A.	RF_R26
t Sign	30			72A_7A
Mos	31			82A_7A
			Я_ ∃ Я	i

2.5.1 8-Bit RF Programming Reference Divider Ratio (RF R Counter)

Divide Ratio		RF_R_CNTR [7:0]							
2	0	0	0	0	0	0	1	0	
3	0	0	0	0	0	0	1	1	
•	•	•	•	•	•	•	•	•	
255	1	1	1	1	1	1	1	1	

Divide ratio for RF R counter is from 2 to 255.

2.5.2 FSTL_CNTR (RF_R[20]-[14])

The Fastlock Timeout Counter is a 10 bit counter wherein only the seven MSB bits are programmable. (The number of phase

detector cycles the fastlock mode remains in HIGH gain is the binary FSTL_CNTR value loaded multiplied by eight.)

Phase Detect Cycles		FSTL_CNTR [6:0]									
24	0	0	0	0	0	1	1				
32	0	0	0	0	7	0	0				
•	•	•	•	•		•	•				
1008	1	1	1	1	1	1	0				
1016	1	1	1	1	1	1	1				

2.5.3 FSTM (RF_R[13]-[12]) and FSTSW (RF_R[11]-[10])

Fastlock enables the designer to achieve both fast frequency transitions and good phase noise performance by dynamically changing the PLL loop bandwidth. The Fastlock modes allow wide band PLL fast locking with seamless transition to a low phase noise narrow band PLL. Consistent gain and phase margins are maintained by simultaneously changing charge pump current magnitude and loop filter damping resistor. In the LMX3305, the RF fastlock can achieve substantial improvement in lock time by increasing the charge pump current by 4X, 7X or 9X, which causes a 2X, 2.6X or 3X increase in the loop bandwidth respectively. The damping resistors are connected to FSTSW pins.

When bit FSTM2 and/or FSTM1 is set HIGH, the RF fastlock is enabled. As a new frequency is loaded, RF_Sw2 pin and/or RF_Sw1 pin goes to a LOW state to switch in the damping resistors, the RF \mbox{CP}_o is set to a higher gain, and fastlock timeout counter starts counting. Once the timeout counter finishes counting, the PLL returns to its normal operation (the lopo gain is forced to 100 $\mu\mbox{A}$ irrespective of RF_Icpo bits).

When bit FSTM2 and/or FSTM1 is set LOW, pins RF_Sw2 and/or RF_Sw1 can be toggled HIGH or LOW to drive other devices. RF_Sw2 and/or RF_Sw1 can also be set LOW to switch in different damping resistors to change the loop filter performance. FSTSW bits control the output states of the RF_Sw2 and RF_Sw1 pins.

RF_R[12] FSTM1	RF_R[10] FSTSW1	RF_Sw1 Output Function
0	0	RF_Sw1 pin reflects RF_SwBit "0" logic state
0	1	RF_Sw1 pin reflects RF_SwBit "1" logic state
1	х	RF_Sw1 pin LOW while T.O. counter is active

RF_R[13] FSTM2	RF_R[11] FSTSW2	RF_Sw2 Output Function
0	0	RF_Sw2 pin reflects RF_SwBit "0" logic state
0	1	RF_Sw2 pin reflects RF_SwBit "1" logic state
1	х	RF_Sw2 pin LOW while T.O. counter is active

2.5.4 FRAC_CAL (RF_R[9]-[5])

These five bits allow the users to optimize the fractional circuitry, therefore reducing the fractional reference spurs. The MSB bit, RF_R[9], activates the other four calibration bits RF_R[8]-[5]. These four bits can be adjusted to improve frac-

tional spur. Improvements can be made by selecting the bits to be one greater or less than the denominator value. For example, in the 1/16 fractional mode, these four bits can be programmed to 15 or 17. In normal operation, these bits should be set to zero.

2.5.5 RF_lcpo (RF_R[4]-[3])

These two bits set the charge pump gain of the RF PLL. The user is able to set the charge pump gain during the acquisition phase of the fastlock mode to 4X, 7X or 9X.

Charge Pump Gain	RF_R[4]	RF_R[3]
100 μA	0	0
400 μA	0	1
700 μA	1	0
900 μA	1	1

2.5.6 RF_PD_POL (RF_R[2])

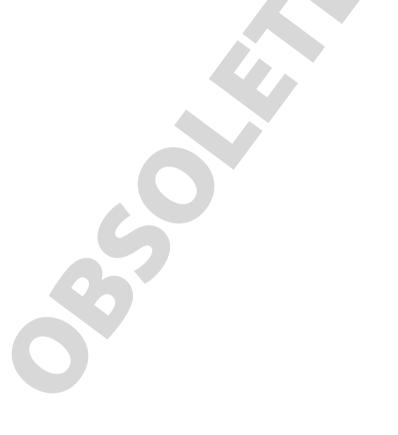
This bit sets the polarity of the RF phase detector. It is set to one when RF VCO characteristics are positive. When RF VCO frequency decreases with increasing control voltage, RF_PD_POL should be set to zero.

2.5.7 RF_RST (RF_R[1])

This bit will reset the RF R and N counters when it is set to one. For normal operation, RF_RST should be set to zero.

2.5.8 V2X (RF_R[0])

V2X when set high enables the voltage doubler for the RF charge pump supply.



2.6 RF_N REGISTER

If the ADDRESS [2:0] field is set to 100, data is transferred from the 32-bit shift register into the RF_N register when LE signal goes high. The RF_N register set the RF PLL's 23-bit fractional N counter and various programmable bits. The fractional N counter consists of 15 bits integer portion and 8 bits fractional portion. The integer portion consists of a 2-bit swallow counter (B word), and a 11-bit programmable counter (C word). The fractional portion consists of a 4-bit numerator and a 4-bit denominator.

	Least Significant Bit	0	Field	0	
	ifican	1	Address Field	0	
	Sign	2	Addı	-	
	east-	3		0]	3F_N0
	1	4		Test [2:0]	3F_N1
		2		Те	3F_N2
		9		RF_PWDN	3F_N3
		7		PCS	3F_N4
		8		Epbs	3F_N5
		6		[(9N_7
		10		FRAC_D [3:0]	ζΝ_ ∃ ξ
		11		JAC_	8N_7F
		12		正	4E_N9
	7	13		[c	3F_N10
,	ATIO	14		FRAC_N [3:0]	3F_N11
	TOC	15			RAC L
	R BIT	16	pja	Ш	3F_N13
,	SHIFT REGISTER BIT LOCATION	20 19 18 17 16 15 14 13 12 11 10	Data Field		3F_N14
	r REG	18	Ď		3F_N15
,	SHIFI	19			3F_N16
	3	20			ZIN_A
		21			SF_N18
,		22		[0]	SF_N19
		23		R [14	3F_N20
		24		CNT	3F_N21
		25		RF_N_CNTR [14:0]	3F_N22
		26			3F_N23
,		27			3F_N24
	int Bi	28			3F_N25
	nifica	29			3F_N26
	Most Significant Bit	30			72N_78
	Mos	31			3F_N28
				F_N	Я

2.6.1 RF_N_CNTR (RF_N[28]-[14])

The RF N counter value is determined by three counter values that work in conjunction with four prescalers. This quadruple modulus prescaler architecture allows lower minimum continuous divide ratios than are possible with a dual modulus prescaler architecture. For the determination of the A, B, and C counter values, the fundamental relationships are shown below.

N = PC + 4B + A

 $C \ge \max \{A,B\} + 2$

The A, B, and C values can be determined as follows:

C = N div P

B = (N - CP) div 4

 $A = (N - CP) \mod 4$

N REGISTER FOR THE CELLULAR (8/9/12/13) PRESCALER OPERATING IN FRACTIONAL MODE

Divide		RF_N_CNTR [14:0]														
Ratio		C Word												B Word A Wo		
1-23		Divide Ratios Less than 24 are impossible since it is required that C ≥ 3														
24-39		Some of these N values are Legal Divide Ratios, some are not														
40	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	
41	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	
16383	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	

N REGISTER FOR THE PCS (16/17/20/21) PRESCALER OPERATING IN FRACTIONAL MODE

Divide		RF_N_CNTF [14:0]													
Ratio		C Word												AW	/ord
1-47		Divide Ratios Less than 48 are impossible since it is required that C ≥ 3													
48-79		Some of these N values are Legal Divide Ratios, some are not													
80	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0
81	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.6.2 FRAC_N (RF_N[13]-[10])

These four bits, the fractional accumulator modulus numera-

tor, set the fractional numerator values in the fraction.

Modulus Numerator		FRAC_	_N [3:0]	
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
•		•	•	•
14	1	1	1	0
15	1	1	1	1

2.6.3 FRAC_D (RF_N[9]-[6])

These four bits, the fractional accumulator modulus denominator, set the fractional denominator from 1/2 to 1/16 resolution

Modulus Denominator	FRAC_D [3:0]									
1-8		Not Allowed								
9	1	1 0 0 1								
10-14	•									
15	1	1	1	1						
16	0	0	0	0						

MODULUS NUMERATOR (FRAC_N) AND DENOMINATOR (FRAC_D) PROGRAMMING

Fractional Numerator						Frac	tional I	Denomi		(FRAC	C_D)					
(FRAC_N)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
RF_N[13]-	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	0000
[10]					<u> </u>				Ļ.,							
0=0000					tions lik	e an in	teger-N	PLL as						i		
1=0001		*	*	*	*	*	*	*	1/9	1/10	1/11	1/12	1/13	1/14	1/15	1/16
		(8/16)	(5/15)	(4/16)	(3/15)		(2/14)	(2/16)			_					
2=0010			*	*	*	*	*	*	2/9	2/10	2/11	2/12	2/13	2/14	2/15	2/16
			•	(8/16)	(6/15)	(4/12)	(4/14)	(4/16)								
0.0011			5)	*	*	*	* .	*	2/0	3/10	0/11	0/10	0/10	0/4.4	0/15	0/10
3=0011				(10/1	(9/15)	(6/12)	(6/14)	(6/16)	3/9	3/10	3/11	3/12	3/13	3/14	3/15	3/16
				6)	(3/13)	(0/12)	(0/14)	(0/10)								
4=0100				0)	*	*	*	*	4/9	4/10	4/11	4/12	4/13	4/14	4/15	4/16
-5155					(12/1	(8/12)	(8/14)	(8/16)	"	" ' '	.,	.,	,,,,	"	"	.,.0
					5)	,	`									
5=0101						*	*	*	5/9	5/10	5/11	5/12	5/13	5/14	5/15	5/16
						(10/1	(10/1	(10/1								
						2)	4)	6)								
6=0110							*	*	6/9	6/10	6/11	6/12	6/13	6/14	6/15	6/16
							(12/1	(12/1								
							4)	6)								
7=0111								*	7/9	7/10	7/11	7/12	7/13	7/14	7/15	7/16
								(14/1								
0.4000	_	D40 F			4.1	•		6)		0/40	0/4.4	0/40	0/40	0/4.4	0/45	0/40
8=1000	, FI	HAC_D	values	betwee	en 1 to	s are no	ot allow	ea.	8/9	8/10	8/11	8/12	8/13	8/14	8/15	8/16
9=1001										9/10	9/11	9/12	9/13	9/14	9/15	9/16
10=1010											10/1	10/1	10/1	10/1	10/1	10/16
											1	2	3	4	5	
11=1011												11/1	11/1	11/1	11/1	11/16
10 1100	-											2	3	4	5	10/10
12=1100													12/1 3	12/1	12/1	12/16
10 1101	-												3	4	5	10/10
13=1101														13/1 4	13/1	13/16
14 1110	-													4	5	14/10
14=1110															14/1	14/16
15 1111	1															15/16
15=1111																15/16

Remark: The *(FRAC_N / FRAC_D) denotes that the fraction number can be represented by (FRAC_N / FRAC_D) as indicated in the parenthesis. For example, 1/2 can be represented by 8/16.

2.6.4 FBPS (RF_N[5])

This bit when set to one will bypass the delay line calculation used in the fractional circuitry. This will improve the phase noise while sacrificing performance on reference spurs. When the bit is set to zero, the delay line circuit is in effect to reduce reference spur.

2.6.5 PCS (RF_N[4])

This bit will determine whether the RF PLL should operate in PCS frequency range or cellular frequency range. When the

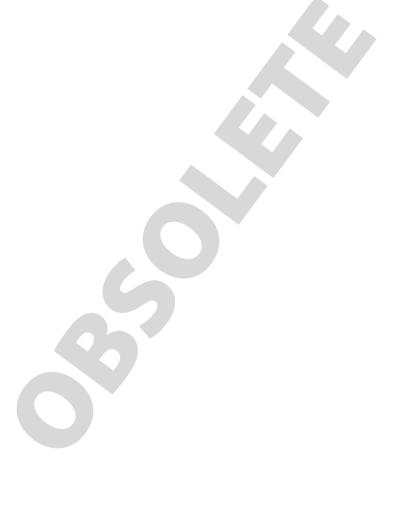
bit is set to one, the RF PLL will operate in the PCS mode and when it is set to zero, the cellular mode.

2.6.6 RF PWDN (RF N[3])

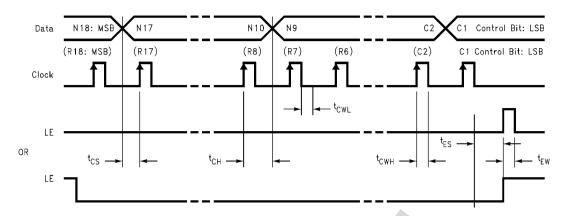
This bit will asynchronously powerdown the RF PLL when set to one. For normal operation, it should be set to zero.

2.6.7 Test (RF_N[2]-[0])

These bits are the internal factory testing only. They should be set to zero for normal operation.



SERIAL DATA INPUT TIMING



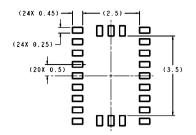
Notes: Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

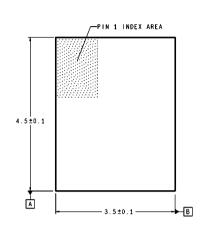
Data is shifted in MSB first.

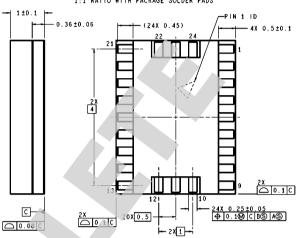
Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{\rm CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 1.84V @ $V_{\rm CC}=2.3V$ and 4.4V @ $V_{\rm CC}=5.5V$.

Physical Dimensions inches (millimeters) unless otherwise noted



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS





DIMENSIONS ARE IN MILLIMETERS

SLB24A (Rev C)

LMX3305 Package Drawing Order Number LMX3305SLBX NS Package Number SLB24A

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