LP324/LP2902 Micropower Quad Operational Amplifier

Check for Samples: LP2902-N, LP324-N

FEATURES

- **Low supply current: 85μA (typ)**
- **Low offset voltage: 2mV (typ)**
- **Low input bias current: 2nA (typ)**
- **Input common mode to GND**
- **Interfaces to CMOS logic**
- **Wide supply range: 3V < V⁺ < 32V**
- **Small Outline Package available**
- **Pin-for-pin compatible with LM324**

DESCRIPTION

The LP324 series consists of four independent, high gain internally compensated micropower operational amplifiers. These amplifiers are specially suited for operation in battery systems while maintaining good input specifications, and extremely low supply current drain. In addition, the LP324 has an input common mode range, and output source range which includes ground, making it ideal in single supply applications.

These amplifiers are ideal in applications which include portable instrumentation, battery backup equipment, and other circuits which require good DC performance and low supply current.

Connection Diagram

Dual-In-Line (N) and SO (M)

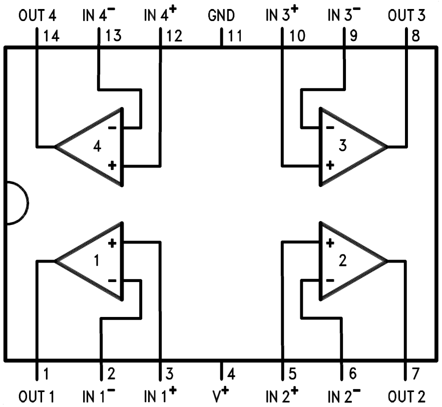


**Figure 1. Order Number LP324M or LP2902M
See NS Package Number M14A
Order Number LP324N or LP2902N
See NS Package Number N14A**

14-Pin TSSOP

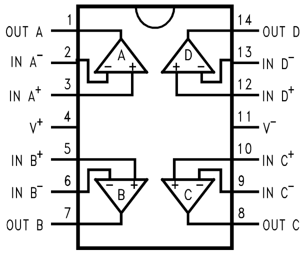
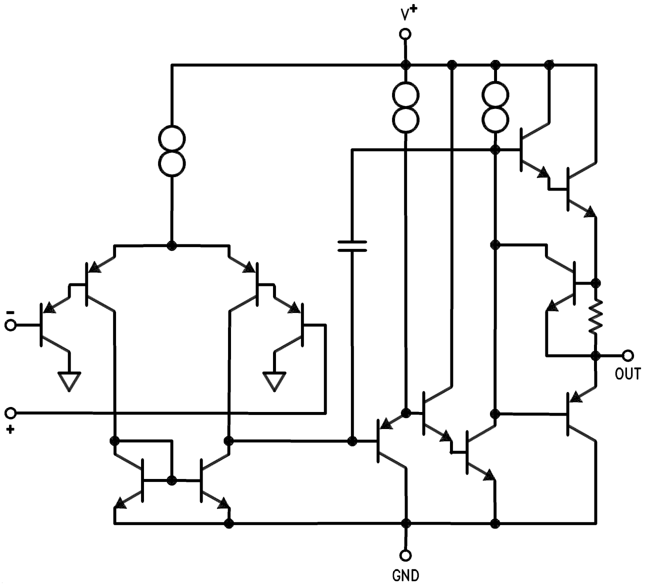


Figure 2. Order Number LP324MT and LP324MTX
See NS Package Number MTC14

Simplified Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

Supply Voltage	
LP324	32V or ± 16V
LP2902	26V or ± 13V
Differential Input Voltage	
LP324	32V
LP2902	26V
Input Voltage [2]	
LP324	−0.3V to 32V
LP2902	−0.3V to 26V
Output Short-Circuit to GND	Continuous
(One Amplifier) [3]	
$V^+ \leq 15V$ and $T_A = 25°C$ ESD Susceptibility [4]	±500V

[1] "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

[2] The input voltage is not allowed to go more than −0.3V below V^- (GND) as this will turn on a parasitic transistor causing large currents to flow through the device.

[3] Short circuits from the output to GND can cause excessive heating and eventual destruction. The maximum sourcing output current is approximately 30 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V_{DC}, continuous short-circuit to GND can exceed the power dissipation ratings (particularly at elevated temperatures) and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

[4] The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Operating Conditions

T_{JMAX}	150°C
θ_{JA} [1]	
MT Package	154°C/W
N Package	90°C/W
M Package	140°C/W
Operating Temp. Range	[2]
Storage Temp. Range	$-65°C \leq T_J \leq 150°C$
Soldering Information	
Wave Soldering(10sec)	260°C(lead temp.)
Convection or Infrared(20sec)	235°C

[1] For operation at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max. $T_J = T_A + \theta_{JA} P_D$.

[2] The LP2902 may be operated from $-40°C \leq T_A \leq +85°C$, and the LP324 may be operated from $0°C \leq T_A \leq +70°C$.

Electrical Characteristics (1)

			LP2902 (2)			LP324			
Symbol	**Parameter**	**Conditions**		**Tested**	**Design**		**Tested**	**Design**	**Units**
			Typ	**Limit**	**Limit**	**Typ**	**Limit**	**Limit**	**Limits**
				(3)	**(4)**		**(3)**	**(4)**	
V_{OS}	Input Offset Voltage		2	4	**10**	2	4	**9**	mV (Max)
I_B	Input Bias Current		2	20	**40**	2	10	**20**	nA (Max)
I_{OS}	Input Offset Current		0.5	4	**8**	0.2	2	**4**	nA (Max)
A_{VOL}	Voltage Gain	R_L = 10k to GND V^+ = 30V	70	40	**30**	100	50	**40**	V/mV (Min)
CMRR	Common Mode Rej. Ratio	V^+ = 30V, 0V ≤ V_{CM} V_{CM} < V^+− 1.5	90	80	**75**	90	80	**75**	dB (Min)
PSRR	Power Supply Rej. Ratio	V^+ = 5V to 30V	90	80	**75**	90	80	**75**	dB (Min)
I_S	Supply Current	R_L = ∞	85	150	**250**	85	150	**250**	μA (Max)
V_O	Output Voltage Swing	I_L = 350μA to GND V_{CM} = 0V	3.6	3.4	**V^+−1.9V**	3.6	3.4	**V^+−1.9V**	V (Min)
		I_L = 350μA to V^+ V_{CM} = 0V	0.7	0.8	**1.0**	0.7	0.8	**1.0**	V (Max)
I_{OUT} Source	Output Source Current	V_O = 3V V_{IN} (diff) = 1V	10	7	**4**	10	7	**4**	mA (Min)
I_{OUT} Sink	Output Sink Current	V_O = 1.5V V_{IN} (diff) = 1V	5	4	**3**	5	4	**3**	mA (Min)
I_{OUT} Sink	Output Sink Current	V_O = 1.5V V_{CM} = 0V	4	2	**1**	4	2	**1**	mA (Min)
I_{SOURCE}	Output Short to GND	V_{IN} (diff) = 1V	20	25 **35**	**35**	20	25 **35**	**35**	mA (Max)
I_{SINK}	Output Short to V^+	V_{IN} (diff) = 1V	15	30	**45**	15	30	**45**	mA (Max)
V_{OS} Drift			10			10			μV/C°
I_{OS} Drift			10			10			pA/C°
GBW	Gain Bandwidth Product		100			100			KHz
SR	Slew Rate		50			50			V/mS

(1) **Boldface** numbers apply at temperature extremes. All other numbers apply only at $T_A = T_J$ = 25°C, V^+ = 5V, V_{cm} = V/2, and R_L =100k connected to GND unless otherwise specified.

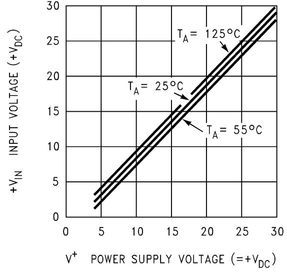
(2) The LP2902 operating supply range is 3V to 26V, and is not tested above 26V.

(3) Guaranteed and 100% production tested.

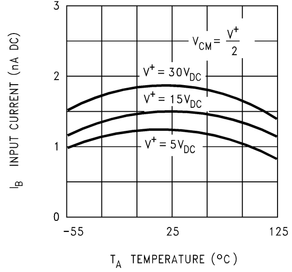
(4) Guaranteed (but not 100% production tested) over the operating supply voltage range (3.0V to 32V for the LP324, LP324, and 3.0V to 26V for the LP2902), and the common mode range (0V to V^+ −1.5V), unless otherwise specified. These limits are not used to calculate outgoing quality levels.

Typical Performance Curves

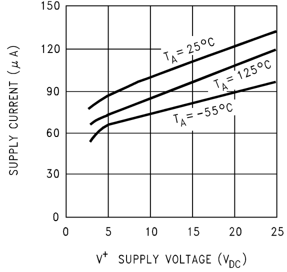
Input Voltage Range



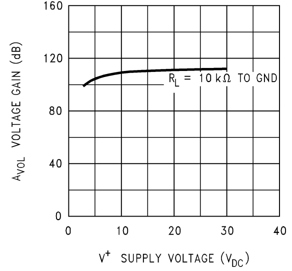
Input Current



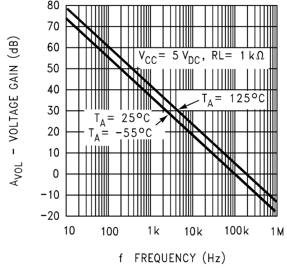
Supply Current



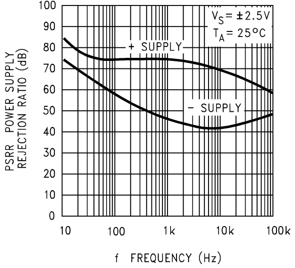
Voltage Gain



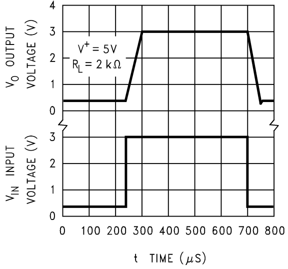
Open Loop Frequency Response



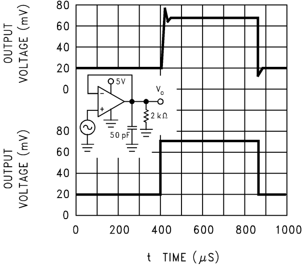
Power Supply Rejection Ratio



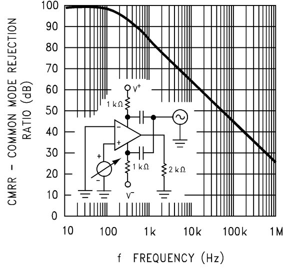
Voltage Follower Pulse Response



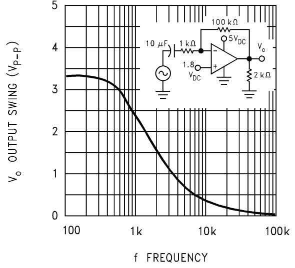
Voltage Follower Pulse Response (Small Signal)



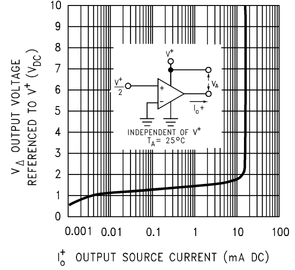
Common Mode Rejection Ratio



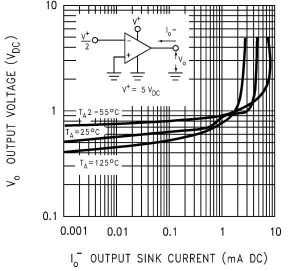
Large Signal Frequency Response



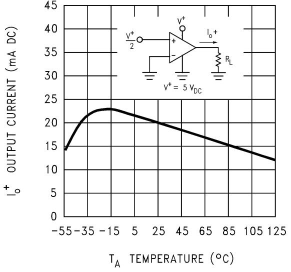
Typical Performance Curves (continued)



Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting

Application Hints

The LP324 series is a micro-power pin-for-pin equivalent to the LM324 op amps. Power supply current, input bias current, and input offset current have all been reduced by a factor of 10 over the LM324. Like its predecessor, the LP324 series op amps can operate on single supply, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or the unit is not inadvertently installed backwards in the test socket as an unlimited current surge through the resulting forward diode within the IC could destroy the unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

The amplifiers have a class B output stage which allows the amplifiers to both source and sink output currents. In applications where crossover distortion is undesirable, a resistor should be used from the output of the amplifier to ground. The resistor biases the output into class A operation.

The LP324 has improved stability margin for driving capacitive loads. No special precautions are needed to drive loads in the 50 pF to 1000 pF range. It should be noted however that since the power supply current has been reduced by a factor of 10, so also has the slew rate and gain bandwidth product. This reduction can cause reduced performance in AC applications where the LM324 is being replaced by an LP324. Such situations usually occur when the LM324 has been operated near its power bandwidth.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example: If all four amplifiers were simultaneously shorted to ground on a 10V supply the junction temperature would rise by 110°C.

Exceeding the negative common-mode limit on either input will cause a reversal of phase to the output and force the amplifier to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a low state. In neither case does a latch occur since returning the input within the common mode range puts the input stage and thus the amplifier in a normal operating mode.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference to $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Figure 3. Driving CMOS

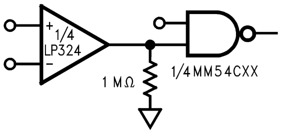


Figure 4. Comparator with Hysteresis

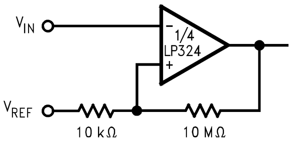


Figure 5. Non-Inverting Amplifier

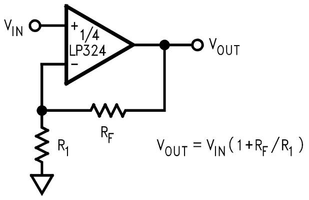


Figure 6. Adder/Subtractor

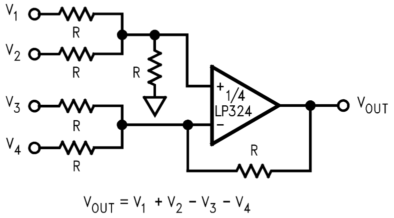


Figure 7. Unity Gain Buffer

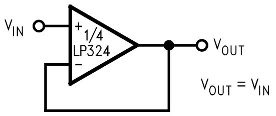


Figure 8. Positive Integrator

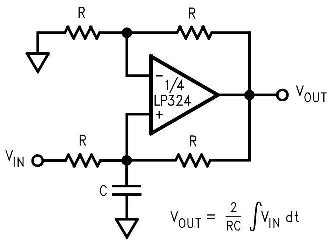


Figure 9. Differential Integrator

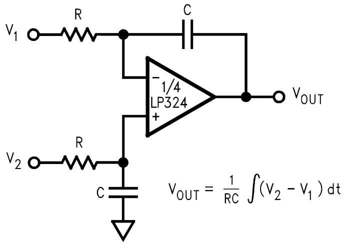


Figure 10. Howland Current Pump

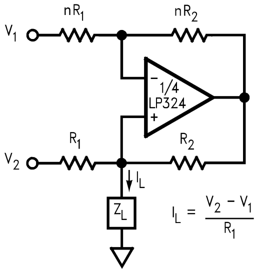


Figure 11. Bridge Current Amplifier

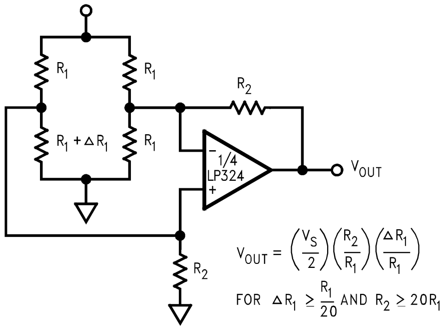


Figure 12. μ Power Current Source

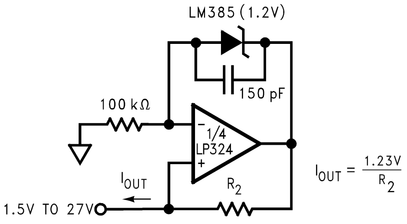


Figure 13. Lowpass Filter

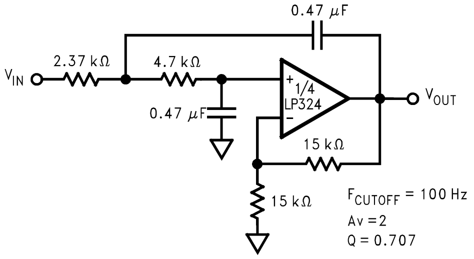


Figure 14. 1 kHz Bandpass Active Filter

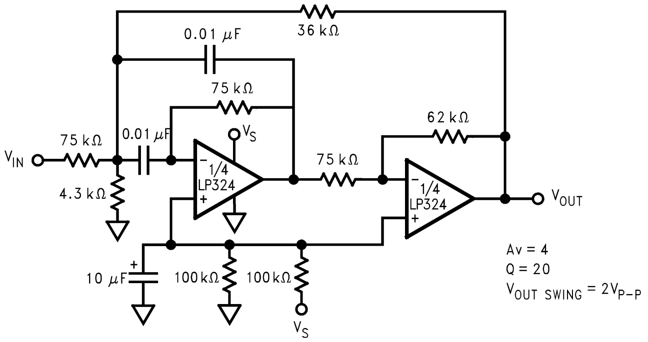


Figure 15. Band-Reject Filter

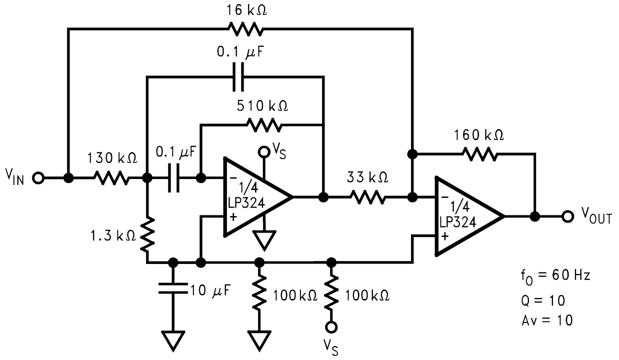


Figure 16. Pulse Generator

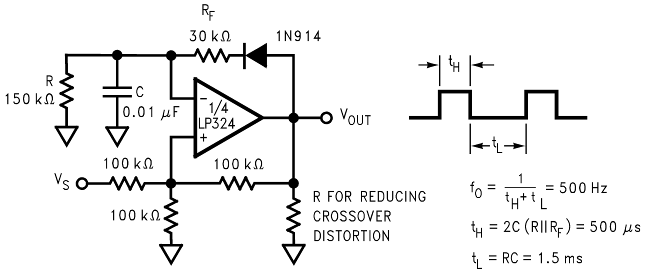
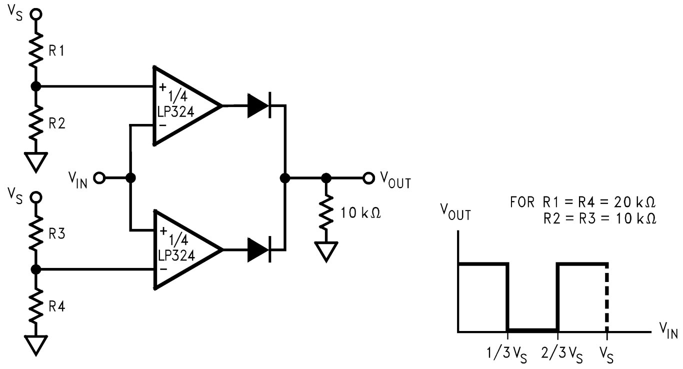


Figure 17. Window Comparator



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LP2902M	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	
LP2902M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP2902MX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LP2902MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP2902N/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	
LP2902N/PB	ACTIVE	PDIP	NFF	14	25	TBD	CU SNPB	Level-1-NA-UNLIM	
LP324M	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	
LP324M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP324MT	ACTIVE	TSSOP	PW	14	94	TBD	CU SNPB	Level-1-260C-UNLIM	
LP324MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP324MTX	ACTIVE	TSSOP	PW	14	2500	TBD	CU SNPB	Level-1-260C-UNLIM	
LP324MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP324MX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LP324MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP324N/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	
LP324N/PB	ACTIVE	PDIP	NFF	14	25	TBD	CU SNPB	Level-1-NA-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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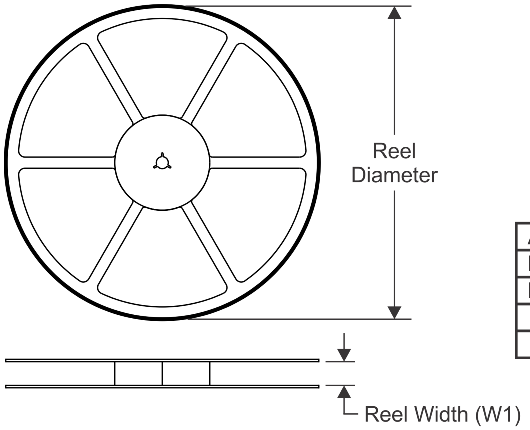
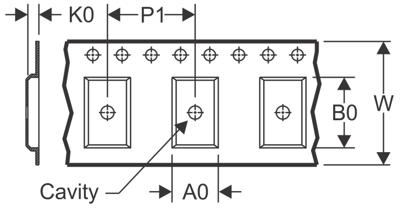
TAPE AND REEL INFORMATION

REEL DIMENSIONS

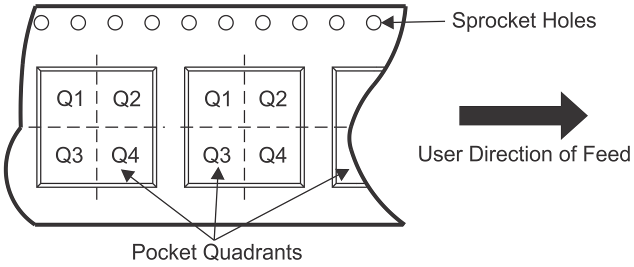


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

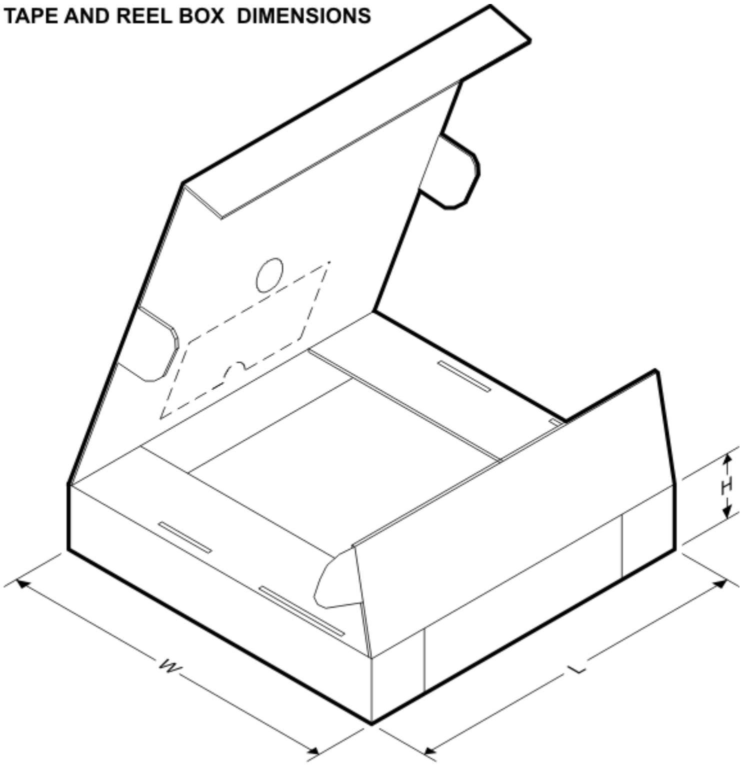
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2902MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LP2902MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LP324MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LP324MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LP324MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LP324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2902MX	SOIC	D	14	2500	349.0	337.0	45.0
LP2902MX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0
LP324MTX	TSSOP	PW	14	2500	349.0	337.0	45.0
LP324MTX/NOPB	TSSOP	PW	14	2500	349.0	337.0	45.0
LP324MX	SOIC	D	14	2500	349.0	337.0	45.0
LP324MX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0

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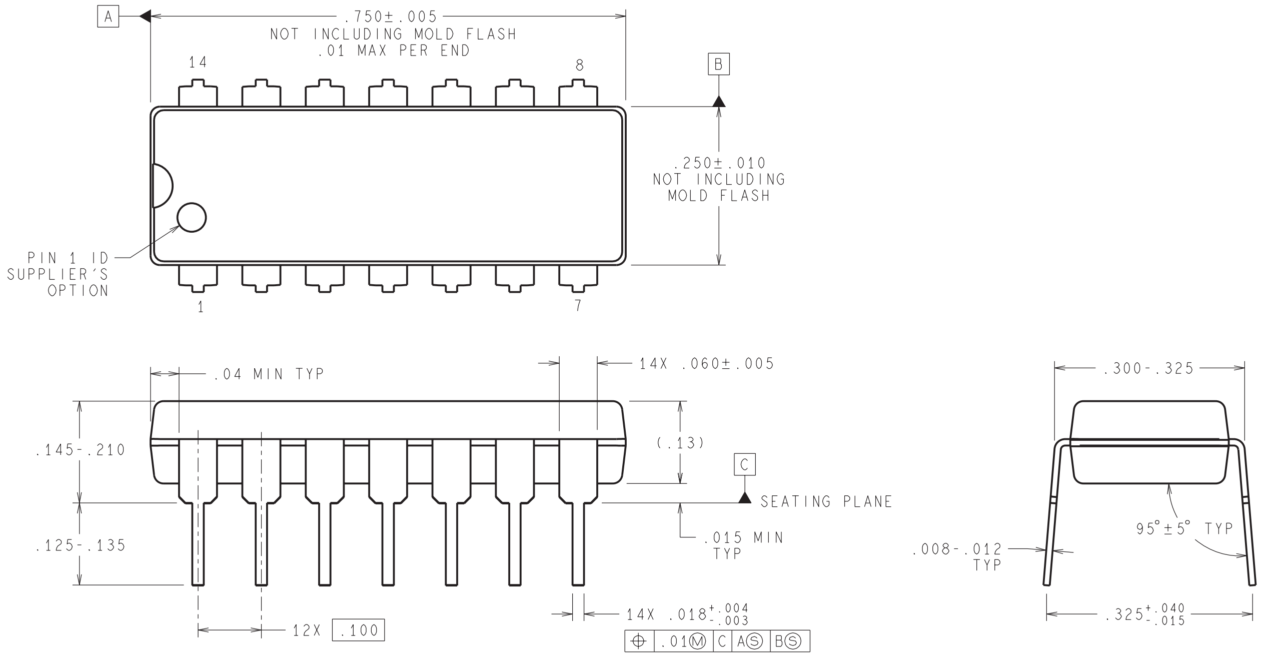
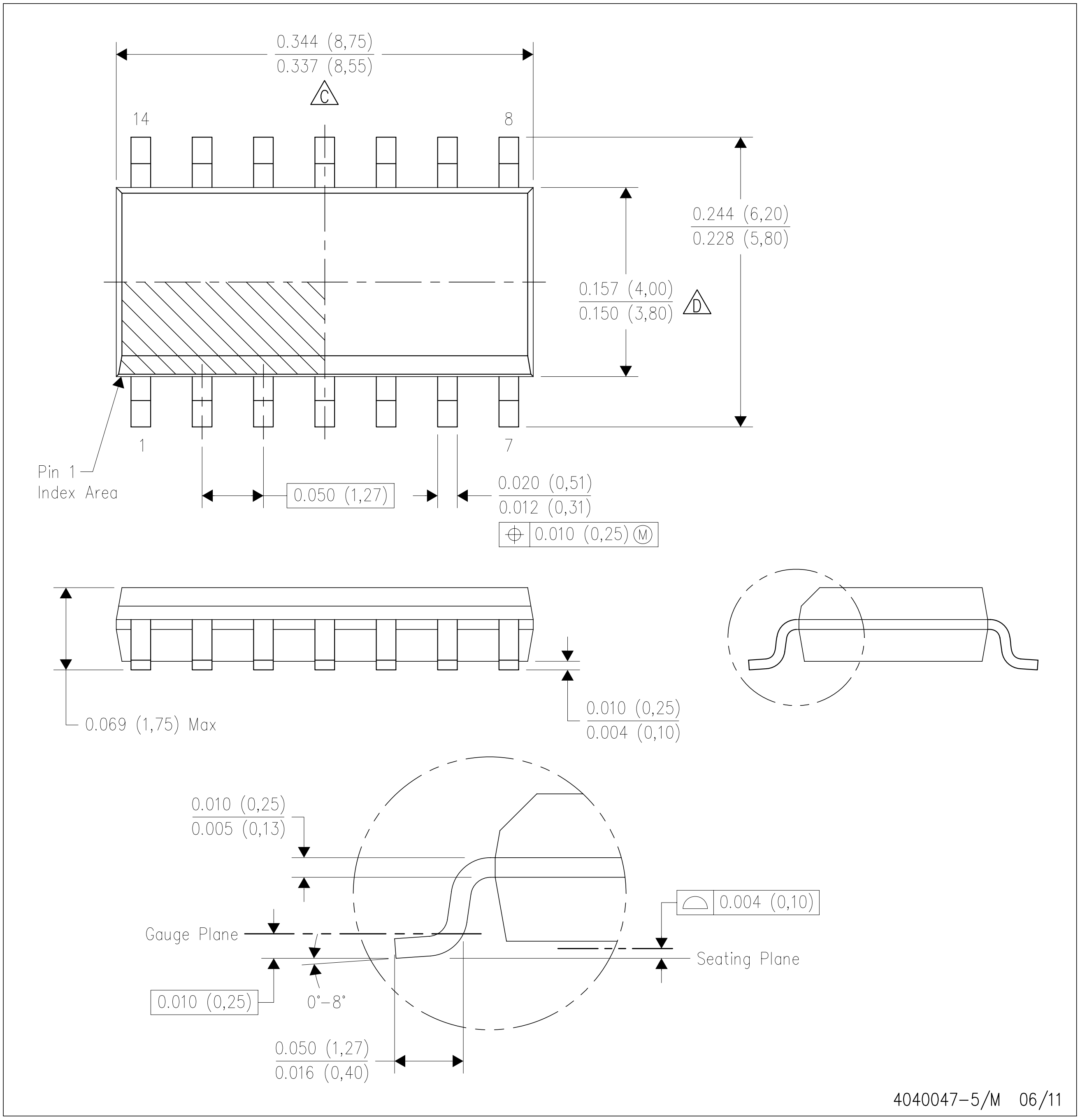


DIMENSIONS ARE IN INCHES

DIMENSIONS IN ( ) FOR REFERENCE ONLY

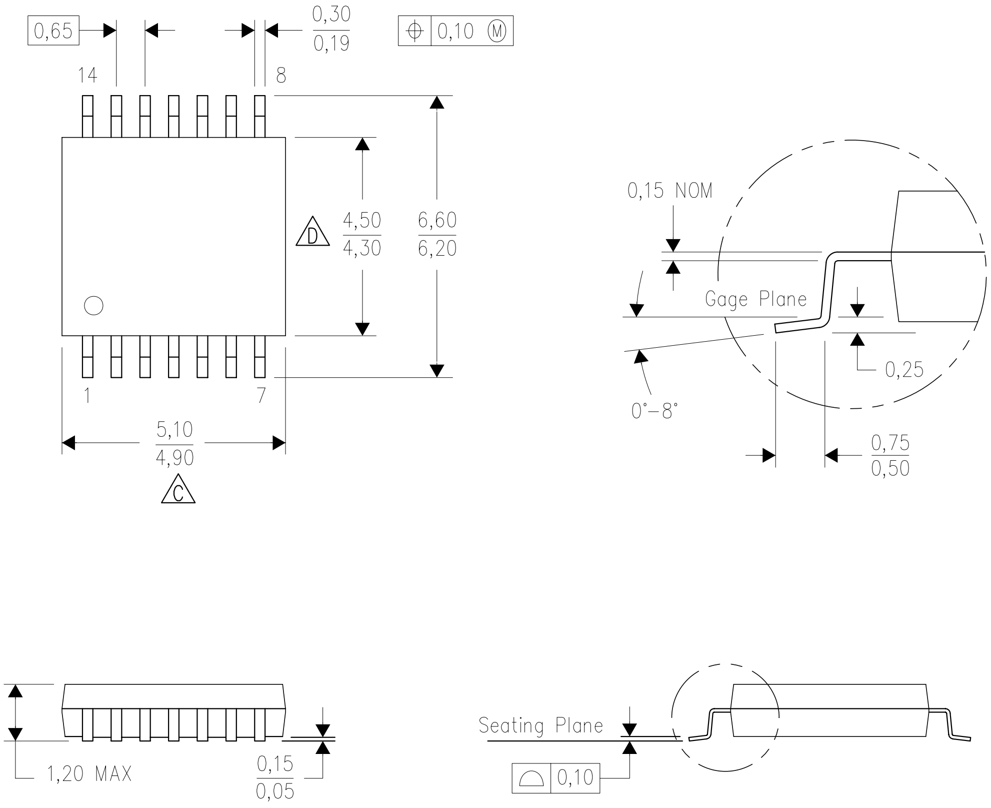
N14A (Rev G)

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

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