LP3883 3A Fast-Response Ultra Low Dropout Linear Regulators

Check for Samples: LP3883

FEATURES

- **Ultra Low Dropout Voltage (210 mV @ 3A typ)**
- **Low Ground Pin Current**
- **Load Regulation of 0.04%/A**
- **60 nA Typical Quiescent Current in Shutdown**
- **1.5% Output Accuracy (25°C)**
- **TO-220, DDPAK/TO-263 Packages**
- **Over Temperature/over Current Protection**
- **−40°C to +125°C Junction Temperature Range**

APPLICATIONS

- **DSP Power Supplies**
- **Server Core and I/O Supplies**
- **Linear Power Supplies for PC Add-in-Cards**
- **Set-Top Box Power Supplies**
- **Microprocessor Power Supplies**
- **High Efficiency Linear Power Supplies**
- **SMPS Post-Regulators**

DESCRIPTION

The LP3883 is a high-current, fast-response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in TO-220 and DDPAK/TO-263 packages.

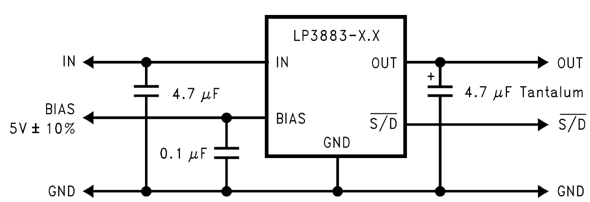
Dropout Voltage: 210 mV (typ) @ 3A load current.

Ground Pin Current: 3 mA (typ) at full load.

Shutdown Current: 60 nA (typ) when S/D pin is low.

Precision Output Voltage: 1.5% room temperature accuracy.

Typical Application Circuit



At least 4.7 µF of input and output capacitance is required for stability.

Connection Diagram

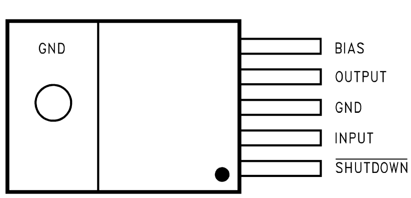


Figure 1. TO-220, Top View
See NDH0005D Package

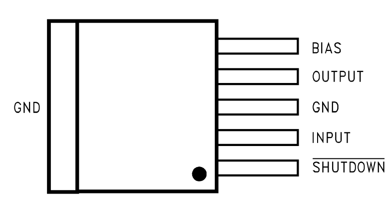
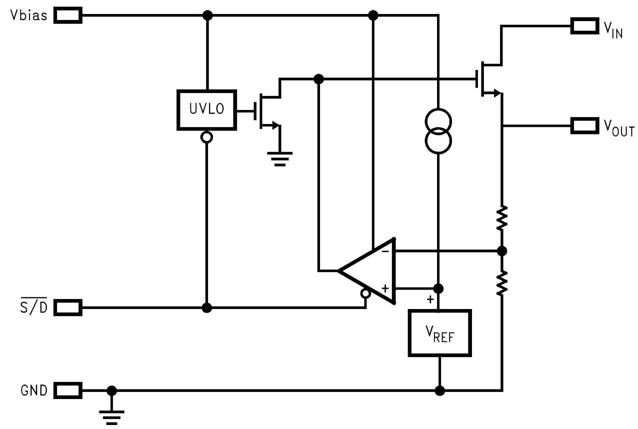


Figure 2. DDPAK/TO-263, Top View
See KTT0005B Package

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Storage Temperature Range		−65°C to +150°C
Lead Temp. (Soldering, 5 seconds)		260°C
ESD Rating	Human Body Model(3)	2 kV
	Machine Model(4)	200V
Power Dissipation(5)		Internally Limited
V_{IN} Supply Voltage (Survival)		−0.3V to +6V
V_{BIAS} Supply Voltage (Survival)		−0.3V to +7V
Shutdown Input Voltage (Survival)		−0.3V to +7V
I_{OUT} (Survival)		Internally Limited
Output Voltage (Survival)		−0.3V to +6V
Junction Temperature		−40°C to +150°C

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.
(4) The machine model is a 220 pF capacitor discharged directly into each pin. The machine model ESD rating of pin 5 is 100V.
(5) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values. $\theta_{J\text{-}A}$ for TO-220 devices is 65°C/W if no heatsink is used. If the TO-220 device is attached to a heatsink, a $\theta_{J\text{-}S}$ value of 4°C/W can be assumed. $\theta_{J\text{-}A}$ for DDPAK/TO-263 devices is approximately 40°C/W if soldered down to a copper plane which is at least 1.5 square inches in area. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

Operating Ratings

V_{IN} Supply Voltage	(V_{OUT} + V_{DO}) to 5.5V
Shutdown Input Voltage	0 to +6V
I_{OUT}	3A
Operating Junction Temperature Range	−40°C to +125°C
V_{BIAS} Supply Voltage	4.5V to 6V

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V_{IN} = V_O(NOM) + 1V, V_{BIAS} = 4.5V, I_L = 10 mA, C_{IN} = C_{OUT} = 4.7 µF, $V_{S/D}$ = V_{BIAS}.

Symbol	Parameter	Conditions	Typical[1]	MIN[2]	MAX[2]	Units
V_O	Output Voltage Tolerance	10 mA < I_L < 3A V_O(NOM) + 1V ≤ V_{IN} ≤ 5.5V 4.5V ≤ V_{BIAS} ≤ 6V	1.216	1.198 **1.186**	1.234 **1.246**	V
			1.5	1.478 **1.455**	1.522 **1.545**	
			1.8	1.773 **1.746**	1.827 **1.854**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation[3]	V_O(NOM) + 1V ≤ V_{IN} ≤ 5.5V	0.01			%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation[4]	10 mA < I_L < 3A	0.04 **0.06**			%/A
V_{DO}	Dropout Voltage[5]	I_L = 3A	210		270 **420**	mV
$I_Q(V_{IN})$	Quiescent Current Drawn from V_{IN} Supply	10 mA < I_L < 3A	3		7 **8**	mA
		$V_{\overline{S/D}}$ ≤ 0.3V	0.03		1 **30**	µA
$I_Q(V_{BIAS})$	Quiescent Current Drawn from V_{BIAS} Supply	10 mA < I_L < 3A	1		2 **3**	mA
		$V_{\overline{S/D}}$ ≤ 0.3V	0.03		1 **30**	µA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V	6			A
Shutdown Input						
V_{SDT}	Output Turn-off Threshold	Output = ON	0.7	**1.3**		V
		Output = OFF	0.7		**0.3**	
Td (OFF)	Turn-OFF Delay	R_{LOAD} X C_{OUT} << Td (OFF)	20			µs
Td (ON)	Turn-ON Delay	R_{LOAD} X C_{OUT} << Td (ON)	15			
$I_{\overline{S/D}}$	$\overline{S/D}$ Input Current	$V_{\overline{S/D}}$ =1.3V	1			µA
		$V_{\overline{S/D}}$ ≤ 0.3V	−1			
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	V_{IN} = V_{OUT} +1V, f = 120 Hz	80			dB
		V_{IN} = V_{OUT} + 1V, f = 1 kHz	65			
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	V_{BIAS} = V_{OUT} + 3V, f = 120 Hz	70			
		V_{BIAS} = V_{OUT} + 3V, f = 1 kHz	65			
	Output Noise Density	f = 120 Hz	1			µV/root−Hz
e_n	Output Noise Voltage V_{OUT} = 1.8V	BW = 10 Hz − 100 kHz	150			µV (rms)
		BW = 300 Hz − 300 kHz	90			

(1) Typical numbers represent the most likely parametric norm for 25°C operation.
(2) Limits are guaranteed through testing, statistical correlation, or design.
(3) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(4) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
(5) Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value.

Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7µF, Cin = 4.7µF, $\overline{S/D}$ pin is tied to V_{BIAS}, V_{IN} = 2.2V, V_{OUT} = 1.8V.

Dropout vs I_L

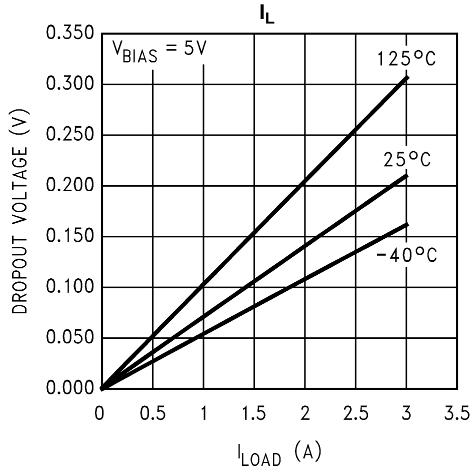


Figure 3.

I_{GND} vs VSD

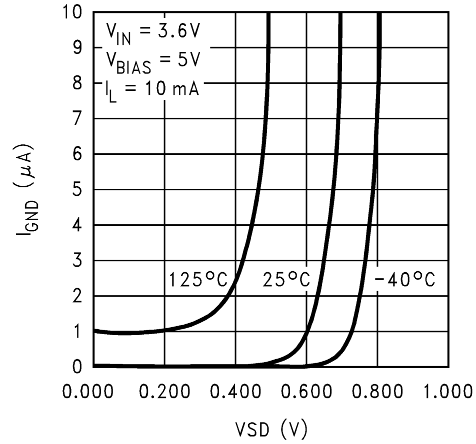


Figure 4.

V_{OUT} vs Temperature

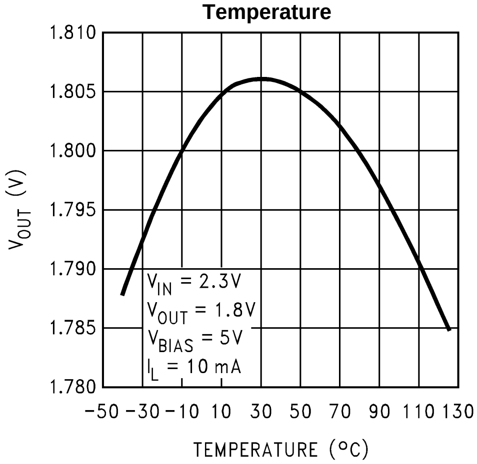


Figure 5.

DC Load Regulation

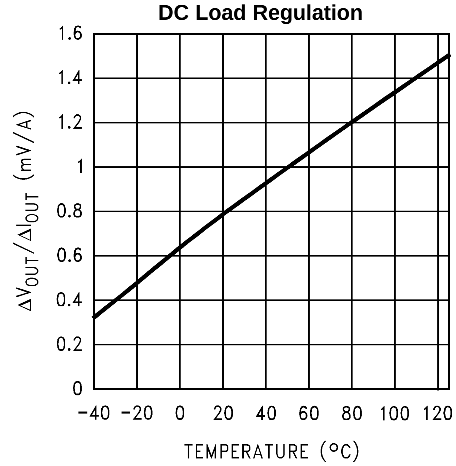


Figure 6.

Line Regulation vs V_{IN}

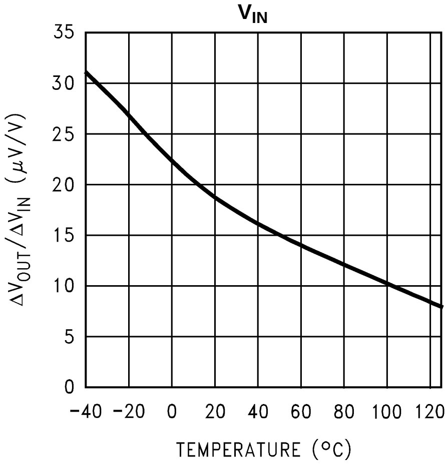


Figure 7.

Line Regulation vs V_{BIAS}

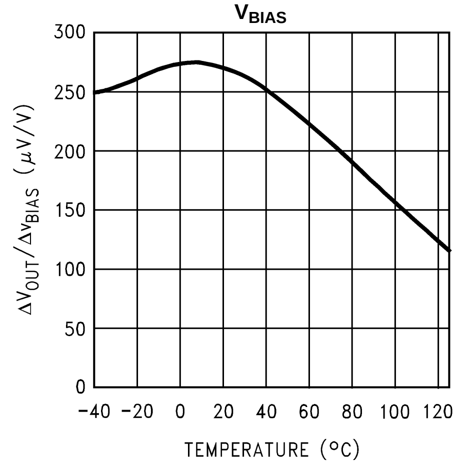


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7µF, Cin = 4.7µF, $\overline{S/D}$ pin is tied to V_{BIAS}, V_{IN} = 2.2V, V_{OUT} = 1.8V.

I_{BIAS} vs I_L

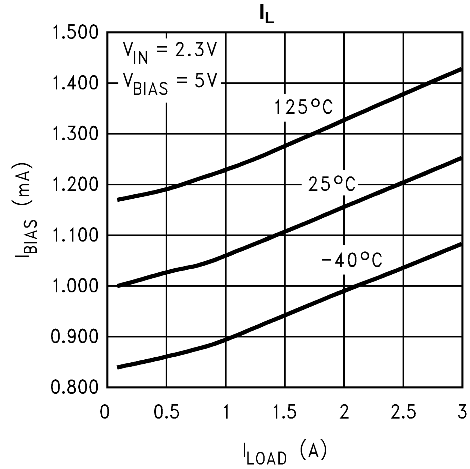


Figure 9.

I_{BIAS} vs V_{BIAS}

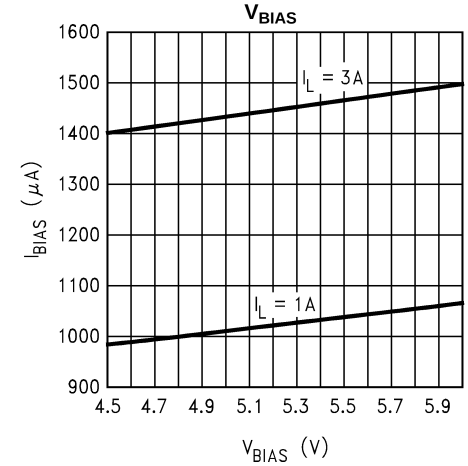


Figure 10.

I_{GND} vs VSD

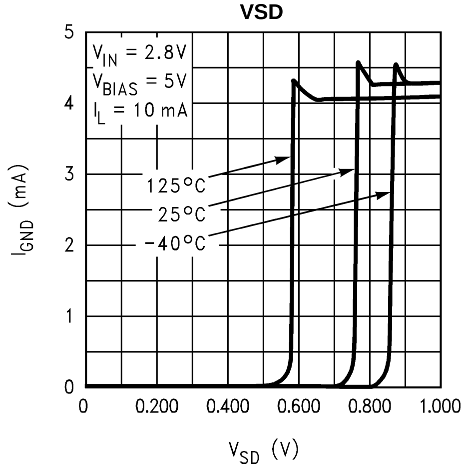


Figure 11.

Noise Measurement

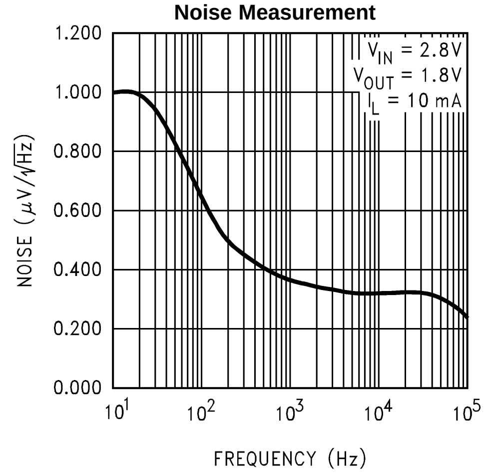


Figure 12.

V_{OUT} Startup Waveform

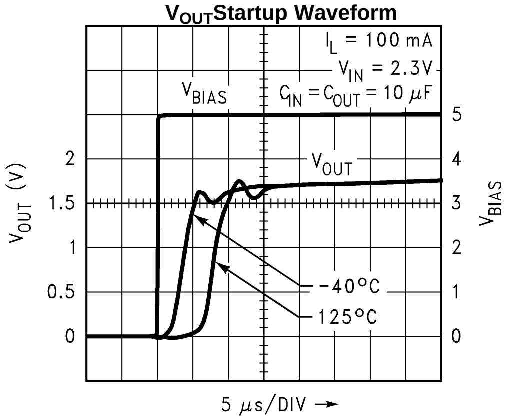


Figure 13.

V_{OUT} Startup Waveform

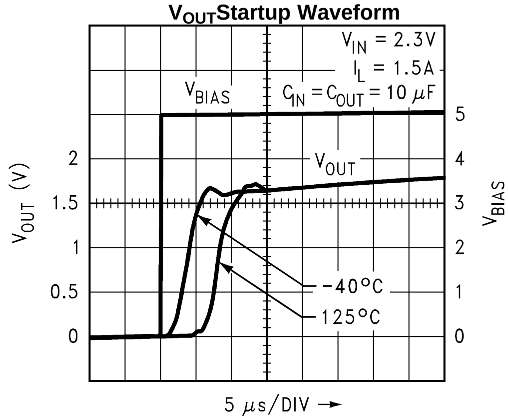


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7µF, Cin = 4.7µF, $\overline{S/D}$ pin is tied to V_{BIAS}, V_{IN} = 2.2V, V_{OUT} = 1.8V.

V_{OUT}Startup Waveform

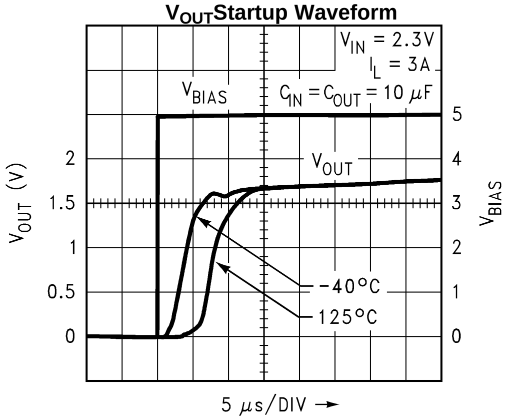


Figure 15.

Line Regulation vs V_{BIAS}

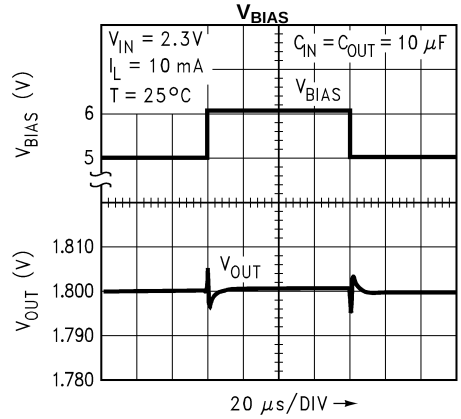


Figure 16.

Line Regulation vs V_{BIAS}

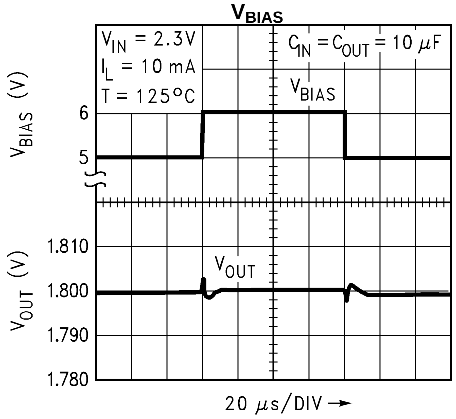


Figure 17.

V_{IN} PSRR

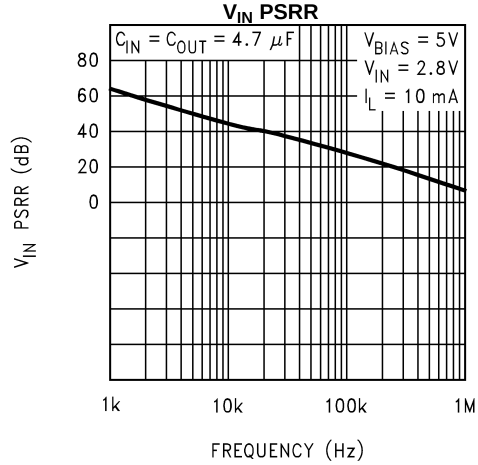


Figure 18.

V_{IN} PSRR

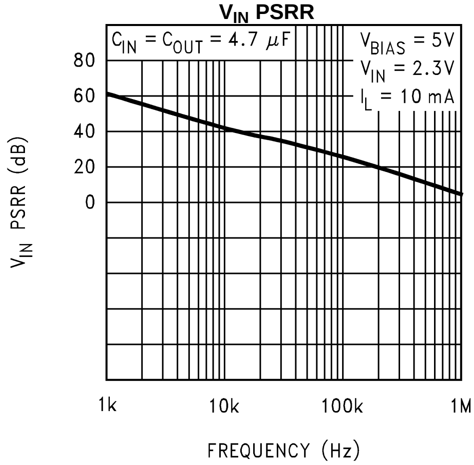


Figure 19.

V_{BIAS} PSRR

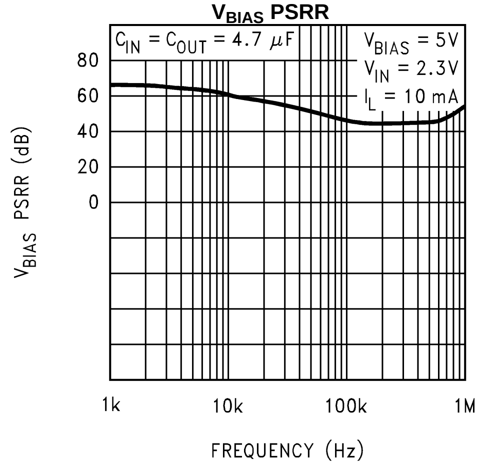


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7µF, Cin = 4.7µF, $\overline{S/D}$ pin is tied to V_{BIAS}, V_{IN} = 2.2V, V_{OUT} = 1.8V.

Load Transient Response (Both Oscon 10µF/3A)

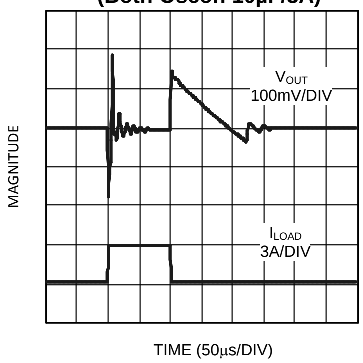


Figure 21.

Load Transient Response (Both Oscon 100µF/3A)

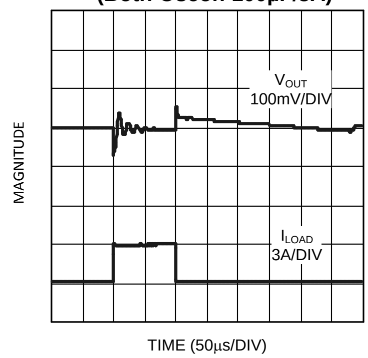


Figure 22.

Load Transient Response (Both POSCAP 100µF/3A)

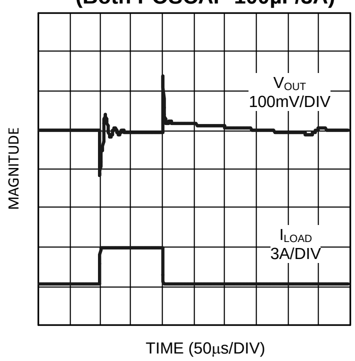


Figure 23.

Load Transient Response (SANYO 150µF/3A)

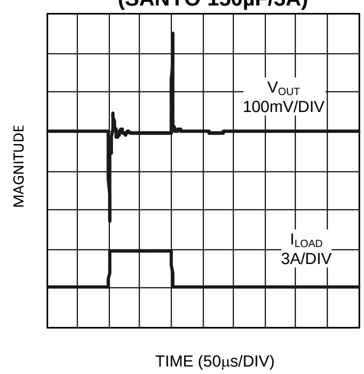


Figure 24.

Load Transient Response (Tantalum 10µF/3A)

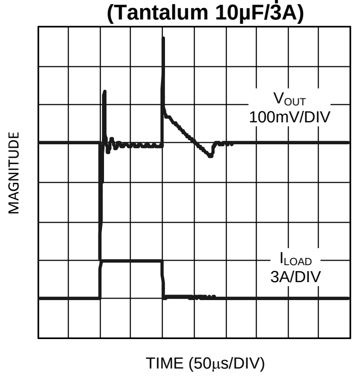


Figure 25.

Load Transient Response (Tantalum 100µF/3A)

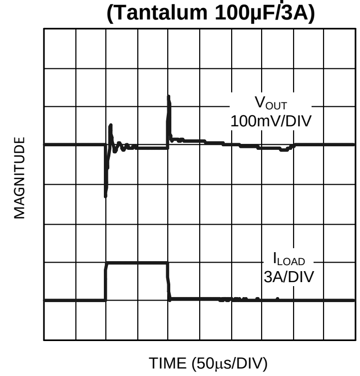


Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 4.7µF, Cin = 4.7µF, $\overline{S/D}$ pin is tied to V_{BIAS}, V_{IN} = 2.2V, V_{OUT} = 1.8V.

Load Transient Response (Both Oscon 10µF/1A)

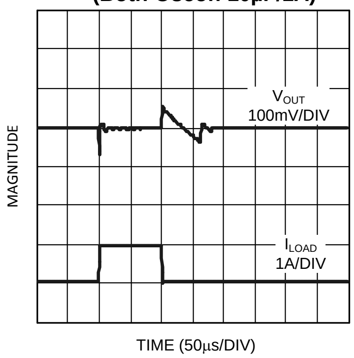


Figure 27.

Load Transient Response (Both Oscon 100µF/1A)

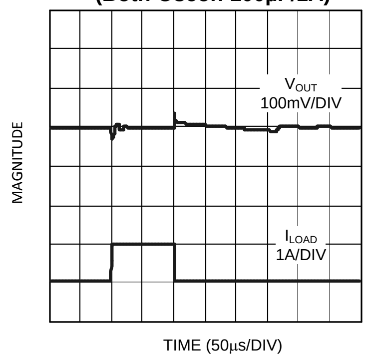


Figure 28.

Load Transient Response (Both POSCAP 100µF/1A)

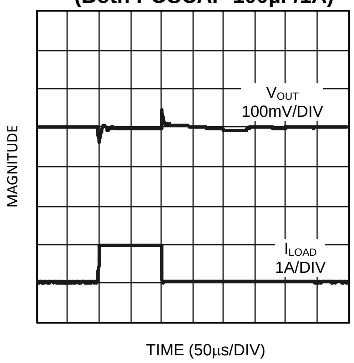


Figure 29.

Load Transient Response (SANYO 150µF/1A)

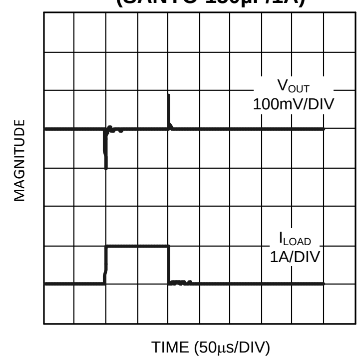


Figure 30.

Load Transient Response (Tantalum 10µF/1A)

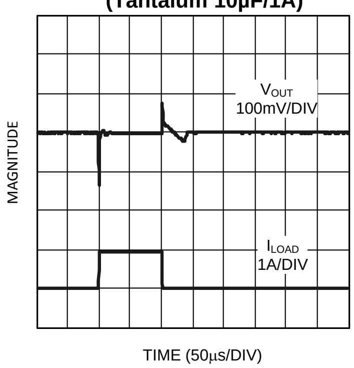


Figure 31.

Load Transient Response (Tantalum 100µF/1A)

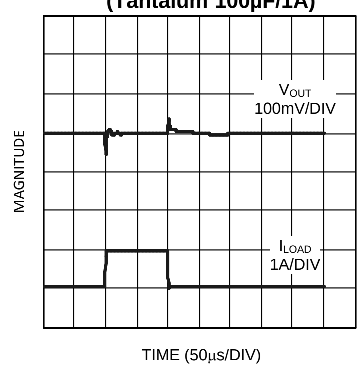


Figure 32.

APPLICATION HINTS

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

OUTPUT CAPACITOR

At least 4.7µF of output capacitance is required for stability (the amount of capacitance can be increased without limit). The output capacitor must be located less than 1 cm from the output pin of the IC and returned to a clean analog ground. The ESR (equivalent series resistance) of the output capacitor must be within the "stable" range as shown in the graph below over the full operating temperature range for stable operation.

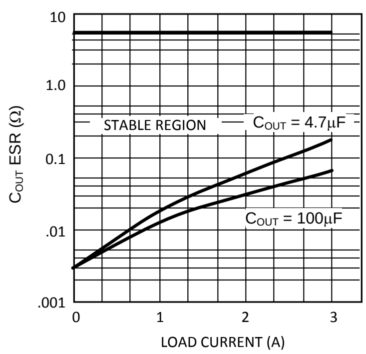


Figure 33. Minimum ESR vs Output Load Current

Tantalum capacitors are recommended for the output as their ESR is ideally suited to the part's requirements and the ESR is very stable over temperature. Aluminum electrolytics are not recommended because their ESR increases very rapidly at temperatures below 10C. Aluminum caps can only be used in applications where lower temperature operation is not required.

A second problem with Al caps is that many have ESR's which are only specified at low frequencies. The typical loop bandwidth of a linear regulator is a few hundred kHz to several MHz. If an Al cap is used for the output cap, it must be one whose ESR is specified at a frequency of 100 kHz or more.

Because the ESR of ceramic capacitors is only a few milli Ohms, they are not suitable for use as output capacitors on LP388X devices. The regulator output can tolerate ceramic capacitance totaling up to 15% of the amount of Tantalum capacitance connected from the output to ground.

OUTPUT "BYPASS" CAPACITORS

Many designers place small value "bypass" capacitors at various circuit points to reduce noise. Ceramic capacitors in the value range of about 1000pF to 0.1µF placed directly on the output of a PNP or P-FET LDO regulator can cause a loss of phase margin which can result in oscillations, even when a Tantalum output capacitor is in parallel with it. This is not unique to National Semiconductor LDO regulators, it is true of any P-type LDO regulator.

The reason for this is that PNP or P-FET regulators have a higher output impedance (compared to an NPN regulator), which results in a pole-zero pair being formed by every different capacitor connected to the output.

The zero frequency is approximately:

$$F_z = 1 / (2 \times \pi \times ESR \times C) \quad (1)$$

where

- ESR is the equivalent series resistance of the capacitor
- C is the value of capacitance

The pole frequency is:

$F_p = 1 / (2 \times \pi \times R_L \times C)$

where

- R_L is the load resistance connected to the regulator output (2)

To understand why a small capacitor can reduce phase margin: assume a typical LDO with a bandwidth of 1MHz, which is delivering 0.5A of current from a 2.5V output (which means R_L is 5 Ohms). We then place a .047 µF capacitor on the output. This creates a pole whose frequency is:

$F_p = 1 / (2 \times \pi \times 5 \times .047 \times 10E\text{-}6) = 677\ kHz$ (3)

This pole would add close to 60 degrees of phase lag at the crossover (unity gain) frequency of 1 MHz, which would almost certainly make this regulator oscillate. Depending on the load current, output voltage, and bandwidth, there are usually values of small capacitors which can seriously reduce phase margin. If the capacitors are ceramic, they tend to oscillate more easily because they have very little internal inductance to damp it out. If bypass capacitors are used, it is best to place them near the load and use trace inductance to "decouple" them from the regulator output.

INPUT CAPACITOR

The input capacitor must be at least 4.7 µF, but can be increased without limit. It's purpose is to provide a low source impedance for the regulator input. Ceramic capacitors work best for this, but Tantalums are also very good. There is no ESR limitation on the input capacitor (the lower, the better). Aluminum electrolytics can be used, but their ESR increase very quickly at cold temperatures. They are not recommended for any application where temperatures go below about 10°C.

BIAS CAPACITOR

The 0.1µF capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 6V to assure proper operation of the part.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 4V.

SHUTDOWN OPERATION

Pulling down the shutdown ($\overline{S/D}$) pin will turn-off the regulator. Pin $\overline{S/D}$ must be actively terminated through a pull-up resistor (10 kΩ to 100 kΩ) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

POWER DISSIPATION/HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$P_D = (V_{IN} - V_{OUT}) I_{OUT} + (V_{IN}) I_{GND}$

where

- I_{GND} is the operating ground current of the device (4)

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$T_{Rmax} = T_{Jmax} - T_{Amax}$ (5)

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D \quad (6)$$

These parts are available in TO-220 and DDPAK/TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 60 °C/W for TO-220 package and ≥ 60 °C/W for DDPAK/TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

HEATSINKING TO-220 PACKAGE

The thermal resistance of a TO220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for TO263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$$\theta_{HA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC}. \quad (7)$$

In this equation, θ_{CH} is the thermal resistance from the case to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. θ_{JC} is about 3°C/W for a TO220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

HEATSINKING DDPAK/TO-263 PACKAGE

The DDPAK/TO-263 package uses the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. The graph below shows a curve for the θ_{JA} of DDPAK/TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

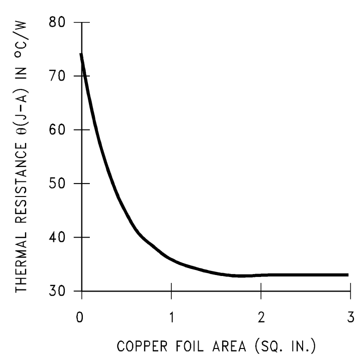


Figure 34. θ_{JA} vs Copper (1 Ounce) Area for DDPAK/TO-263 package

As shown in the graph below, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

Figure 35 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

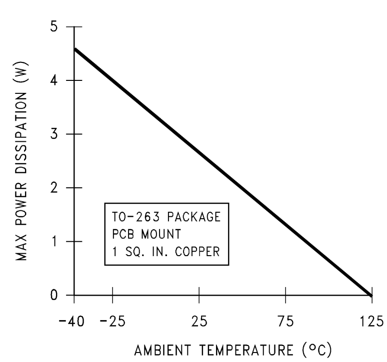


Figure 35. Maximum power dissipation vs ambient temperature for DDPAK/TO-263 package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP3883ES-1.2	ACTIVE	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3883ES -1.2	Samples
LP3883ES-1.2/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3883ES -1.2	Samples
LP3883ES-1.5	ACTIVE	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3883ES -1.5	Samples
LP3883ES-1.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3883ES -1.5	Samples
LP3883ESX-1.2	ACTIVE	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LP3883ES -1.2	Samples
LP3883ESX-1.2/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3883ES -1.2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION

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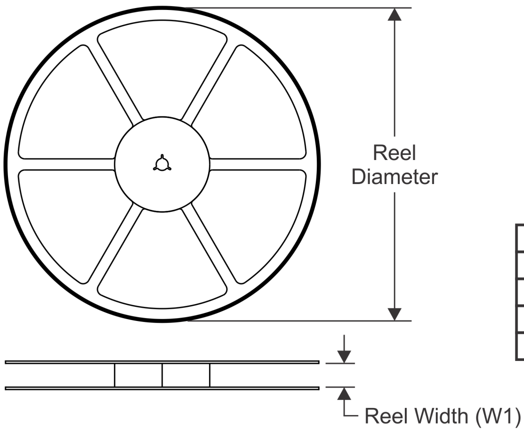
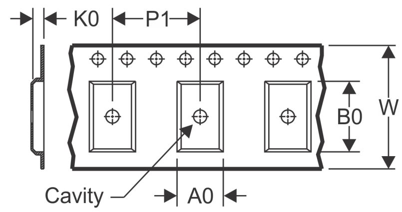
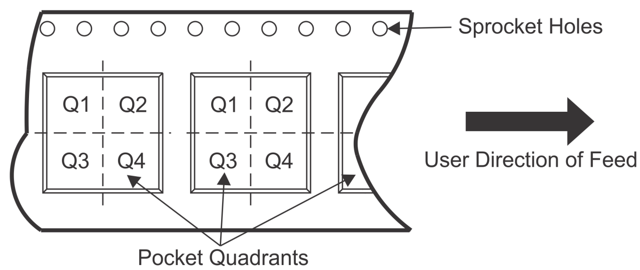


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

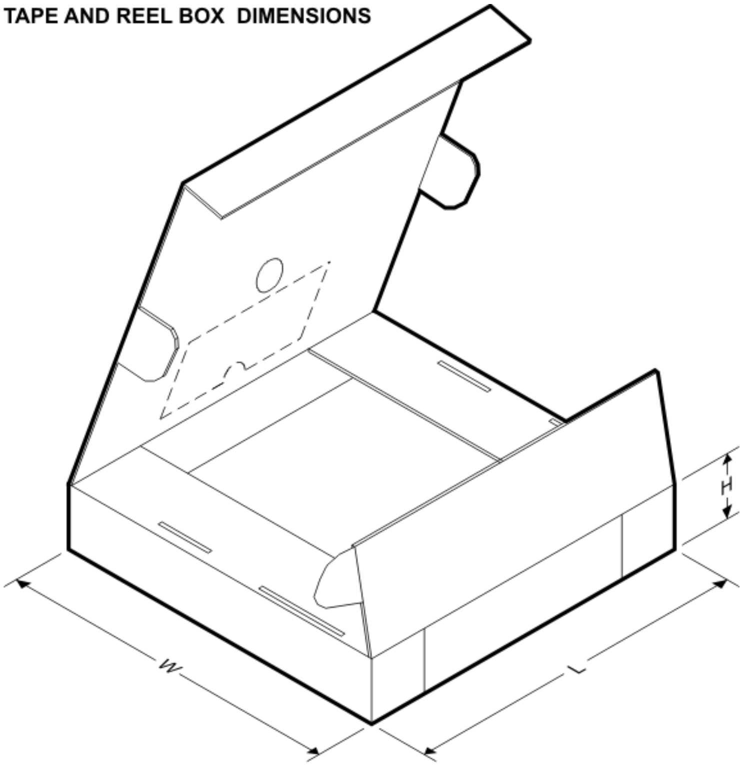
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3883ESX-1.2	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3883ESX-1.2/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3883ESX-1.2	DDPAK/TO-263	KTT	5	500	358.0	343.0	63.0
LP3883ESX-1.2/NOPB	DDPAK/TO-263	KTT	5	500	358.0	343.0	63.0

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