LP3984 Micropower, 150mA Ultra Low-Dropout CMOS Voltage Regulator in Subminiature 4-I/O DSBGA Package

Check for Samples: LP3984

FEATURES

- **Miniature 4-I/O DSBGA and SOT-23-5 Package**
- **Logic controlled enable**
- **Stable with Tantalum Capacitors**
- **1 µF Tantalum Output Capacitor**
- **Fast Turn-On**
- **Thermal Shutdown and Short-Circuit Current Limit**

APPLICATIONS

- **CDMA Cellular Handsets**
- **Wideband CDMA Cellular Handsets**
- **GSM Cellular Handsets**
- **Portable Information Appliances**

KEY SPECIFICATIONS

- **2.5 to 6.0V Input Range**
- **150mA Guaranteed Output**
- **60dB PSRR at 1kHz, 40dB at 10kHz @ 3.1V_{IN}**
- **≤1.2µA Quiescent Current when Shut Down**
- **Fast Turn-On Time: 20 µs (typ.)**
- **75mV typ Dropout with 150mA Load**
- **−40 to +125°C Junction Temperature Range for Operation**
- **1.5V, 1.8V, 2.0V, 2.9V and 3.1V**

DESCRIPTION

The LP3984 is designed for portable and wireless applications with demanding performance and space requirements.

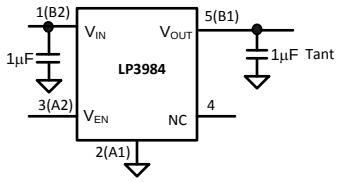
The LP3984's performance is optimized for battery powered systems to deliver extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10 kHz. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 150 mA from a 2.5V to 6V input. The LP3984 consumes less than 1.2µA in disable mode and has fast turn-on time less than 20µs.

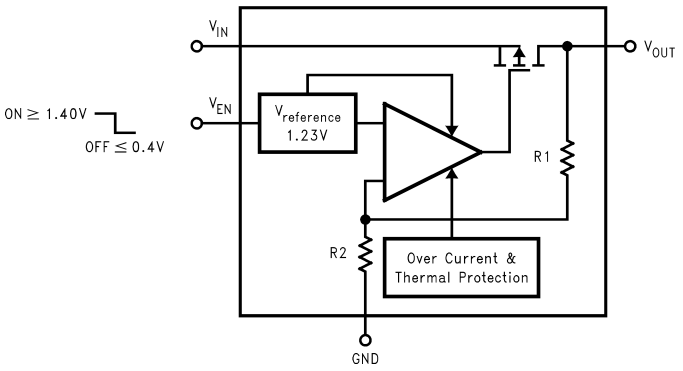
The LP3984 is available in a 4 bump DSBGA and 5 pin SOT-23 package. Performance is specified for −40°C to +125°C temperature range and is available in 1.5V, 1.8V, 2.0V, 2.9V and 3.1V output voltages. For other output voltage options from 1.5V to 3.5V, please contact TI sales office.

Typical Application Circuit



Note: Pin Numbers in parenthesis indicate DSBGA package.

Block Diagram



Pin Descriptions

Name	* DSBGA	SOT	Function
V_{EN}	A2	3	Enable Input Logic, Enable High
GND	A1	2	Common Ground
V_{OUT}	B1	5	Output Voltage of the LDO
V_{IN}	B2	1	Input Voltage of the LDO
N.C.		4	No Connection

Connection Diagram

SOT-23-5 Package

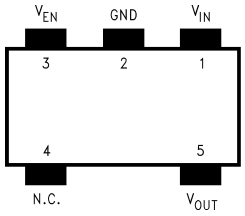


Figure 1. Top View
See Package Number DBV

DSBGA, 4 Bump Package

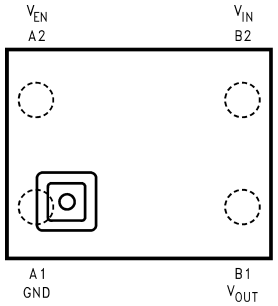


Figure 2. Top View
See Package Number YPB0004

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

V_{IN}, V_{EN}		−0.3 to 6.5V
V_{OUT}		-0.3 to (V_{IN}+0.3) ≤ 6.5V
Junction Temperature		150°C
Storage Temperature		−65°C to +150°C
Lead Temp.		235°C
Pad Temp.(4)		235°C
Maximum Power Dissipation(5)	SOT23-5	364mW
	DSBGA	235mW
ESD Rating(6)	Human Body Model	2kV
	Machine Model	200V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Additional information on pad temperature can be found in the TI AN-1112 Application Report (SNOA401).
(5) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P_D = (T_J - T_A)/\theta_{JA}$,where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 364mW rating for SOT23-5 appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150°C, for T_J, 70°C for T_A, and 220°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70°C . Less power can be dissipated safely at ambient temperatures above 70°C. The Absolute Maximum power dissipation for SOT23-5 can be increased by 4.5mW for each degree below 70°C, and it must be derated by 4.5mW for each degree above 70°C.
(6) The human body model is 100pF discharged through 1.5kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Operating Ratings(1)(2)

V_{IN}		2.5 to 6V
V_{EN}		0 to (V_{IN}+0.3V) ≤ 6V
Junction Temperature		−40°C to +125°C
Thermal Resistance	θ_{JA} (SOT23-5)	220°C/W
	θ_{JA} (DSBGA)	340°C/W
Maximum Power Dissipation(3)	SOT23-5	250mW
	DSBGA	160mW

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 250mW rating for SOT23-5 appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125°C, for T_J, 70°C for T_A, and 220°C/W for θ_{JA} into () above. More power can be dissipated at ambient temperatures below 70°C . Less power can be dissipated at ambient temperatures above 70°C. The maximum power dissipation for operation can be increased by 4.5mW for each degree below 70°C, and it must be derated by 4.5mW for each degree above 70°C.

Electrical Characteristics

Unless otherwise specified: V_{IN} = 2.5V for 1.5, 1.8, & 2.0V options, V_{IN} = V_{OUT} + 0.5 for output options higher than 2.5V, C_{IN} = 1 µF, I_{OUT} = 1mA, C_{OUT} = 1 µF, tantalum. Typical values and limits appearing in standard typeface are for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (1) (2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance			−1.2 **−2.0**	1.2 **2.0**	% of $V_{OUT(nom)}$
	Line Regulation Error	V_{IN} = 2.5V to 4.5V for 1.5, 1.8, 2.0V options V_{IN} = (V_{OUT} + 0.5V) to 4.5V for Voltage options higher than 2.5V	0.05	**−0.15**	**0.15**	%/V
	Load Regulation Error(3)	I_{OUT} = 1 mA to 150 mA LP3984IM5 (SOT23-5)	0.002		**0.005**	%/mA
		LP3984IBP (DSBGA)	0.0009		**0.002**	
PSRR	Power Supply Rejection Ratio	V_{IN} = $V_{OUT(nom)}$ + 0.2V, f = 1 kHz, I_{OUT} = 50 mA, Figure 4	60			dB
		V_{IN} = $V_{OUT(nom)}$ + 0.2V, f = 10 kHz, I_{OUT} = 50 mA, Figure 4	40			
I_Q	Quiescent Current	V_{EN} = 1.4V, I_{OUT} = 0 mA	80		**125**	µA
		V_{EN} = 1.4V, I_{OUT} = 0 to 150 mA	110		**150**	
		V_{EN} = 0.4V	0.005		**1.2**	
	Dropout Voltage(4)	I_{OUT} = 1 mA	0.6		**2.5**	mV
		I_{OUT} = 50 mA	25		**40**	
		I_{OUT} = 100 mA	50		**80**	
		I_{OUT} = 150 mA	75		**120**	
I_{SC}	Short Circuit Current Limit	Output Grounded (Steady State)	600			mA
$I_{OUT(PK)}$	Peak Output Current	V_{OUT} ≥ $V_{OUT(nom)}$ - 5%	600	**300**		mA
T_{ON}	Turn-On Time(5)		20			µs
e_n	Output Noise Voltage	BW = 10 Hz to 100 kHz, C_{OUT} = 1µF tant.	90			µVrms
I_{EN}	Maximum Input Current at EN	V_{EN} = 0.4 and V_{IN} = 6.0	±1			nA
V_{IL}	Maximum Low Level Input Voltage at EN	V_{IN} = 2.5 to 6.0V			**0.4**	V
V_{IH}	Minimum High Level Input Voltage at EN	V_{IN} = 2.5 to 6.0V		**1.4**		V
C_{OUT}	Output Capacitor	Capacitance		**1**	**22**	µF
		ESR		**2**	**10**	Ω
TSD	Thermal Shutdown Temperature		160			°C
	Thermal Shutdown Hysteresis		20			°C

(1) All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.
(3) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(4) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.
(5) Turn-on time is time measured between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.

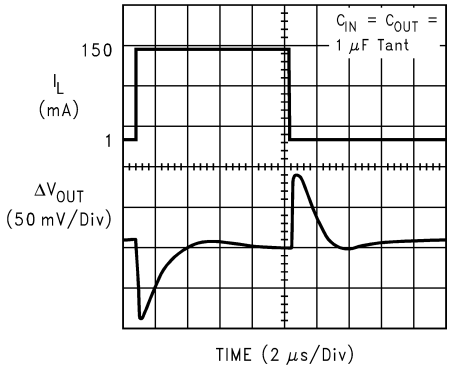


Figure 3. Line Transient Input Test Signal

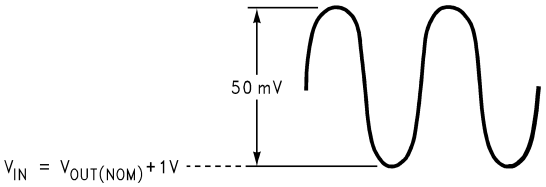


Figure 4. PSRR Input Test Signal

Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Tantalum, $V_{IN} = 2.5$ for 1.5, 1.8, and 2.0V options, $V_{IN} = V_{OUT} + 0.2V$ for output options higher than 2.5V, $T_A = 25°C$, Enable pin is tied to V_{IN}.

Power Supply Rejection Ratio (V_{IN} = 3.5V)

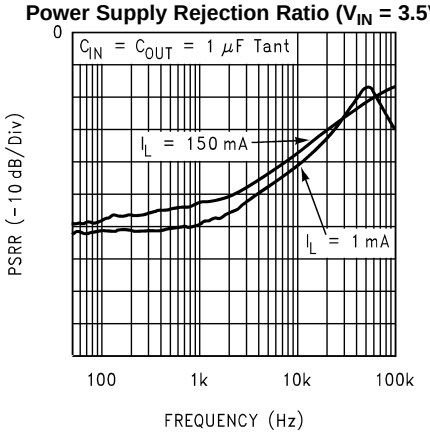


Figure 5.

Power Supply Rejection Ratio (V_{IN} = 3.5V)

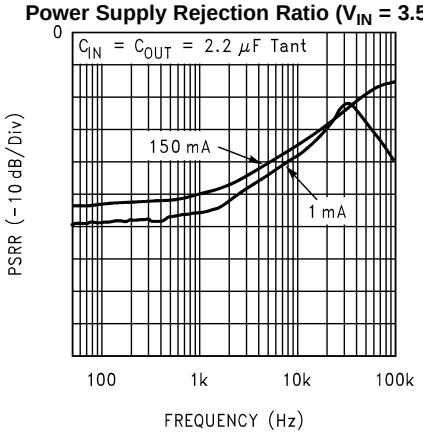


Figure 6.

Power Supply Rejection Ratio (V_{IN} = 3.5V)

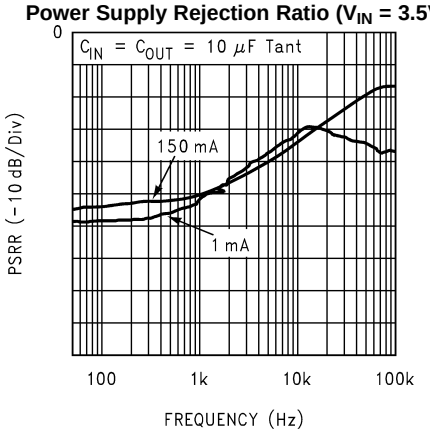


Figure 7.

Power Supply Rejection Ratio (LP3984-1.5, V_{IN} = 2.5V)

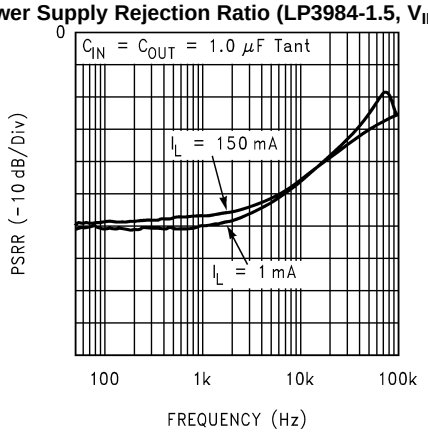


Figure 8.

Line Transient Response (LP3984-3.1)

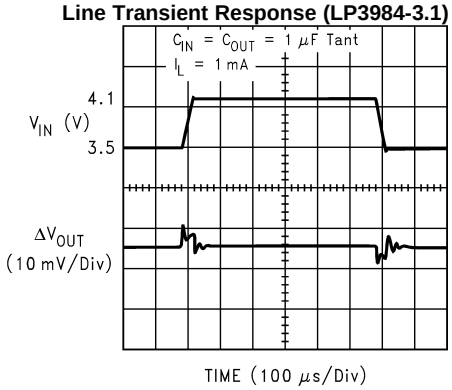


Figure 9.

Line Transient Response (LP3984-3.1)

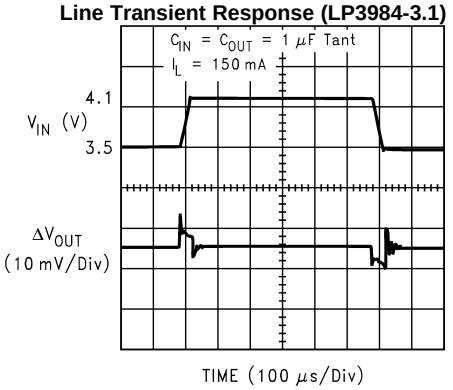


Figure 10.

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Tantalum, $V_{IN} = 2.5$ for 1.5, 1.8, and 2.0V options, $V_{IN} = V_{OUT} + 0.2$V for output options higher than 2.5V, $T_A = 25°C$, Enable pin is tied to V_{IN}.

Line Transient Response (LP3984-3.1)

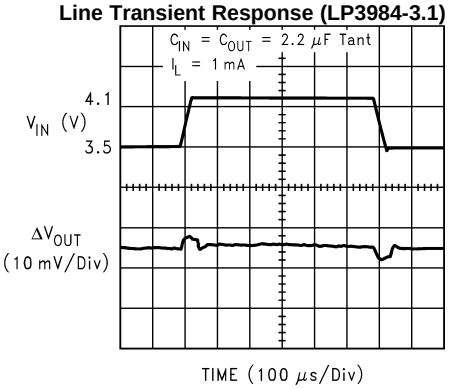


Figure 11.

Line Transient Response (LP3984-3.1)

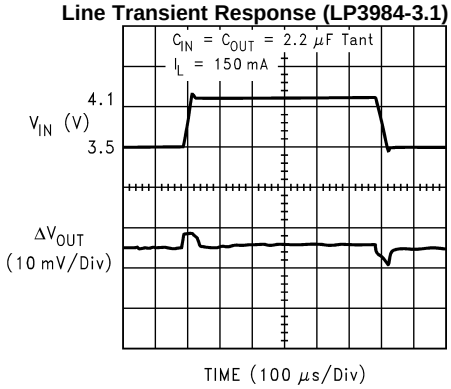


Figure 12.

Line Transient Response (LP3984-3.1)

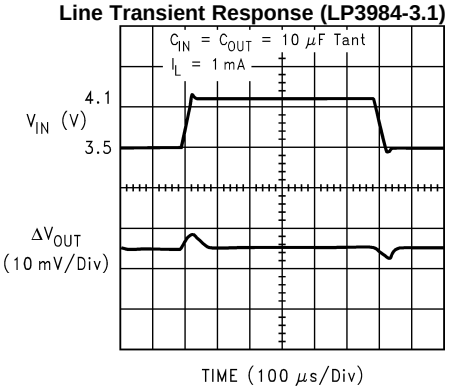


Figure 13.

Line Transient Response (LP3984-3.1)

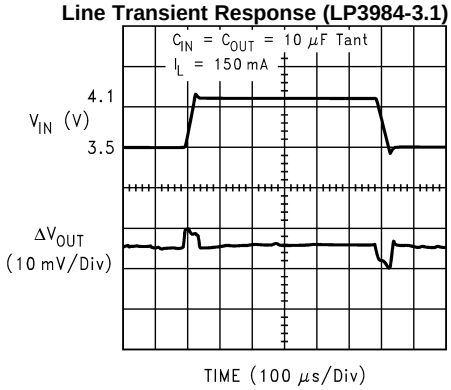


Figure 14.

Start Up Response

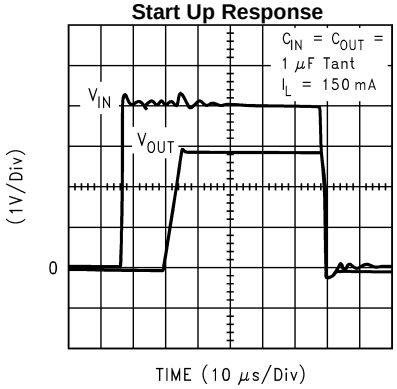


Figure 15.

Start Up Response

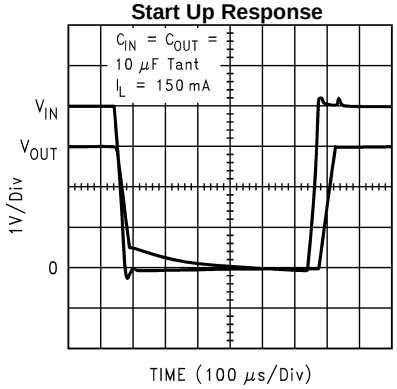


Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\ \mu F$ Tantalum, $V_{IN} = 2.5$ for 1.5, 1.8, and 2.0V options, $V_{IN} = V_{OUT} + 0.2V$ for output options higher than 2.5V, $T_A = 25°C$, Enable pin is tied to V_{IN}.

Enable Response

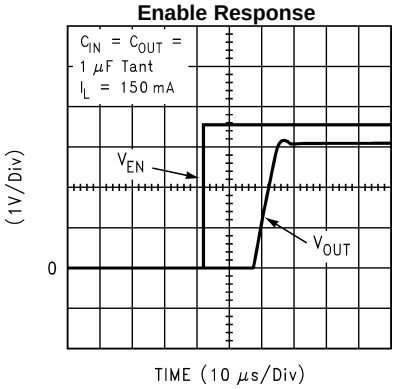


Figure 17.

Load Transient Response (LP3984-3.1

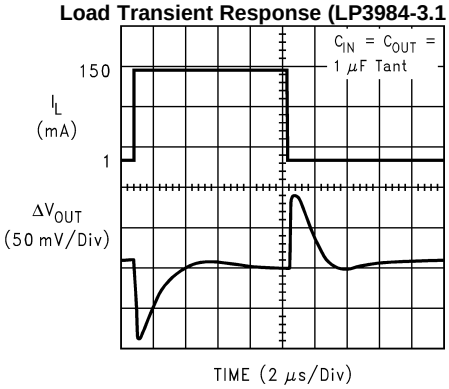


Figure 18.

Load Transient Response (LP3984-3.1)

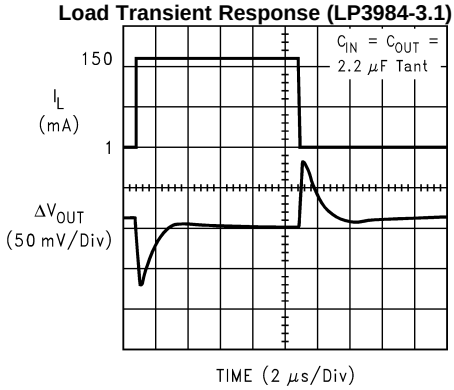


Figure 19.

Load Transient Response (V_{IN} = 4.2V)

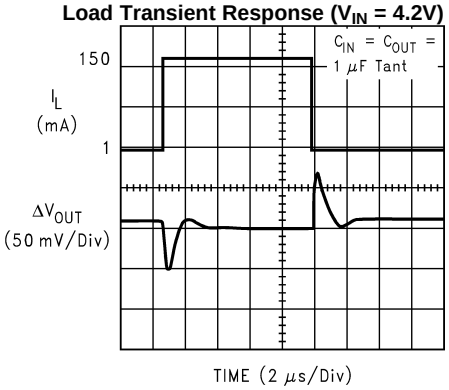


Figure 20.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3984 requires external capacitors for regulator stability. The LP3984 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of ≅ 1µF is required between the LP3984 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 1µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3984 is designed specifically to work with tantalum output capacitors. A tantalum capacitor in 1 to 22 µF range with 2Ω to 10Ω ESR range is suitable in the LP3984 application circuit.

It may also be possible to use film capacitors at the output, but these are not as attractive for reasons of size and cost.

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (2Ω to 10Ω).

NO-LOAD STABILITY

The LP3984 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

ON/OFF INPUT OPERATION

The LP3984 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all times. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

FAST ON-TIME

The LP3984 output is turned on after V_{ref} voltage reaches its final value (1.23V nominal). To speed up this process, the noise reduction capacitor at the bypass pin is charged with an internal 70µA current source. The curernt source is turned off when the bandgap voltage reaches approximately 95% of its final value. The turn on time is determined by the time constant of the bypass cpacitor. The smaller the capacitor value, the shorter the turn on time, but less noise gets reduced. As a result, turn on time and noise reduction need to be taken into design consideration when choosing the value of the byupass capacitor.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in TI AN-1112 Application Report (SNOA401). Referring to the section *SMT Assembly Considerations*, it should be noted that the pad style which must be used with the 5 pin package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct sunlight will cause misoperation of the device. Light sources such as halogen lamps can effect electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A DSBGA test board was brought to within 1cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP3984IMF-1.5	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI		LEAB	Samples
LP3984IMF-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LEAB	Samples
LP3984IMF-1.8	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI		LEBB	Samples
LP3984IMF-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LEBB	Samples
LP3984IMF-3.1	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LEDB	Samples
LP3984IMF-3.1/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LEDB	Samples
LP3984IMFX-1.8	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	LEBB	Samples
LP3984IMFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LEBB	Samples
LP3984ITP-2.9/NOPB	ACTIVE	DSBGA	YPB	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3984ITP-3.1/NOPB	ACTIVE	DSBGA	YPB	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3984ITPX-1.8/NOPB	ACTIVE	DSBGA	YPB	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3984ITPX-3.1/NOPB	ACTIVE	DSBGA	YPB	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

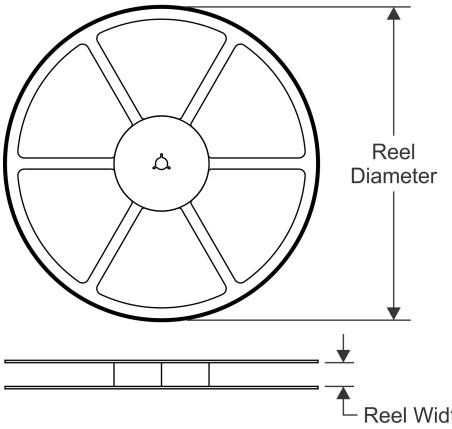
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

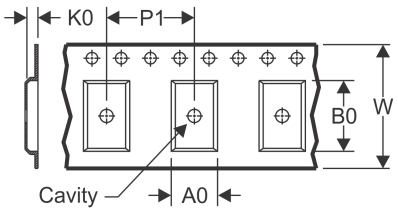
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

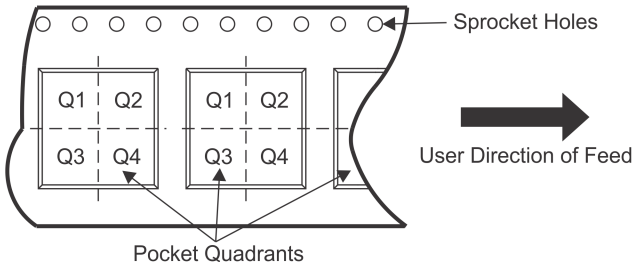


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

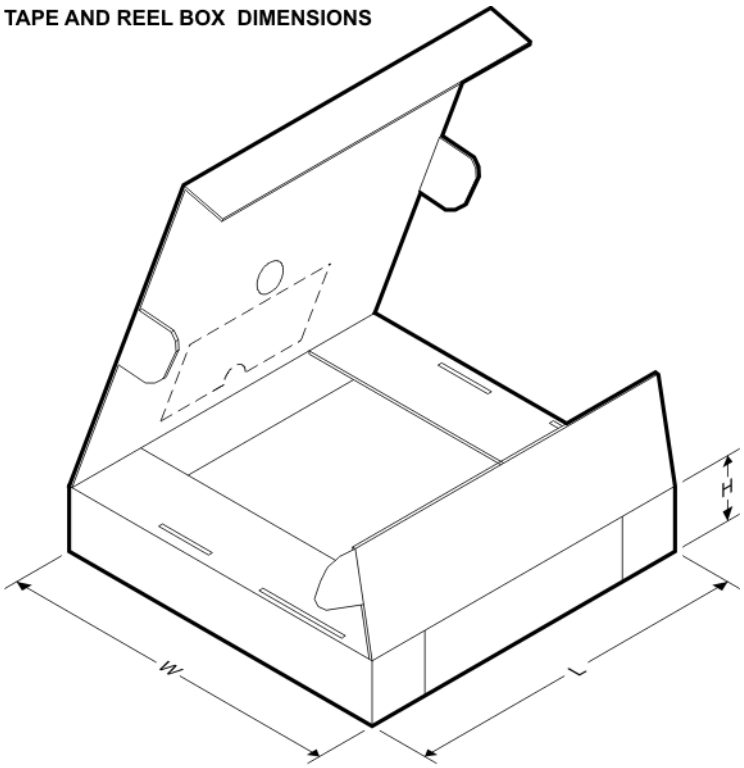
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3984IMF-1.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3984IMF-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3984IMF-1.8	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3984IMF-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3984IMF-3.1	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3984IMF-3.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3984IMFX-1.8	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3984IMFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3984ITP-2.9/NOPB	DSBGA	YPB	4	250	178.0	8.4	1.02	1.09	0.66	4.0	8.0	Q1
LP3984ITP-3.1/NOPB	DSBGA	YPB	4	250	178.0	8.4	1.02	1.09	0.66	4.0	8.0	Q1
LP3984ITPX-1.8/NOPB	DSBGA	YPB	4	3000	178.0	8.4	1.02	1.09	0.66	4.0	8.0	Q1
LP3984ITPX-3.1/NOPB	DSBGA	YPB	4	3000	178.0	8.4	1.02	1.09	0.66	4.0	8.0	Q1

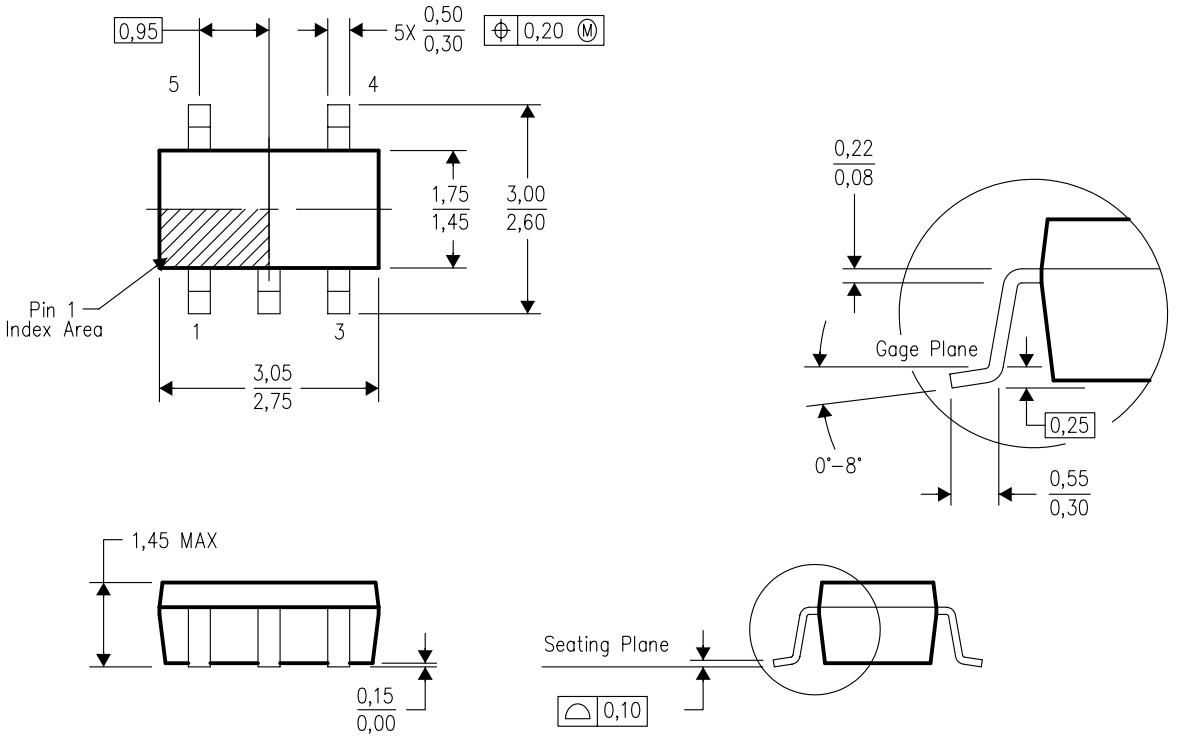
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3984IMF-1.5	SOT-23	DBV	5	1000	203.0	190.0	41.0
LP3984IMF-1.5/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LP3984IMF-1.8	SOT-23	DBV	5	1000	203.0	190.0	41.0
LP3984IMF-1.8/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LP3984IMF-3.1	SOT-23	DBV	5	1000	203.0	190.0	41.0
LP3984IMF-3.1/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LP3984IMFX-1.8	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP3984IMFX-1.8/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP3984ITP-2.9/NOPB	DSBGA	YPB	4	250	203.0	190.0	41.0
LP3984ITP-3.1/NOPB	DSBGA	YPB	4	250	203.0	190.0	41.0
LP3984ITPX-1.8/NOPB	DSBGA	YPB	4	3000	206.0	191.0	90.0
LP3984ITPX-3.1/NOPB	DSBGA	YPB	4	3000	206.0	191.0	90.0

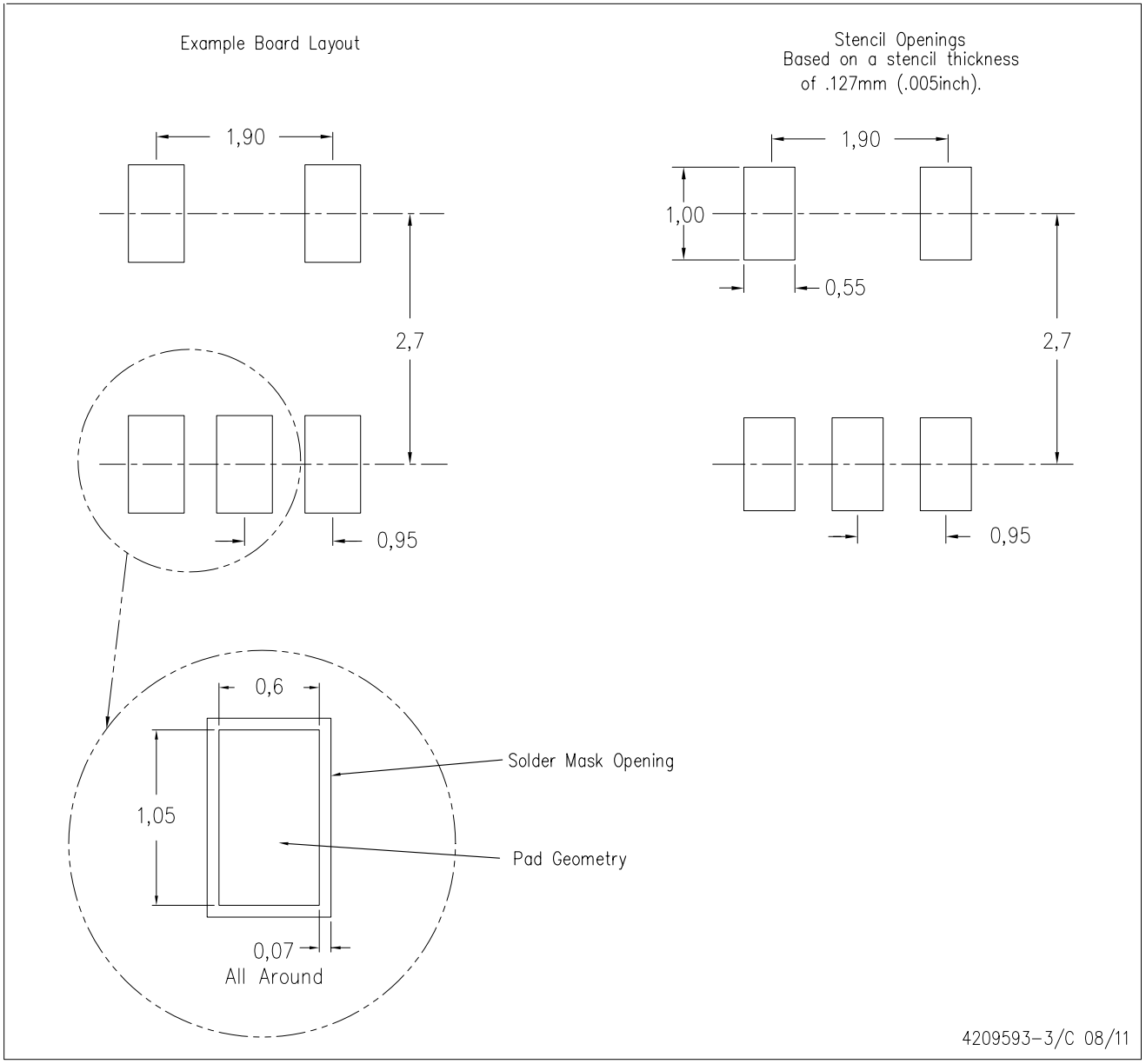
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

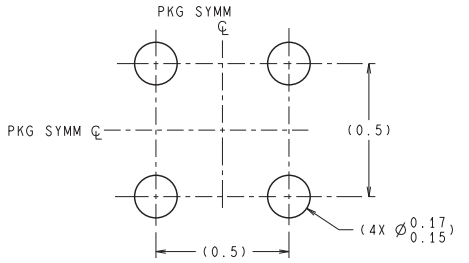
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



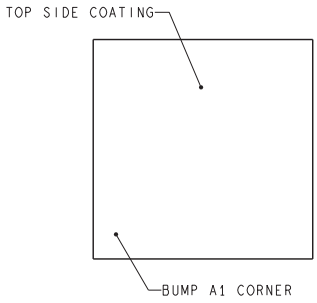
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

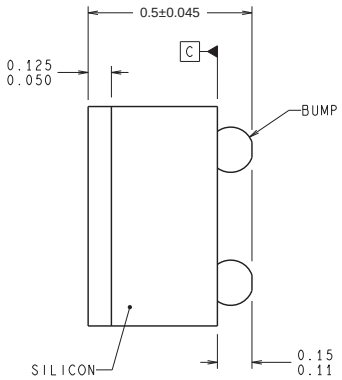
YPB0004

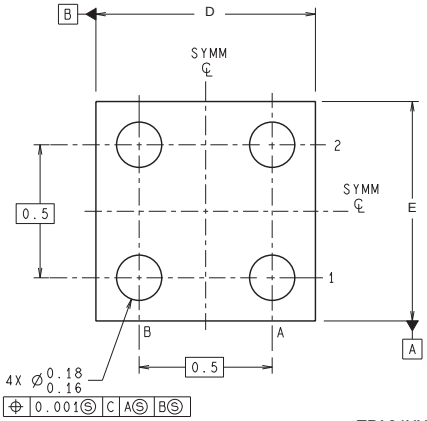


DIMENSIONS ARE IN MILLIMETERS

LAND PATTERN RECOMMENDATION







TPA04XXX (Rev B)

D: Max = 1.039 mm, Min =0.938 mm

E: Max = 0.925 mm, Min =0.824 mm

4215097/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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