LP5524 Parallel LED Driver with PWM Brightness Control in DSBGA Package

Check for Samples: LP5524

FEATURES

- **High Side LED Driver**
- **Drives 4 LEDs with Up to 25mA per LED**
- **Ultra-Small Solution Size:**
  - **No External Components**
  - **DSBGA-9 Package with 0.4 mm pitch:**
    - **1.215mm x 1.215mm x 0.6mm (LxWxH)**
- **0.4% Typical Current Matching**
- **PWM Brightness Control**
- **Over-Current Protection**
- **Wide Input Voltage Range: 2.7V to 5.5V**

APPLICATIONS

- **Sub display Backlight**
- **Keypad LED Backlight**
- **Indicator LED**

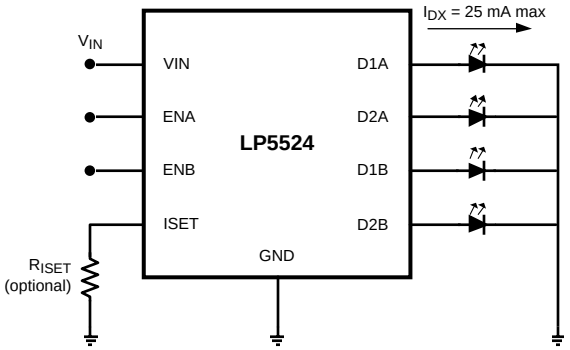
DESCRIPTION

The LP5524 is a highly integrated dual-zone LED driver that can drive up to four LEDs in parallel with a total output current of 100mA. Regulated high side internal current sources deliver excellent current and brightness matching in all LEDs.

LED driver current sources are split into two independently controlled banks for driving secondary displays, keypad and indicator LEDs. Brightness control is achieved by applying PWM signals to each enable pin. Default LED current is factory-programmable and an optional external resistor can be used to set LED current to user programmable values.

LP5524 is available in National's tiny 9-bump thin DSBGA package.

Typical Application



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Connection Diagram

Connection Diagrams and Package Mark Information

DSBGA-9 package, 1.215 x 1.215 x 0.60 mm body size, 0.4 mm pitch

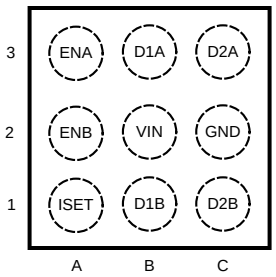

Figure 1. Top View

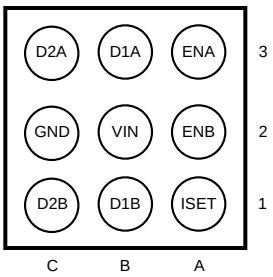

Figure 2. Bottom View

PIN DESCRIPTIONS(1)

Pin	Name	Type	Description
A1	ISET	AI	Current set input
A2	ENB	DI	Enable for bank B
A3	ENA	DI	Enable for bank A
B1	D1B	AO	Current source output, bank B LED1
B2	VIN	P	Power supply pin
B3	D1A	AO	Current source output, bank A LED1
C1	D2B	AO	Current source output, bank B LED2
C2	GND	G	Ground
C3	D2A	AO	Current source output, bank A LED2

(1) A: Analog Pin D: Digital Pin G: Ground Pin P: Power Pin I: Input Pin O: Output Pin

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)(2)(3)

V (VIN, DX, ISET)	-0.3V to +6.0V
Voltage on logic pins (ENA, ENB)	-0.3V to +6.0V
Continuous Power Dissipation(4)	Internally Limited
Junction Temperature (T_{J-MAX})	125°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Reflow soldering, 3 times)	See(5)
ESD Rating(6) Human Body Model	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typ.) and disengages at T_J=140°C (typ.).
(5) For detailed soldering specifications and information, please refer to National Semiconductor Application Note AN1112 : DSBGA Wafer Level Chip Scale Package.
(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. MIL-STD-883 3015.7

Operating Ratings(1)(2)

Voltage on power pin (VIN)	2.7V to 5.5V
Junction Temperature (T_J) Range	-40°C to +125°C
Ambient Temperature (T_A) Range(3)	-40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), YFQ0009AAA Package(1)	80 - 125°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

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Electrical Characteristics[1][2]

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (-40°C < T_A < +85°C). Unless otherwise noted, specifications apply to the LP5524 Block Diagram with: V_{IN} = 3.6V, R_{ISET} = 32.4 kΩ, C_{IN} = 100 nF.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{VIN}	Shutdown Supply Current	ENA = ENB = 0V		0.2	**1**	µA
	Active Mode Supply Current	ENA = ENB = H, ISET = open		170	**210**	µA
I_{DX}	Recommended LED Current		3		25	mA
I_{OUT}	LED Output Current Accuracy	I_{DX} = 5mA, V_{DX} = V_{IN} - 0.2V ISET = open		0.5	**5**	%
	LED Output Current Accuracy	I_{DX} = 15.9mA, V_{DX} = V_{IN} - 0.2V		0.5	**4**	%
I_{MATCH}	LED Current Matching[3]	I_{DX} = 15.9mA		0.4	**2.5**	%
$\Delta I_{DX}\%/\Delta V_{IN}$	Line Regulation			1		%/V
$\Delta I_{DX}\%/\Delta V_{DX}$	Load Regulation	V_{DX} < V_{IN} - 0.2V		0.4		%/V
V_{HR}	Minimum Headroom Voltage (V_{IN} - V_{DX})[4]	I_{DX} set to 5 mA		10		mV
		I_{DX} set to 15 mA		30	**75**	mV
I_{MIRROR}	External R_{ISET} to LED Current Mirroring Ratio			1:416		
V_{ISET}	ISET Reference Voltage			1.237		V
I_{ISET}	ISET Pin Current Range		**2.5**		**62.5**	µA
$t_{PWM\ MIN}$	Recommended Minimum On Time For PWM Signal			33		µs
V_{IL}	Logic Input Low Level				**0.4**	V
V_{IH}	Logic Input High Level		**1.2**			V
I_{IN}	CTRL Input Current	ENA / ENB = 1.2V		1.2	**1.9**	µA
t_{SD}	Shutdown Delay Time	Delay from ENA and ENB = low to I_{DX} = 0.1 x I_{DX} nom		20	25	µs

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(3) Matching is the maximum difference from the average.
(4) The current source is connected internally between V_{IN} an V_{DX}. The voltage across the current source, (V_{IN} - V_{DX}), is referred to a Headroom Voltage (V_{HR}). Minimum Headroom Voltage is defined as the V_{HR} voltage when the LED current has dropped 20% from the value measured at V_{DX} = V_{IN} - 1V.

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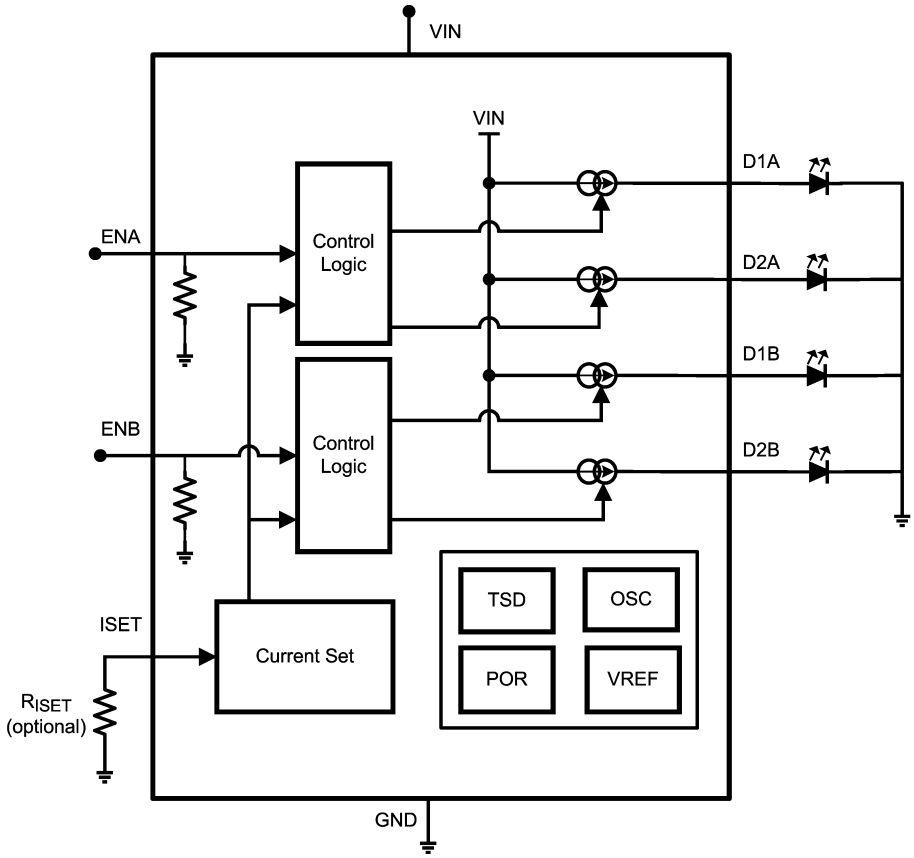
LP5524 Block Diagram



LED Driver Typical Performance Characteristics

T_J = 25°C. Unless otherwise noted, typical performance characteristics apply to the LP5524 Block Diagram with: V_{IN} = 3.6V, R_{ISET} = 32.4 kΩ, C_{IN} = 100 nF.

Output Current vs R_{ISET} (Expanded Range)

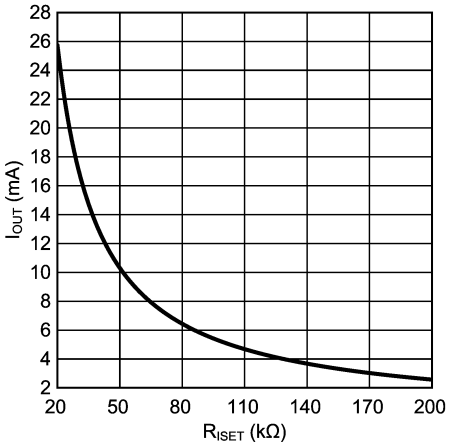


Figure 3.

Output Current vs R_{ISET}

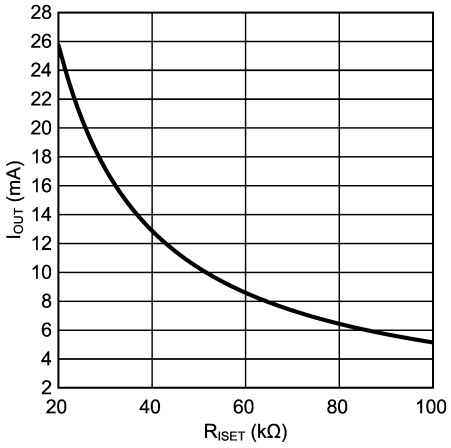


Figure 4.

Output Current vs Input Voltage (ISET Connected To VDD)

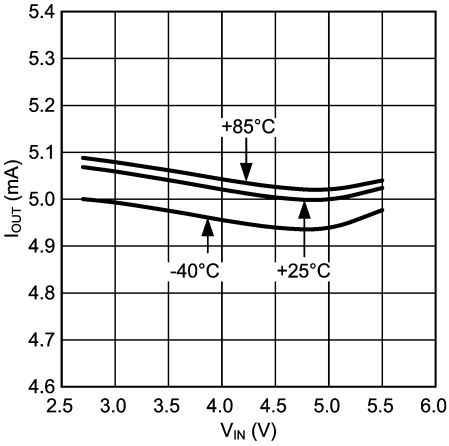


Figure 5.

Output Current vs Headroom Voltage

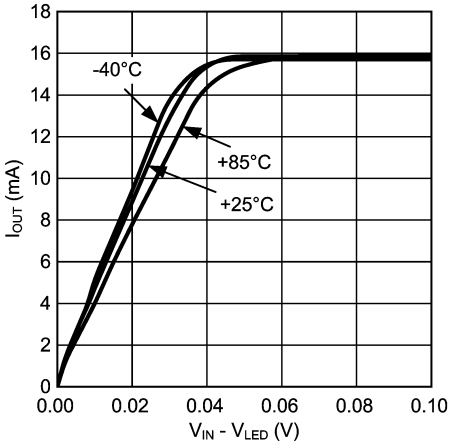


Figure 6.

PWM Responce (Both Channels)

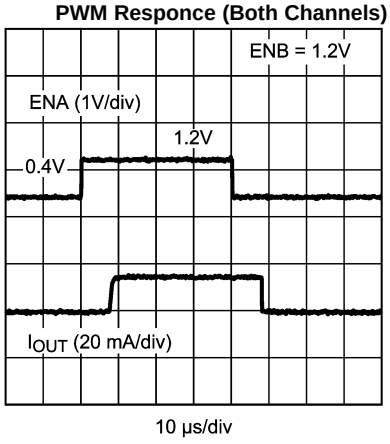


Figure 7.

PWM Response (Single Channel)

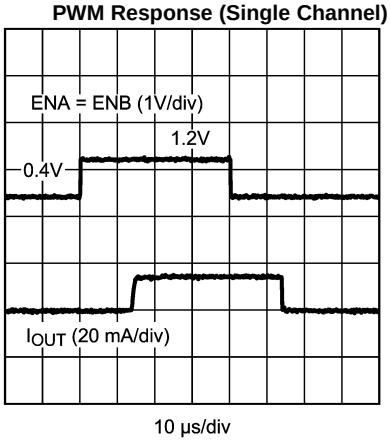


Figure 8.

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APPLICATION INFORMATION

ENABLE MODE

The LP5524 has four constant current LED outputs which are split into two independently controlled banks. Each bank has its own enable input. ENA is used to control bank A and ENB is used to control bank B. Both enables are active high and have internal pull–down resistors. When both enables are low part is in low power standby mode. Driving either enable high will activate the part and corresponding LED outputs.

ISET PIN

An external resistor (R_{ISET}) connected to ISET pin sets the output current of all the LEDs. The internal current mirror sets the LEDs output current with a 416:1 ratio to the current through R_{ISET}. The following equation approximates the LED current:

$$I_{DX} = 515 / R_{ISET} \text{ (Amps)} \quad (1)$$

The use of R_{ISET} is optional. If R_{ISET} is not used ISET pin can be left floating or connected to V_{IN}. In these cases LED current is set to default current.

PWM BRIGHTNESS CONTROL

The brightness of LEDs can be linearly varied from zero up to the maximum programmed current level by applying a Pulse–Width–Modulated signal to the ENx pin of the LP5524. The following procedures illustrate how to program the LED drive current and adjust the output current level using a PWM signal.

1. Determine the maximum desired LED current. Use the I_{DX} equation to calculate R_{ISET}.
2. Brightness control can be implemented by pulsing a signal at the ENx pin. LED brightness is proportional to the duty cycle (D) of the PWM signal.

For linear brightness control over the full duty cycle adjustment range, the LP5524 uses a special turn–off time delay to compensate the turn–on time of the device.

If the PWM frequency is much less than 100Hz, flicker may be seen in the LEDs. For the LP5524, zero duty cycle will turn off the LEDs and a 50% duty cycle will result in an average I_{DX} being half of the programmed LED current. For example, if R_{ISET} is set to program LED current to 15 mA, a 50% duty cycle will result in an average I_{DX} of 7.5mA.

LED HEADROOM VOLTAGE

A single current source is connected internally between VIN and DX outputs (D1A, D2A, D1B and D2B). The voltage across the current source, (V_{IN} – V_{DX}), is referred to as headroom voltage (V_{HR}). The current source requires a sufficient amount of headroom voltage to be present across it in order to regulate properly.

Figure 6 shows how output current of the LP5524 varies with respect to headroom voltage. On the flat part of the graph, the current is regulated properly as there is sufficient headroom voltage for regulation. On the sloping part of the graph the headroom voltage is too small, the current source is squeezed, and the current drive capability is limited. Thus, operating the LP5524 with insufficient headroom voltage across the current source should be avoided.

LED OUTPUTS

If more than 25 mA of output current is required LED outputs can be connected parallel. Connecting LED outputs of different group parallel generates a simply two stage brightness control. With I_{DX} set to 25 mA, enabling one group sets the LED current to 25 mA. Enabling second bank increases the LED current to 50 mA. Unused LED outputs can be left floating or tied to VIN.

Recommended External Components

INPUT CAPACITOR, C_{IN}

Although not required for normal operation, a capacitor can be added to V_{IN} to reduce line noise. A surface-mount multi-layer ceramic capacitor (MLCC) is recommended. MLCCs with a X7R or X5R temperature characteristic are preferred.

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CURRENT SET RESISTOR, R_{ISET}

If other than 5 mA current is required, R_{ISET} resistor can be used to adjust the current. For 15.9 mA current 32.4 kΩ resistor is required. Accuracy of the resistor directly effects to the accuracy of the LED current. 1% or better is recommended.

LED

Forward voltage of LED must be less than minimum input voltage minus minimum headroom voltage (V_{HR}). For example with 2.7V input voltage and 20 mA LED current the maximum LED forward voltage is 2.7V - 100 mV = 2.6V.

Table 1. List of Recommended External Components

Symbol	Symbol Explanation	Value	Unit	Type
C_{IN}	VDD Bypass Capacitor	100	nF	Ceramic, X7R or X5R
R_{ISET}	Current Set Resistor for 15.9 mA LED Current	32.4	kΩ	1%
LEDs		User defined		

Table 2. Recommended E96 Series (1% Tolerance) Current Set Resistors

R_{ISET} (kΩ)	I_{DX} (mA)	R_{ISET} (kΩ)	I_{DX} (mA)
169	3.0	34.0	15.1
127	4.1	32.4	15.9
102	5.0	30.1	17.1
84.5	6.1	28.7	17.9
73.2	7.0	26.7	19.3
64.9	7.9	25.5	20.2
56.2	9.2	24.3	21.2
51.1	10.1	23.2	22.2
46.4	11.1	22.1	23.3
42.2	12.2	21.5	24.0
39.2	13.1	20.5	25.1
36.5	14.1		

$$I_{DX} = 515 / R_{ISET} \text{ (Amps)} \quad (2)$$

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP5524TM-5/NOPB	ACTIVE	DSBGA	YFQ	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	V2	Samples
LP5524TMX-5/NOPB	ACTIVE	DSBGA	YFQ	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	V2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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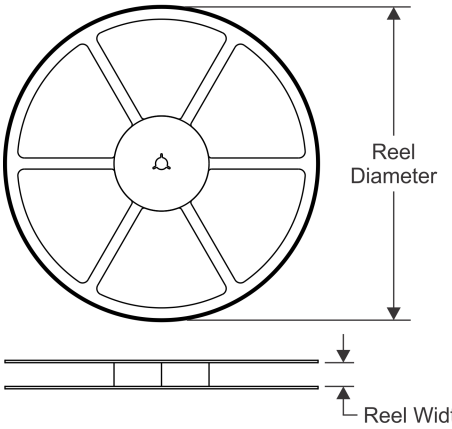
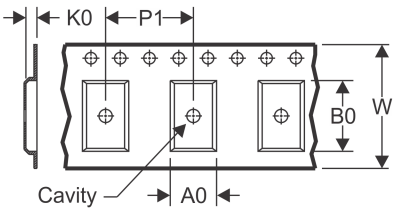
REEL DIMENSIONS

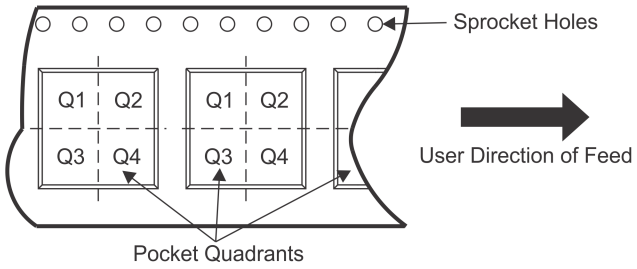


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

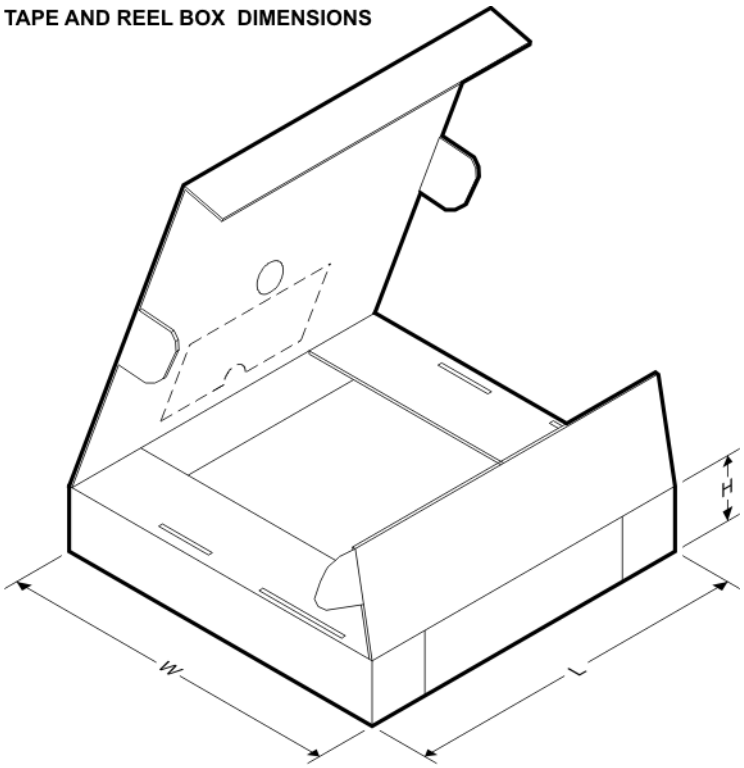
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5524TM-5/NOPB	DSBGA	YFQ	9	250	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1
LP5524TMX-5/NOPB	DSBGA	YFQ	9	3000	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1

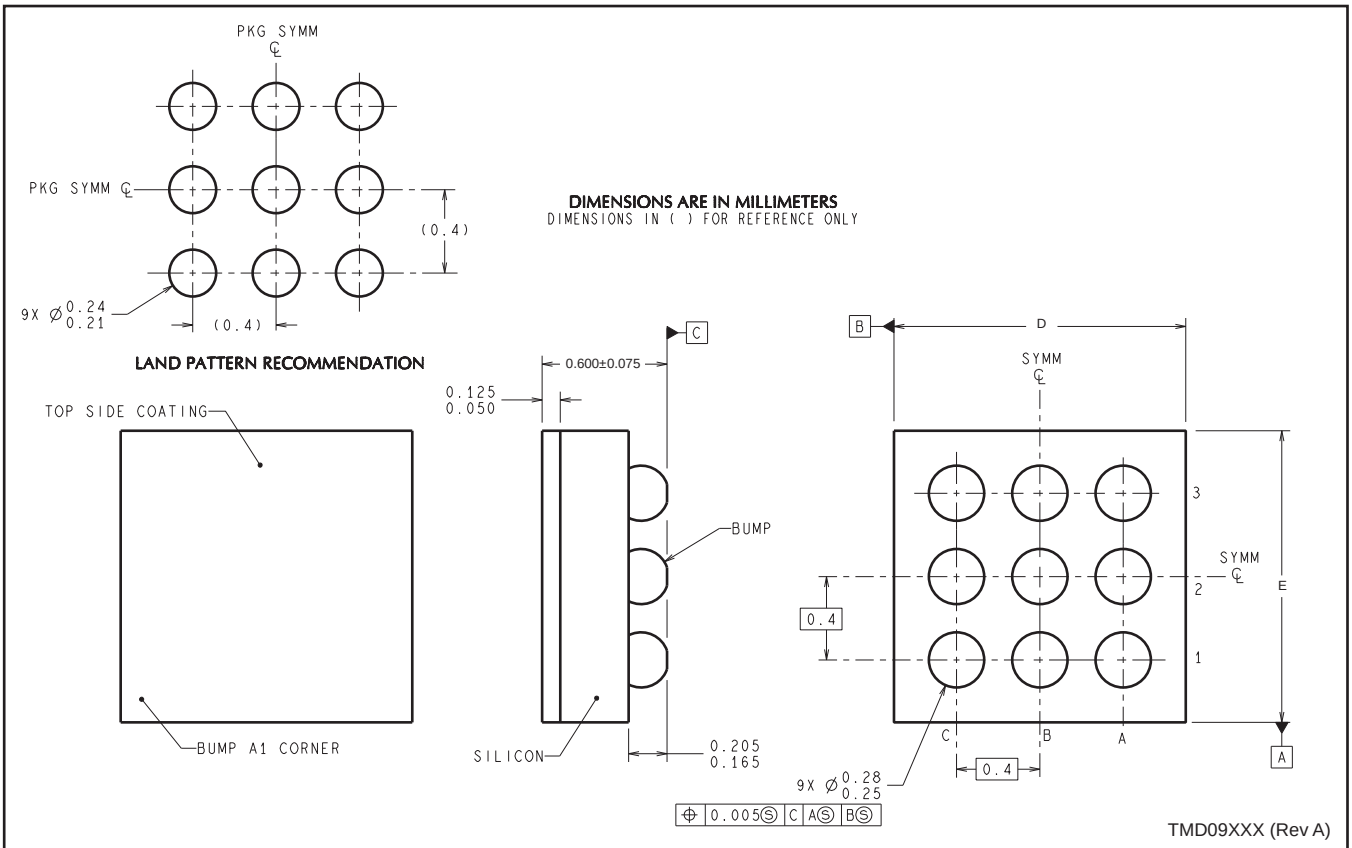
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5524TM-5/NOPB	DSBGA	YFQ	9	250	203.0	190.0	41.0
LP5524TMX-5/NOPB	DSBGA	YFQ	9	3000	206.0	191.0	90.0

YFQ0009



D: Max = 1.26 mm, Min = 1.16 mm

E: Max = 1.26 mm, Min = 1.16 mm

4215077/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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