NXP LPCOpen LPC8xx Release Notes

LPCOpen LPC8xx version release history and known issues

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The version history and known issue lists on this page are for v3.xx, and 2.xx releases of LPCOpen only. Version history previous to v2.xx releases can be found HERE..

Some issues are known at the time of the versioned package release. Issues found after the release can be found on the LPCOpen bug tracker pages.

LPCOpen v3.02 release (Released: 12/22/2017)

Project and Example updates

Features Added

- None

Changes

- File structure was organized.

Known issues (Carried Forward)

LPCOpen v3.01 release (Released: 04/06/2017)

Project and Example updates

Features Added

- V2 LPCOpen code was converted to V3 LPCOpen. This simplifies code structure and decrease path lengths, LPCOpen has been reorganized to a flatter structure. These changes have been made in an effort to improve usability and maintainability of LPCOpen software

Changes

- I2c_rom: renamed the address to reflect the 8-bit value was ADDR7BIT now ADDR8BIT
- I2cm_8xx.h: Added check for error condition of not completing a transaction
- gpio_8xx.h: Fixed the mask for IO bits (was 8-bit char, and is now 32 bits)
- Updated ring_buffer.c, and ring_buffer.h files
- Board setup file updated to allow selection of XTAL
- I2C master example: "status" in "I2CM_XFER_T" was made "volatile"
  In function "Chip_I2CM_XferHandler", member "status" in "I2CM_XFER_T" set to "STATUS_OK" only after "I2C_STAT_MSTCODE_IDLE" flag is set). Also, "I2C_INTENSET_MSTPENDING" IRQ was disabled (can use “Chip_I2C_ClearInt (pI2C, I2C_INTENSET_MSTPENDING);”) when I2C_STAT_MSTCODE_IDLE is detected (master job is done) to prevent unwanted IRQ firing.
- I2C slave: "Chip_I2CS_SlaveContinue(pI2C);" should be called in slave ISR even if "I2C_INTENSET_SLVDESEL" flag is set
- Updated GPIO API file
- uart_8xx.c:
  - Fixed the print string to calculate length correctly
  - In function “Chip_UART_ReadBlocking”, the judgement "while (readBytes < numBytes)" is wrong. Was changed to "while (numBytes > 0)
  - Should be int Chip_UART_ReadBlocking(LPC_USART_T *pUART, void *data, int numBytes)
- mbed MAX board has CMSIS_DAP debugger software as default. All projects need to be configured to use CMSIS-DAP as default.
- In IAR, all examples have wrong path. It checks for examples_81x instead of example_82x.
- periph_dma_mem and periph_dma_uart: Fixed hard fault during execution.

Known issues (Carried Forward)

LPCOpen v2.19 release (Released: 09/01/2015)

Project and Example updates

Changes

- Added PLL example
- Updated the PLL driver to support multiple frequencies
- Updated IAP library API for reading the Unique ID
- Fixed UART baud rate calculation

Known issues (Carried Forward)

- Chip_GPIO_SetPortDIROutput() and other GPIO Port functions must have the pinMask type as uint32_t instead of uint8_t

LPCOpen v2.15 release (Released: 01/08/2015)

Project and Example updates

Changes

- Fixed system clock frequency calculation function
- Fixed IAR/Keil build warnings
- Added support to run from IRC without using PLL
- Keil Projects updated to Keil uVision v5.xx
- IAR Projects updated to IAR version 7.xx
- Updated ADC and ACMP examples [Directly connects to POT in EA Base board]
- Examples updated, so that it won't depend on EA Motor control board
- Glitch Filter APIs updated
- Board library UART Fractional generator configuration updated
- Fixed low power mode API Chip_PMU_SleepState()
- readme files updated
- Updated SCT Examples
- Fixed a stack overwrite problem in IAP code
- PININT interrupt names made consistent

Known issues (Carried Forward)

- During debugging LPCXpresso_824 keil might show "Invalid ROM Table" error, in which case reset button must be pressed and released while holding the ISP button down
- Chip_GPIO_SetPortDIROutput() and other GPIO Port functions must have the pinMask type as uint32_t instead of uint8_t

LPCOpen v2.13 release (Released: 09/30/2014)

LPC824 updates only

The v2.13 update adds support for the LPC82x chip and LPCXpresso board with LPC824.

Changes

- Added support for LPC82x Chip
- Initial release for LPCXpresso LPC824 board

Known issues (Carried Forward)

- During debugging keil might show "Invalid ROM Table" error, in which case reset button must be pressed and released while holding the ISP button down

LPCOpen v2.01 release (Released: 10/04/2013)

LPC8XX updates only

The v2.01 update adds support for the LPC800_MAX board and some small tweaks in the LPC8xx chip layer code.

Changes

- Added support for LPC800-MAX board with LPC812 device for Keil, IAR, and LPCXpresso toolchains.
- LPC8xx chip layer changes
  - SCT driver register structured reorganized to include 32x1/16x2 unions. Should not impact existing code.
  - For fixed pin enumerations in the swm_8xx.h file, 'SWM_FIXED_' now precedes the definition name to identify it was a SWM fixed pin definition: Example: ACMP_I1 changed to SWM_FIXED_ACMP_I1
  - Minor commenting and formatting fixes, some DoxyGen related cleanup
  - Fixed logic for Chip_SWM_IsEnabled() function
  - Header files for ROM functions are now prefixed with rom_ (example rom_uart_8xx.h)
  - Moved soem functions related to clocking from syscon_8xx.h to clock_8xx.h
  - Added new function Chip_UART_GetIntsEnabled() for returning enabled UART interrupts
  - CMSIS IRQ names (NVIC) mapped to interrupt handler function names in documentation now
  - cmsis.h file was moved inside the chip_8xx area
  - Fixed offset for DEVICEID for LPC8xx in SYSCON (submitted by developer)
  - Renamed Chip_PININT_IsHighEnable() to Vhip_PININT_GetHighEnabled() and Chip_PININT_IsLowEnabled to Chip_PININT_GetLowEnabled()
  - 'PMI' convention changed to 'PININT' convention for PININT driver, LPC_PMI changed to LPC_PININT
  - Added build warnings to some examples when pin muxing hasn't been defined
  - Keil and IAR project cleanup to improve consistency
  - Added a 'board_api_stubs_8xx.c' file to use as a drop-in board layer stub

Known issues (Carried Forward)

- Periph_i2c_rom_slave example builds and runs, but does not work correctly. (LPC8xx release only)
- ACMP ladder selection is wrong.

LPCOpen v2.00 release for LPC8XX only (Released: 08/30/2013)

Changes

- LPCOpen changes (also applies to upcoming LPC11xx and LPC13xx releases, but not LPC17xx/40xx and LPC18xx/43xx releases)
    - Chip layer code and Board layer code are no longer blended into a single platform library
    - Chip layer code no longer requires definitions that were defined in the board layer such as oscillator rate, internal clock input rate, etc.
        - For these few cases where these were used, the chip layer now uses them as external constants defined somewhere else (usually in the board layer)
    - The lpc_ip layer has been completely removed and all functionality has been moved the the chip layer. Files in this area had to be selectively added to projects 'per device' along with chip layer code - adding is no longer needed. Removing this layer has also allow the chip layer code to be a bit smaller. In almost all cases, the Chip layer APIs were not altered with this change.
    - Chip layer changes (./lpcopen/lpc_core/lpc_chip/<chip>)
        - All chip layer code for a specific device family can now be (mass) added to a single project and only the files specific to the device in that family will built
        - The 'sys_config.h'' file is now a chip file and only details which CHIP_* definition to use when build ing the code. Pre-populated sys_config.h files are available for all supported devices in a single family in the chip layer area. Just add the include path for your device to your project to build for that specific device
        - A chip specific Chip_SystemInit() is now provided that sets up the system to boot using the IRC/PLL, but doesn't setup pin muxing or memory
        - Moved SystemCoreClockUpdate() function and SystemCoreClock variable from board the chip layer
    - Board layer changes (./lpcopen/lpc_core/lpc_board/<chip>/<board>)
        - Named board header file merged with board.h (this extra named file wasn't needed)
        - DEBUG_* definitions used to control DEBUG_* functions are now part of the board.h file
        - Named board source and system init files renamed to generic named files board.c and board_sysinit.c (allows simply overwriting the files to change the board)
        - SystemInit() function renamed to Board_SystemInit()
    - FreeRTOS source code updated from v7.3.0 to V7.4.2
    - Package release model changed from flat/combined release to include packaged Keil/IAR release and dedicated LPCXpresso archive
    - Very minor API changes for some drivers
    - Keil and IAR projects are relocated into a central area and are 'per board' instead of 'per device'
        - This prevents projects that have support for many boards and selection of the wrong target board
        - Allows easier packaging of LPCOpen 'per board' and easier long-term maintainenece of the projects
    - LPCXpresso projects have been replaced by LPCXpresso project XML import files
        - The import files can be used to generate the LPCXpresso projects in the LPCOpen flast release by simply importing them
    - The file containing SystemInit() is included in each project example now
- LPC8xx only changes
    - Major rewrite of some LPC8xx drivers

    - New ring buffer based UART driver, improved GPIO functions, new PININT driver
    - Improvements and new functions for FMC, PMU, SYSCON, IOCON, WKT, MRT, CRC, WDT, ROM APIs
    - Uses enumeration for indexing IOCON registers: Example: LPC_IOCON->PIO0[IOCON_PIO0] = 0x1; // LPC_IOCON->PIO0[0] is not correct!
  - Added additional examples for SCT, UART, GPIO/PINIT, ROM APIs, etc. Improved some existing examples
    - Some projects support CRP and MTB
  - SystemInit() code has the option of using the ROM PLL setup functions instead of the clock driver

Known issues (Carried Forward)

- Periph_i2c_rom_slave example builds and runs, but does not work correctly.

How to Reach Us

Home Page: www.nxp.com
Web Support: www.nxp.com/support

USA/Europe or Locations Not Listed:
NXP Semiconductor
Technical Information Center,
EL516 2100 East Elliot Road
Tempe, Arizona 85284 +1-800-
521-6274 or +1-480-768-2130
www.nxp.com/support

Europe, Middle East, and Africa:
NXPHalbleiter Deutschland
GmbH Technical Information
Center Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.nxp.com/support

Japan:
NXP Semiconductor
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-
ku, Tokyo 153-0064, Japan
0120 191014 or +81 3 5437
9125 support.japan@nxp.com

Asia/Pacific:
NXP Semiconductor Hong Kong
Ltd. Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong
Kong +800 2666 8080
support.asia@nxp.com

Contributor/Author
Name
Title