

# **LPV321 Single/LPV358 Dual/LPV324 Quad General Purpose, Low Voltage, Low Power, Rail-to-Rail Output Operational Amplifiers**

Check for Samples: [LPV321-N](#), [LPV324-N](#), [LPV358-N](#)

## **FEATURES**

(For  $V^+ = 5V$  and  $V^- = 0V$ , typical unless otherwise noted)

- **Guaranteed 2.7V and 5V performance**
- **No crossover distortion**
- **Space saving package**
  - 5-Pin SC70 2.0x2.1x1.0 mm
- **Industrial temperature range,  $-40^{\circ}C$  to  $+85^{\circ}C$**
- **Gain-bandwidth product, 152 kHz**
- **Low supply current**
  - LPV321, 9  $\mu A$

- LPV358, 15  $\mu A$
- LPV324, 28  $\mu A$
- **Rail-to-rail output swing @ 100 k $\Omega$  Load**
  - $V^+ - 3.5$  mV
  - $V^- + 90$  mV
- $V_{CM}$ ,  $-0.2V$  to  $V^+ - 0.8V$

## **APPLICATIONS**

- **Active filters**
- **General purpose low voltage applications**
- **General purpose portable devices**

## **DESCRIPTION**

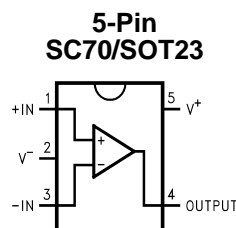
The LPV321/358/324 are low power (9  $\mu A$  per channel at 5.0V) versions of the LMV321/358/324 op amps. This is another addition to the LMV321/358/324 family of commodity op amps.

The LPV321/358/324 are the most cost effective solutions for the applications where low voltage, low power operation, space saving and low price are needed. The LPV321/358/324 have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed-power ratio, achieving 5 kHz of bandwidth with a supply current of only 9  $\mu A$ .

The LPV321 is available in space saving 5-Pin SC70, which is approximately half the size of 5-Pin SOT23. The small package saves space on PC boards, and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The chips are built with National's advanced submicron silicon-gate BiCMOS process. The LPV321/358/324 have bipolar input and output stages for improved noise performance and higher output current drive.

## **Connection Diagram**



**Figure 1. Top View**



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### 8-Pin SOIC/MSOP

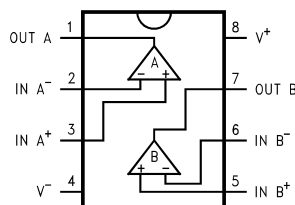


Figure 2. Top View

### 14-Pin SOIC/TSSOP

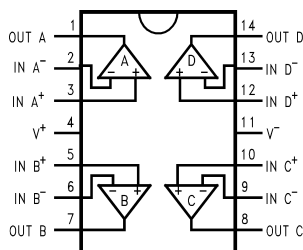


Figure 3. Top View



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings <sup>(1)</sup>

ESD Tolerance <sup>(2)</sup>	
Human Body Model	
LPV324	2000V
LPV358	1500V
LPV321	1500V
Machine Model	
	100V
Differential Input Voltage	±Supply Voltage
Supply Voltage (V <sup>+</sup> –V <sup>–</sup> )	5.5V
Output Short Circuit to V <sup>+</sup>	<sup>(3)</sup>
Output Short Circuit to V <sup>–</sup>	<sup>(4)</sup>
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temperature Range	–65°C to 150°C
Junction Temp. (T <sub>J</sub> , max) <sup>(5)</sup>	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

(3) Shorting output to V<sup>+</sup> will adversely affect reliability.

(4) Shorting output to V<sup>–</sup> will adversely affect reliability.

(5) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> – T<sub>A</sub>)/ θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

**Operating Ratings** <sup>(1)</sup>

Supply Voltage	2.7V to 5V
Temperature Range	–40°C to +85°C
Thermal Resistance ( $\theta_{JA}$ ) <sup>(2)</sup>	
5-Pin SC70	478°C/W
5-Pin SOT23	265°C/W
8-Pin SOIC	190°C/W
8-Pin MSOP	235°C/W
14-Pin SOIC	145°C/W
14-Pin TSSOP	155°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) All numbers are typical, and apply for packages soldered directly onto a PC board in still air.

## 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 1.0\text{V}$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
$V_{OS}$	Input Offset Voltage			1.2	7	mV
$TCV_{OS}$	Input Offset Voltage Average Drift			2		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current			1.7	50	nA
$I_{OS}$	Input Offset Current			0.6	40	nA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 1.7\text{V}$	50	70		dB
PSRR	Power Supply Rejection Ratio	$2.7\text{V} \leq V^+ \leq 5\text{V}$ $V_O = 1\text{V}$ , $V_{CM} = 1\text{V}$	50	65		dB
$V_{CM}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{ dB}$	0	-0.2		V
				1.9	1.7	
$V_O$	Output Swing	$R_L = 100\text{ k}\Omega$ to $1.35\text{V}$	$V^+ - 100$	$V^+ - 3$		mV
				80	180	mV
$I_S$	Supply Current	LPV321		4	8	$\mu\text{A}$
		LPV358 Both Amplifiers		8	16	$\mu\text{A}$
		LPV324 All Four Amplifiers		16	24	$\mu\text{A}$

- (1) All limits are guaranteed by testing or statistical analysis.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

## 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 1.0\text{V}$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
GBWP	Gain-Bandwidth Product	$C_L = 22\text{ pF}$		112		kHz
$\Phi_m$	Phase Margin			97		Deg
$G_m$	Gain Margin			35		dB
$e_n$	Input-Referred Voltage Noise	$f = 1\text{ kHz}$		178		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$		0.50		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$

- (1) All limits are guaranteed by testing or statistical analysis.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

## 5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 2.0\text{V}$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
$V_{OS}$	Input Offset Voltage			1.5	<b>7</b> <b>10</b>	mV
$TCV_{OS}$	Input Offset Voltage Average Drift			2		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current			2	<b>50</b> <b>60</b>	nA
$I_{OS}$	Input Offset Current			0.6	<b>40</b> <b>50</b>	nA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 4\text{V}$	50	71		dB
PSRR	Power Supply Rejection Ratio	$2.7\text{V} \leq V^+ \leq 5\text{V}$ $V_O = 1\text{V}$ , $V_{CM} = 1\text{V}$	50	65		dB
$V_{CM}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{ dB}$	0	-0.2		V
				4.2	4	
$A_V$	Large Signal Voltage Gain (3)	$R_L = 100\text{ k}\Omega$	<b>15</b> <b>10</b>	100		V/mV
$V_O$	Output Swing	$R_L = 100\text{ k}\Omega$ to $2.5\text{V}$	$V^+ - 100$ $V^+ - 200$	$V^+ - 3.5$		mV
				90	<b>180</b> <b>220</b>	
$I_O$	Output Short Circuit Current Sourcing	LPV324, LPV358, and LPV321 $V_O = 0\text{V}$	2	16		mA
	Output Short Circuit Current Sinking	LPV321 $V_O = 5\text{V}$	20	60		mA
		LPV324 and LPV358 $V_O = 5\text{V}$	11	16		mA
$I_S$	Supply Current	LPV321		9	<b>12</b> <b>15</b>	$\mu\text{A}$
		LPV358 Both amplifiers		15	<b>20</b> <b>24</b>	$\mu\text{A}$
		LPV324 All four amplifiers		28	<b>42</b> <b>46</b>	$\mu\text{A}$

(1) All limits are guaranteed by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(3)  $R_L$  is connected to  $V^-$ . The output voltage is  $0.5\text{V} \leq V_O \leq 4.5\text{V}$ .

## 5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 2.0\text{V}$ ,  $V_O = V^+/2$  and  $R_L > 1\text{M}\Omega$ .

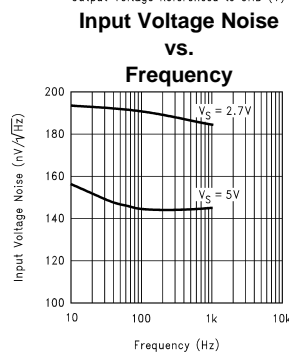
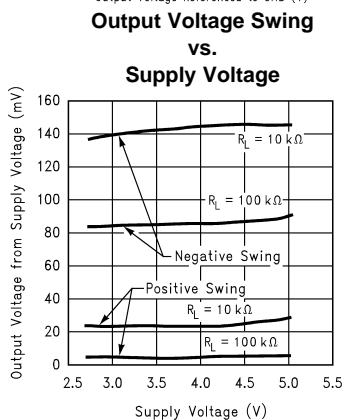
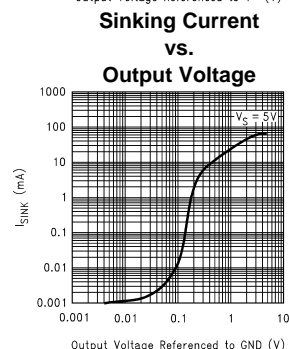
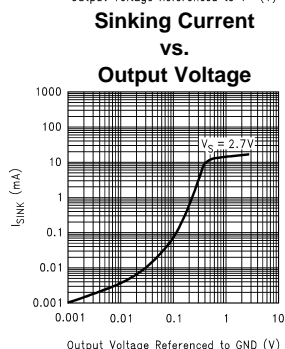
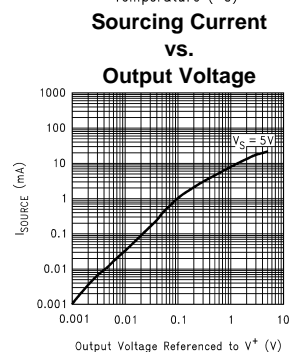
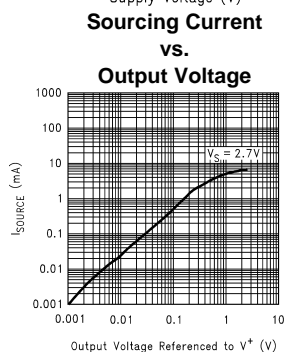
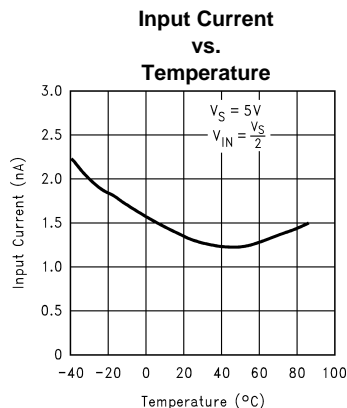
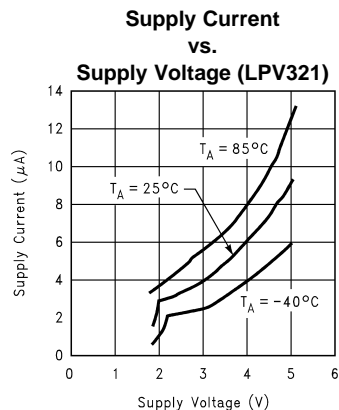
**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Min (1)	Units
SR	Slew Rate	(3)		0.1		V/ $\mu\text{s}$
GBWP	Gain-Bandwidth Product	$C_L = 22\text{ pF}$		152		kHz
$\Phi_m$	Phase Margin			87		Deg
$G_m$	Gain Margin			19		dB
$e_n$	Input-Referred Voltage Noise	$f = 1\text{ kHz}$ ,		146		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$		0.30		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$

- (1) All limits are guaranteed by testing or statistical analysis.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (3) Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

## Typical Performance Characteristics

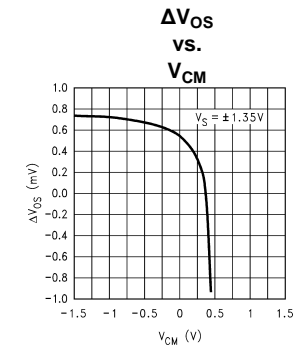
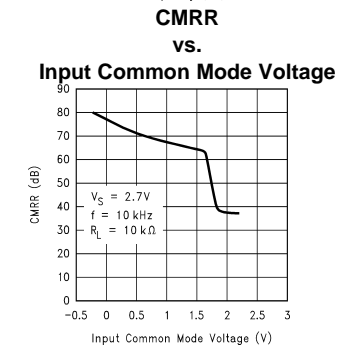
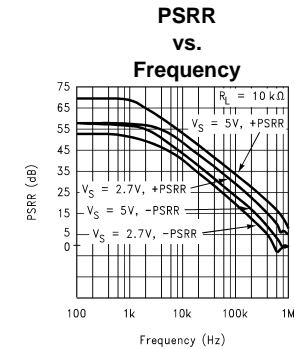
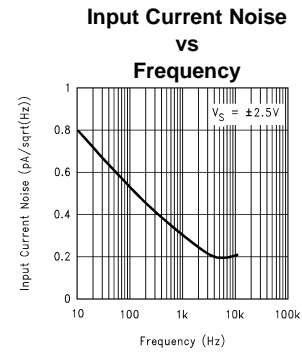
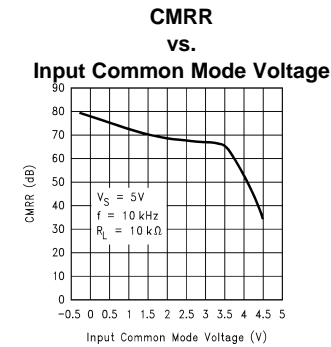
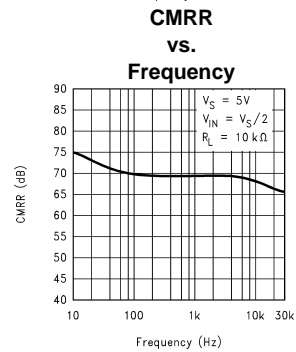
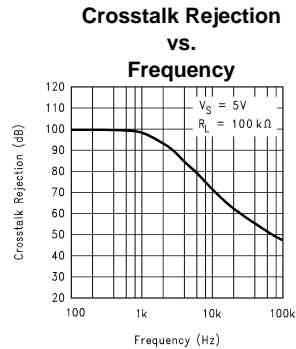
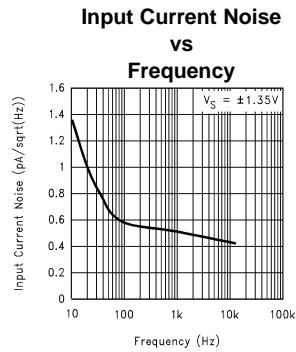
Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .





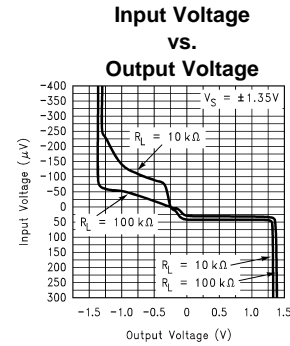
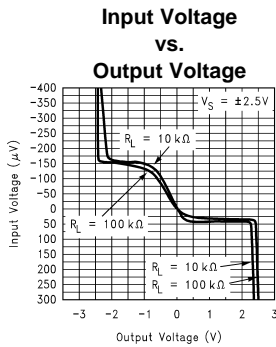
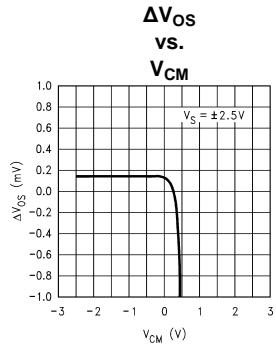
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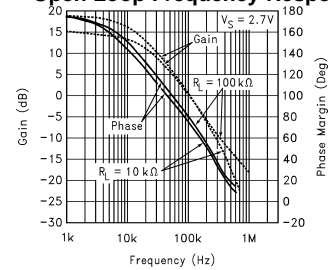


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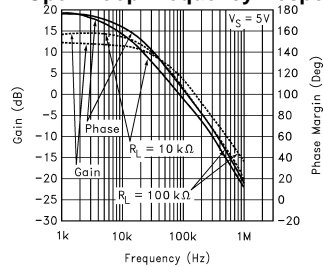
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### Open Loop Frequency Response



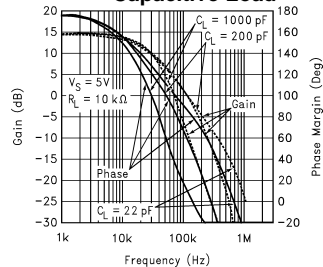
### Open Loop Frequency Response



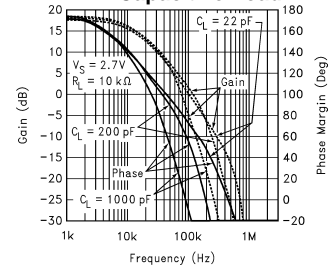
### Gain and Phase

vs.

### Capacitive Load



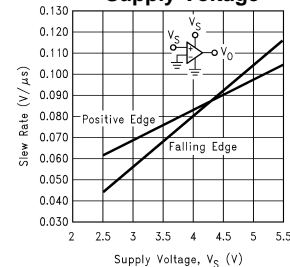
### Capacitive Load



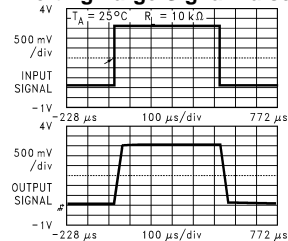
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vs.

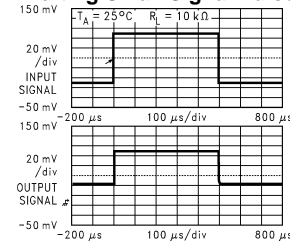
### Supply Voltage



### Non-Inverting Large Signal Pulse Response



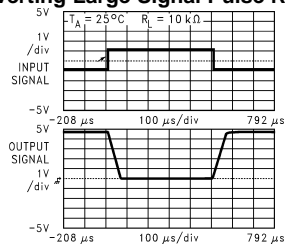
### Non-Inverting Small Signal Pulse Response



## Typical Performance Characteristics (continued)

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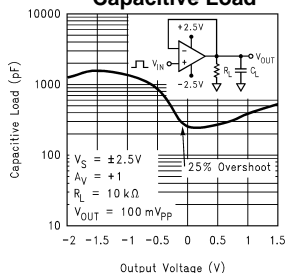
### Inverting Large Signal Pulse Response



Stability

vs.

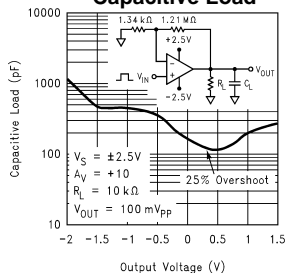
### Capacitive Load



Stability

vs.

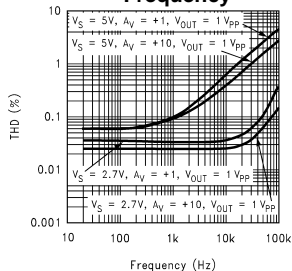
### Capacitive Load



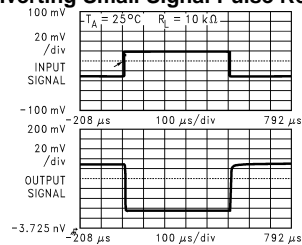
THD

vs.

### Frequency



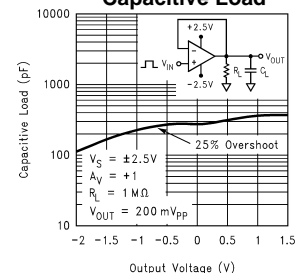
### Inverting Small Signal Pulse Response



Stability

vs.

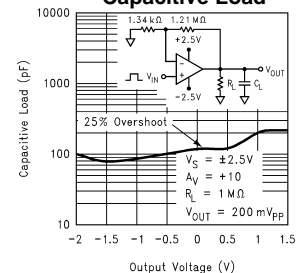
### Capacitive Load



Stability

vs.

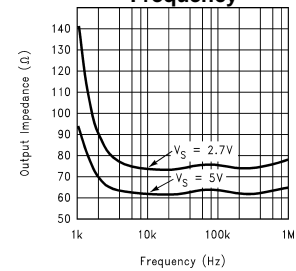
### Capacitive Load



### Open Loop Output Impedance

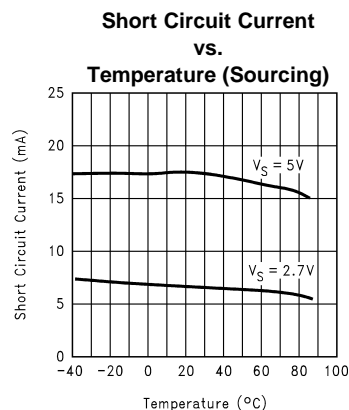
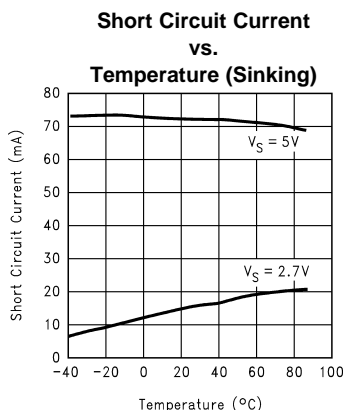
vs.

### Frequency



## Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .



## Application Information

### BENEFITS OF THE LPV321/358/324

#### Size

The small footprints of the LPV321/358/324 packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. The low profile of the LPV321/358/324 make them possible to use in PCMCIA type III cards.

#### Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LPV321/358/324 can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

#### Simplified Board Layout

These products help you to avoid using long pc traces in your pc board layout. This means that no additional components, such as capacitors and resistors, are needed to filter out the unwanted signals due to the interference between the long pc traces.

#### Low Supply Current

These devices will help you to maximize battery life. They are ideal for battery powered systems.

#### Low Supply Voltage

National provides guaranteed performance at 2.7V and 5V. These guarantees ensure operation throughout the battery lifetime.

#### Rail-to-Rail Output

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

#### Input Includes Ground

Allows direct sensing near GND in single supply operation.

The differential input voltage may be larger than  $V^+$  without damaging the device. Protection should be provided to prevent the input voltages from going negative more than  $-0.3V$  (at  $25^\circ C$ ). An input clamp diode with a resistor to the IC input terminal can be used.

## CAPACITIVE LOAD TOLERANCE

The LPV321/358/324 can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, circuit in Figure 4 can be used.

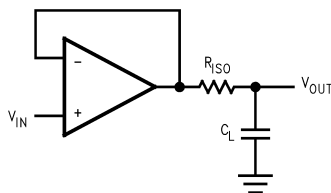


Figure 4. Indirectly Driving A Capacitive Load Using Resistive Isolation

In Figure 4, the isolation resistor  $R_{ISO}$  and the load capacitor  $C_L$  form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of  $R_{ISO}$ . The bigger the  $R_{ISO}$  resistor value, the more stable  $V_{OUT}$  will be. Figure 5 is an output waveform of Figure 4 using 100 k $\Omega$  for  $R_{ISO}$  and 1000 pF for  $C_L$ .

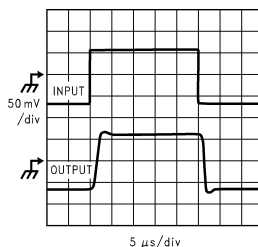


Figure 5. Pulse Response of the LPV324 Circuit in Figure 4

The circuit in Figure 6 is an improvement to the one in Figure 4 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 4, the output would be voltage divided by  $R_{ISO}$  and the load resistor. Instead, in Figure 6,  $R_F$  provides the DC accuracy by using feed-forward techniques to connect  $V_{IN}$  to  $R_L$ . Caution is needed in choosing the value of  $R_F$  due to the input bias current of the LPV321/358/324.  $C_F$  and  $R_{ISO}$  serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of  $C_F$ . This in turn will slow down the pulse response.

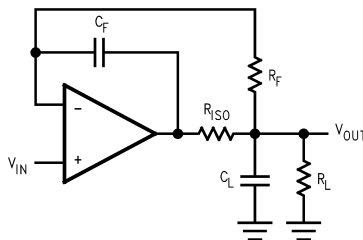


Figure 6. Indirectly Driving A Capacitive Load with DC Accuracy

## INPUT BIAS CURRENT CANCELLATION

The LPV321/358/324 family has a bipolar input stage. The typical input bias current of LPV321/358/324 is 1.5 nA with 5V supply. Thus a 100 k $\Omega$  input resistor will cause 0.15 mV of error voltage. By balancing the resistor values at both inverting and non-inverting inputs, the error caused by the amplifier's input bias current will be reduced. The circuit in Figure 7 shows how to cancel the error caused by input bias current.

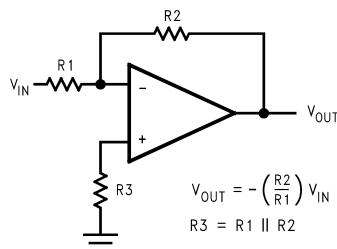


Figure 7. Cancelling the Error Caused by Input Bias Current

## TYPICAL SINGLE-SUPPLY APPLICATION CIRCUITS

### Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.

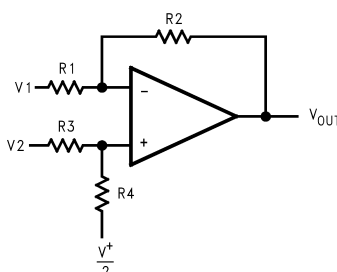


Figure 8. Difference Amplifier

$$V_{OUT} = \left( \frac{R_1 + R_2}{R_3 + R_4} \right) \frac{R_4}{R_1} V_2 - \frac{R_2}{R_1} V_1 + \left( \frac{R_1 + R_2}{R_3 + R_4} \right) \frac{R_3}{R_1} \cdot \frac{V^+}{2}$$

for  $R_1 = R_3$  and  $R_2 = R_4$

$$V_{OUT} = \frac{R_2}{R_1} (V_2 - V_1) + \frac{V^+}{2}$$

(1)

### Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistor  $R_1$ ,  $R_2$ ,  $R_3$ , and  $R_4$ . To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.

### Three-op-amp Instrumentation Amplifier

The quad LPV324 can be used to build a three-op-amp instrumentation amplifier as shown in [Figure 9](#)

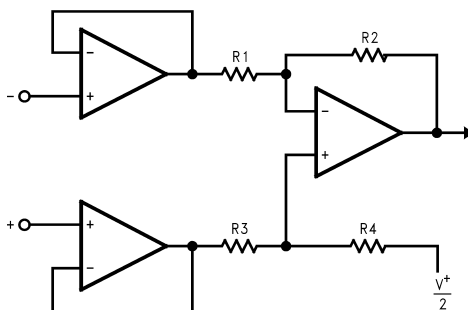


Figure 9. Three-op-amp Instrumentation Amplifier

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100 MΩ. The gain of this instrumentation amplifier is set by the ratio of  $R_2/R_1$ .  $R_3$  should equal  $R_1$  and  $R_4$  equal  $R_2$ . Matching of  $R_3$  to  $R_1$  and  $R_4$  to  $R_2$  affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making  $R_4$  slightly smaller than  $R_2$  and adding a trim pot equal to twice the difference between  $R_2$  and  $R_4$  will allow the CMRR to be adjusted for optimum.

### Two-op-amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier can also be used to make a high-input-impedance DC differential amplifier (Figure 10). As in the three-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR.  $R_4$  should equal to  $R_1$  and  $R_3$  should equal  $R_2$ .

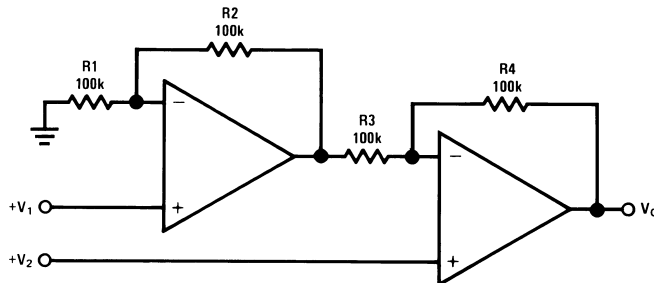


Figure 10. Two-op-amp Instrumentation Amplifier

$$V_O = \left(1 + \frac{R_4}{R_3}\right)(V_2 - V_1), \text{ where } R_1 = R_4 \text{ and } R_2 = R_3$$

$$\text{As shown: } V_O = 2(V_2 - V_1)$$

(2)

### Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using  $R_3$  and  $R_4$  is implemented to bias the amplifier so the input signal is within the input common-mode voltage range of the amplifier. The capacitor  $C_1$  is placed between the inverting input and resistor  $R_1$  to block the DC signal going into the AC signal source,  $V_{IN}$ . The values of  $R_1$  and  $C_1$  affect the cutoff frequency,  $f_c = 1/2\pi R_1 C_1$ .

As a result, the output signal is centered around mid-supply (if the voltage divider provides  $V^+/2$  at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.

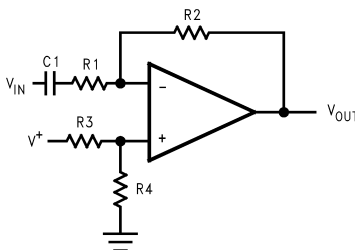


Figure 11. Single-Supply Inverting Amplifier

$$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$$

(3)

## ACTIVE FILTER

### Simple Low-Pass Active Filter

The simple low-pass filter is shown in Figure 12. Its low-frequency gain ( $\omega \rightarrow 0$ ) is defined by  $-R_3/R_1$ . This allows low-frequency gains other than unity to be obtained. The filter has a  $-20$  dB/decade roll-off after its corner frequency  $f_c$ .  $R_2$  should be chosen equal to the parallel combination of  $R_1$  and  $R_3$  to minimize errors due to bias current. The frequency response of the filter is shown in Figure 13

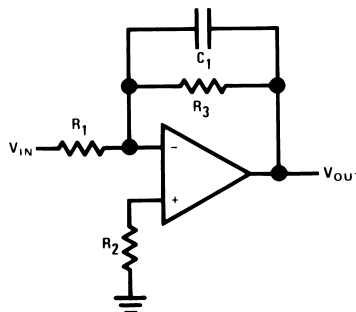


Figure 12. Simple Low-Pass Active Filter

$$A_L = -\frac{R_3}{R_1}$$

$$f_c = \frac{1}{2\pi R_3 C_1}$$

$$R_2 = R_1 \parallel R_3$$

(4)

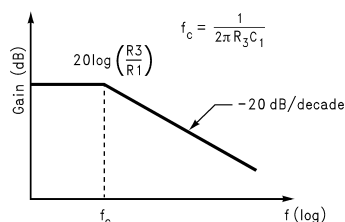


Figure 13. Frequency Response of Simple Low-pass Active Filter in Figure 9

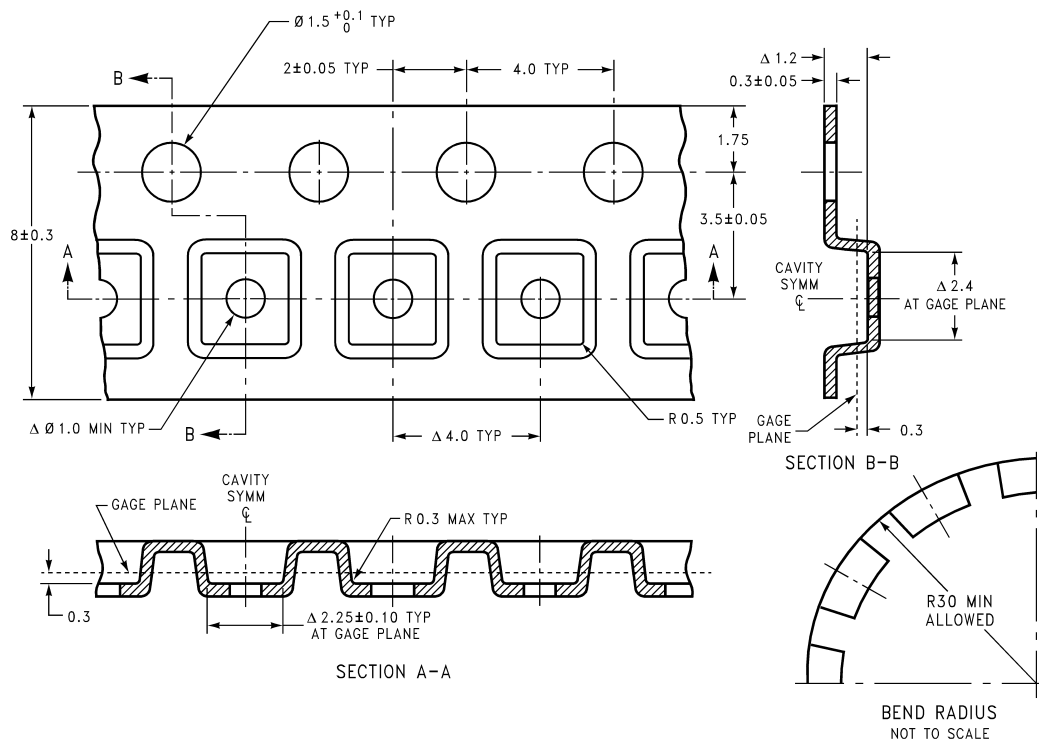
Note that the single-op-amp active filters are used in to the applications that require low quality factor,  $Q (\leq 10)$ , low frequency ( $\leq 5$  kHz), and low gain ( $\leq 10$ ), or a small value for the product of gain times  $Q (\leq 100)$ . The op amp should have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp should have a slew rate that meets the following requirement:

$$\text{Slew Rate} \geq 0.5 \times (\omega_H V_{OPP}) \times 10^{-6} \text{V}/\mu\text{sec}$$

Where  $\omega_H$  is the highest frequency of interest, and  $V_{OPP}$  is the output peak-to-peak voltage.



## SC70-5 Tape and Reel Specification

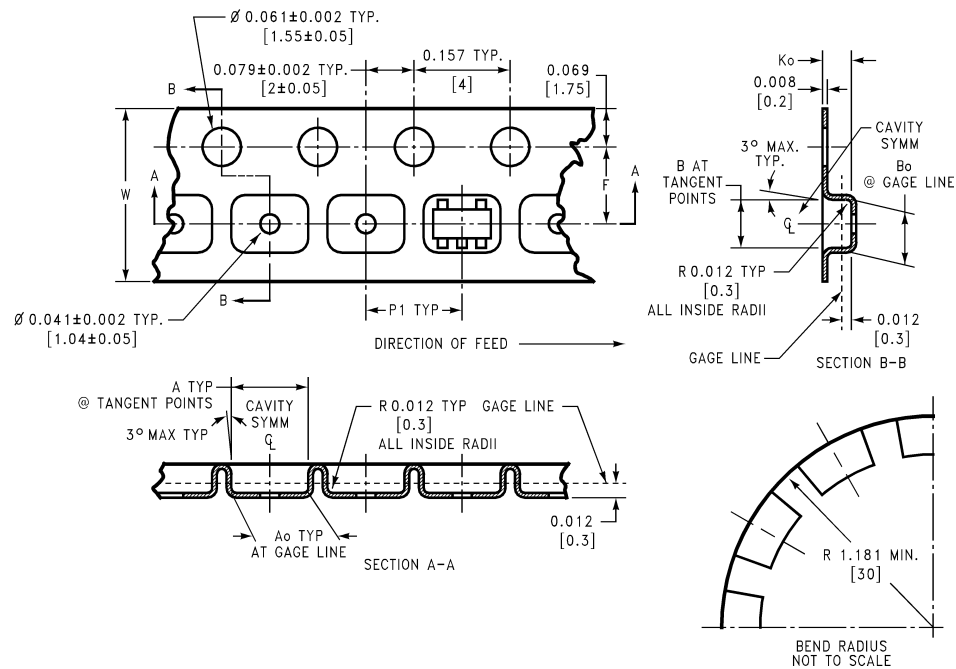


## SOT-23-5 Tape and Reel Specification

### TAPE FORMAT

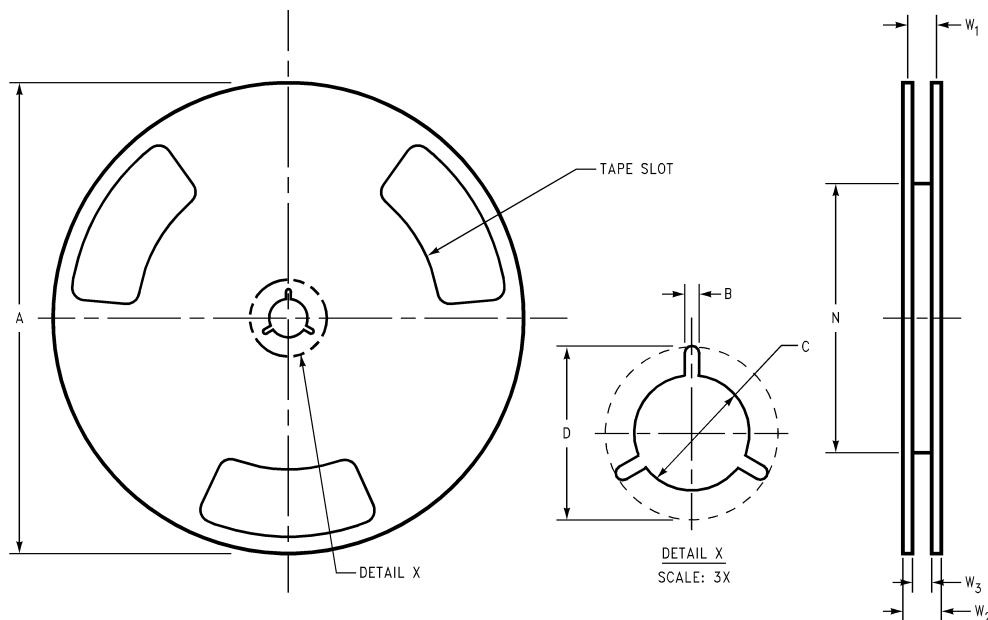
Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader	0 (min)	Empty	Sealed
(Start End)	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer	125 (min)	Empty	Sealed
(Hub End)	0 (min)	Empty	Sealed

## TAPE DIMENSIONS



8 mm	0.130	0.124	0.130	0.126	0.138 $\pm$ 0.002	0.055 $\pm$ 0.004	0.157	0.315 $\pm$ 0.012
	(3.3)	(3.15)	(3.3)	(3.2)	(3.5 $\pm$ 0.05)	(1.4 $\pm$ 0.11)	(4)	(8 $\pm$ 0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

## REEL DIMENSIONS



8 mm	7.00	0.059	0.512	0.795	2.165	0.331 + 0.059/-0.000	0.567	W1+ 0.078/-0.039
	330.00	1.50	13.00	20.20	55.00	8.40 + 1.50/-0.00	14.40	W1 + 2.00/-1.00
Tape Size	A	B	C	D	N	W1	W2	W3

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LPV321M5	ACTIVE	SOT-23	DBV	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A27A	<a href="#">Samples</a>
LPV321M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A27A	<a href="#">Samples</a>
LPV321M5X	ACTIVE	SOT-23	DBV	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A27A	<a href="#">Samples</a>
LPV321M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A27A	<a href="#">Samples</a>
LPV321M7	ACTIVE	SC70	DCK	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A19	<a href="#">Samples</a>
LPV321M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A19	<a href="#">Samples</a>
LPV321M7X	ACTIVE	SC70	DCK	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A19	<a href="#">Samples</a>
LPV321M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A19	<a href="#">Samples</a>
LPV324M	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LPV324M	<a href="#">Samples</a>
LPV324M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV324M	<a href="#">Samples</a>
LPV324MT	ACTIVE	TSSOP	PW	14	94	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	LPV324 MT	<a href="#">Samples</a>
LPV324MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT	<a href="#">Samples</a>
LPV324MTX	ACTIVE	TSSOP	PW	14	2500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	LPV324 MT	<a href="#">Samples</a>
LPV324MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT	<a href="#">Samples</a>
LPV324MX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LPV324M	<a href="#">Samples</a>
LPV324MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV324M	<a href="#">Samples</a>
LPV358M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LPV 358M	<a href="#">Samples</a>
LPV358MM	ACTIVE	VSSOP	DGK	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	P358	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LPV358MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	P358	<a href="#">Samples</a>
LPV358MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	P358	<a href="#">Samples</a>
LPV358MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	P358	<a href="#">Samples</a>
LPV358MX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LPV 358M	<a href="#">Samples</a>
LPV358MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LPV 358M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

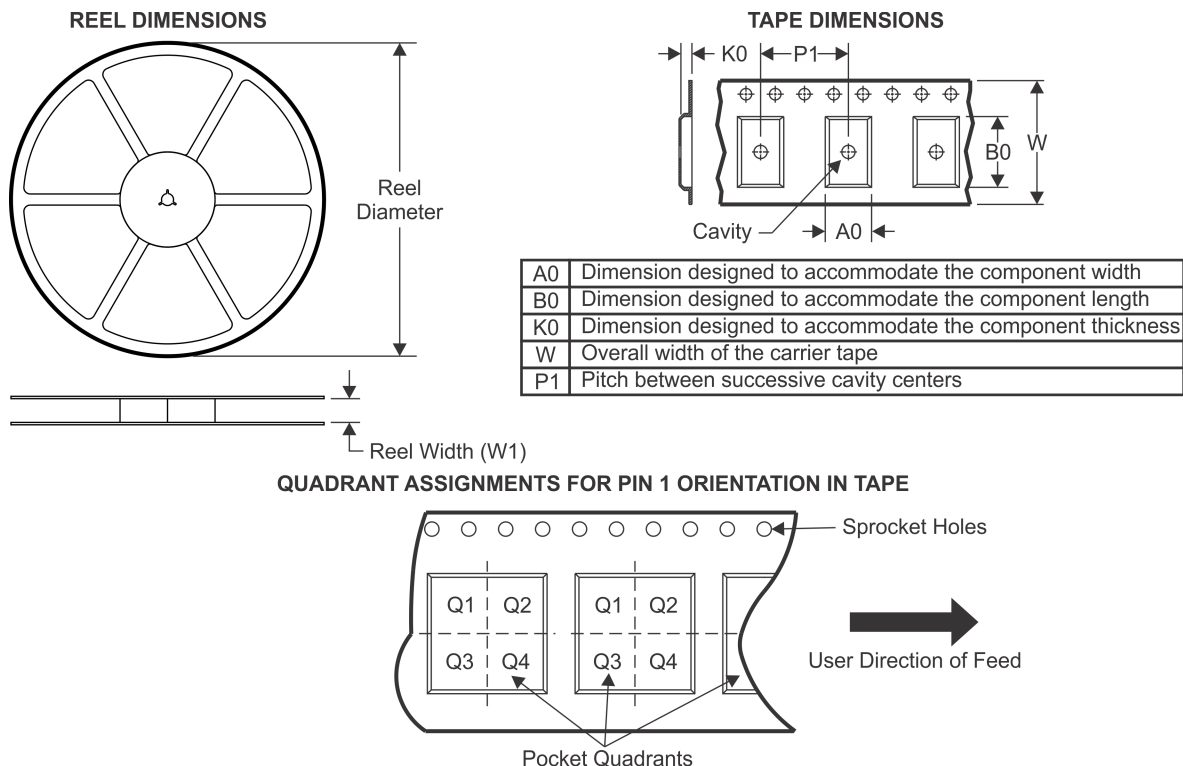
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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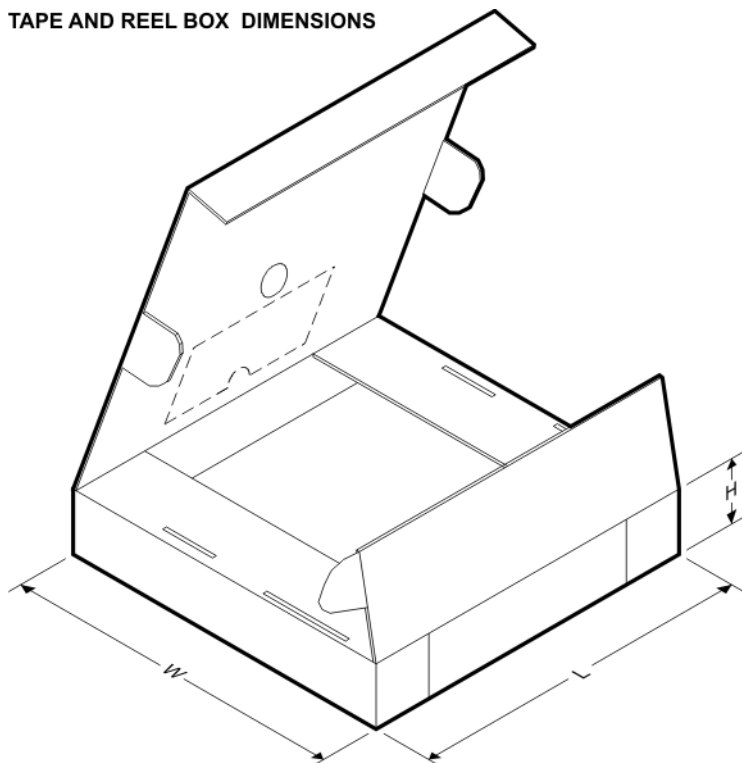


**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV321M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV321M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV321M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV321M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV321M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV321M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV321M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV321M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV324MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LPV324MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LPV324MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LPV324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LPV358MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LPV358MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

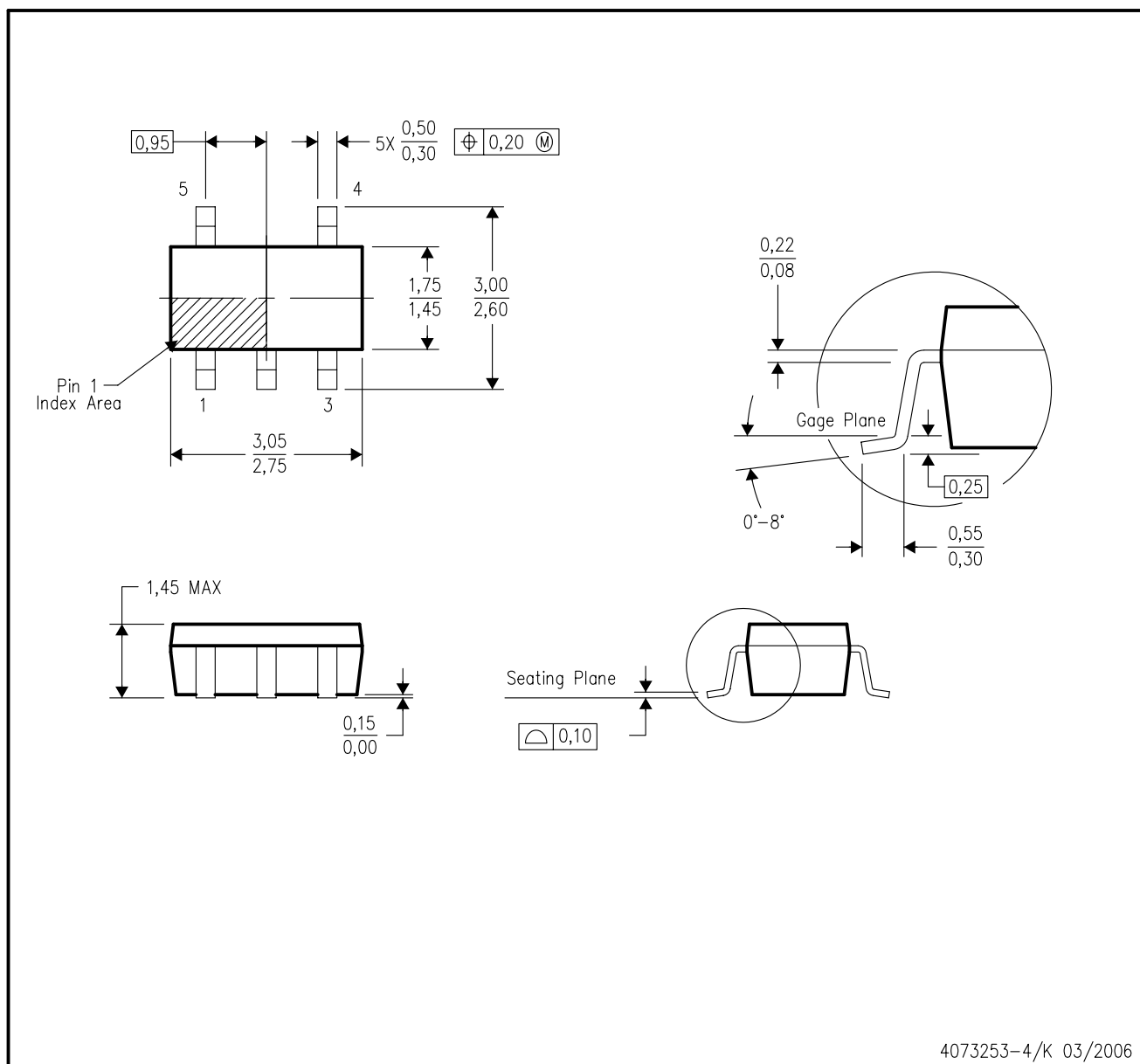


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV321M5	SOT-23	DBV	5	1000	203.0	190.0	41.0
LPV321M5/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LPV321M5X	SOT-23	DBV	5	3000	206.0	191.0	90.0
LPV321M5X/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LPV321M7	SC70	DCK	5	1000	203.0	190.0	41.0
LPV321M7/NOPB	SC70	DCK	5	1000	203.0	190.0	41.0
LPV321M7X	SC70	DCK	5	3000	206.0	191.0	90.0
LPV321M7X/NOPB	SC70	DCK	5	3000	206.0	191.0	90.0
LPV324MTX	TSSOP	PW	14	2500	349.0	337.0	45.0
LPV324MTX/NOPB	TSSOP	PW	14	2500	349.0	337.0	45.0
LPV324MX	SOIC	D	14	2500	349.0	337.0	45.0
LPV324MX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0
LPV358MM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LPV358MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LPV358MMX	VSSOP	DGK	8	3500	349.0	337.0	45.0
LPV358MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0
LPV358MX	SOIC	D	8	2500	349.0	337.0	45.0
LPV358MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

## DBV (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE

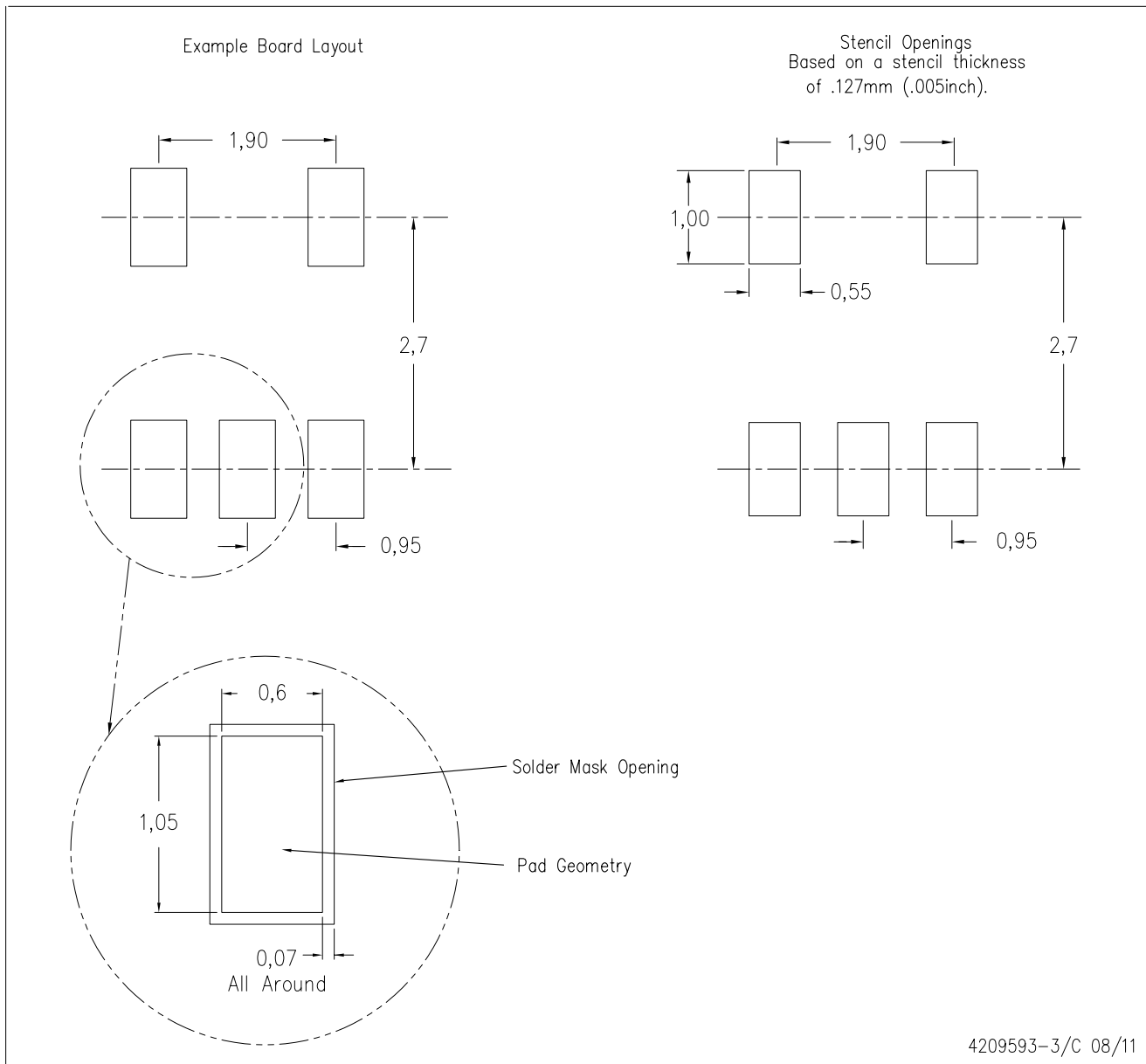


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

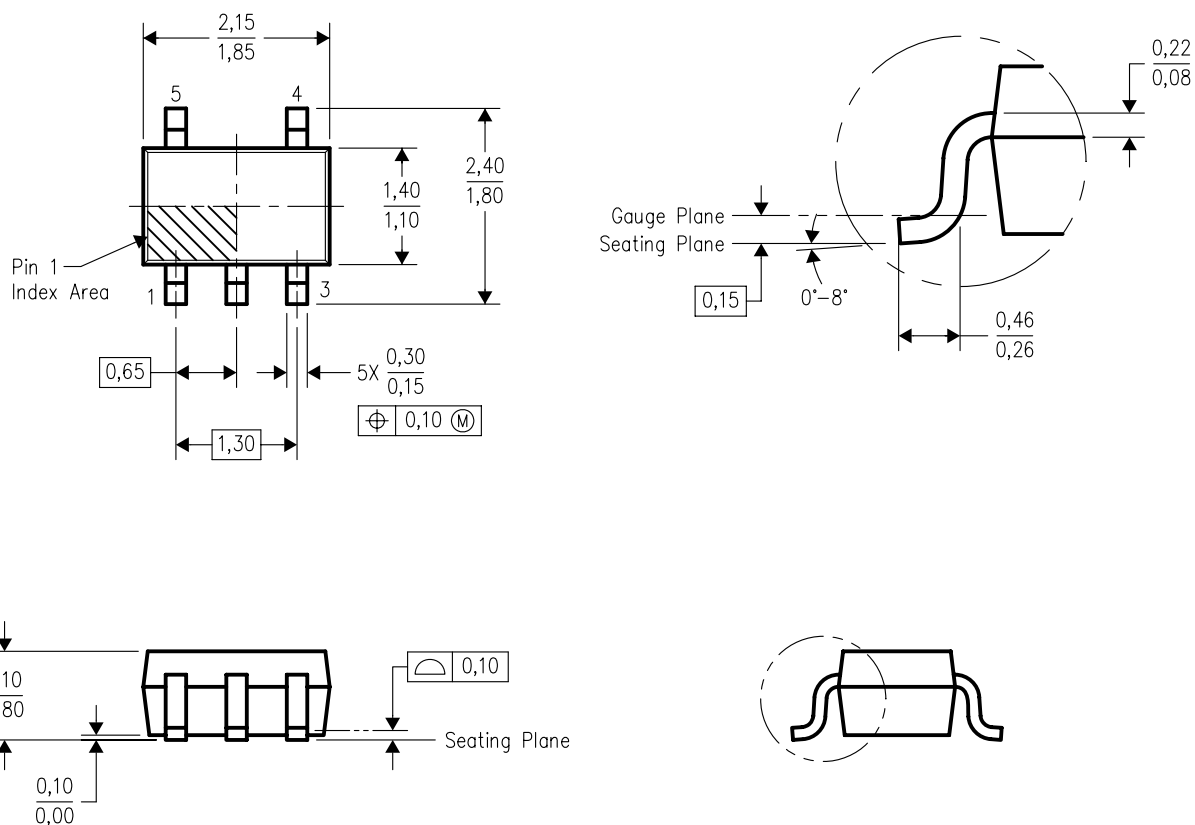
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE

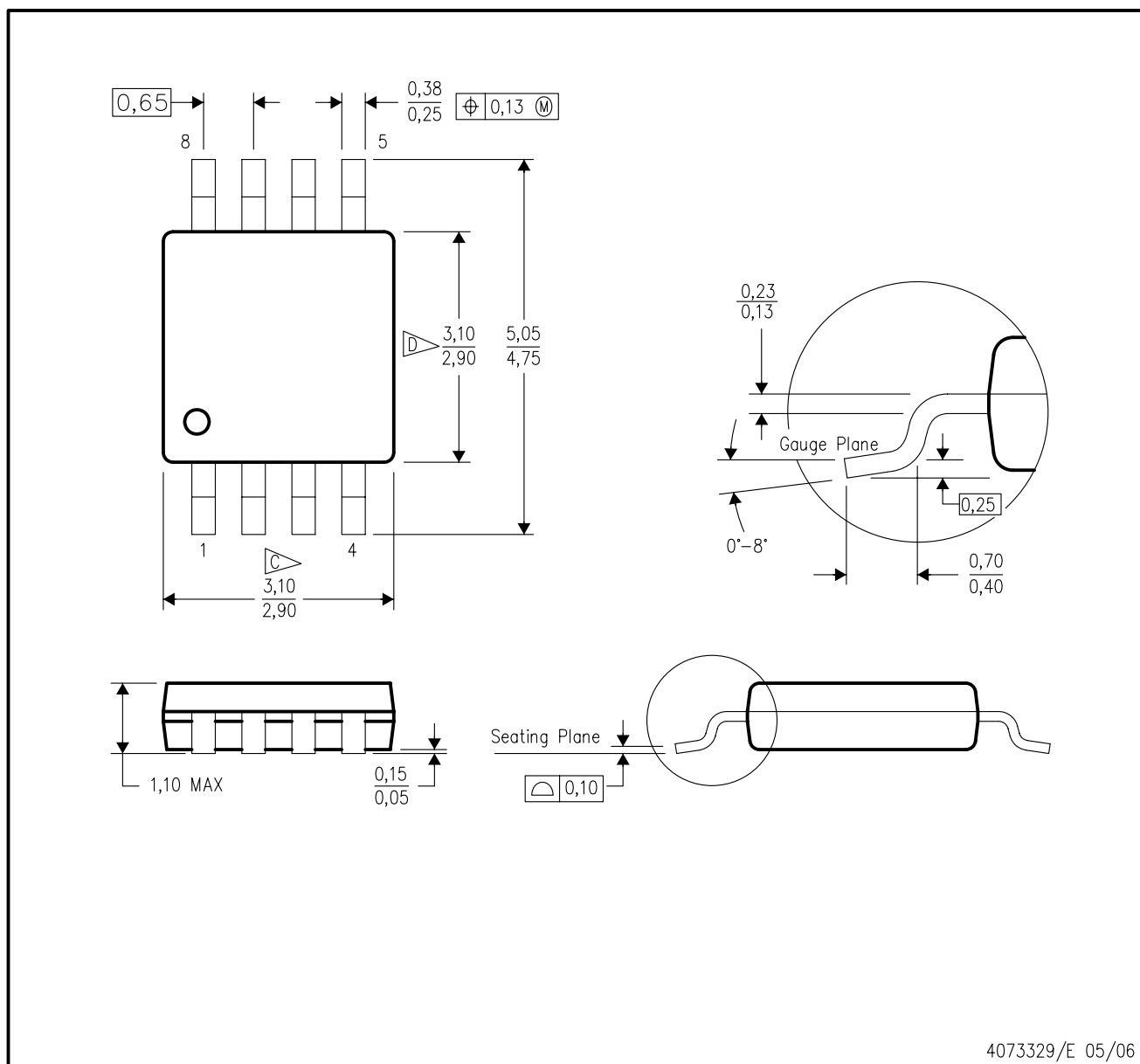


4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

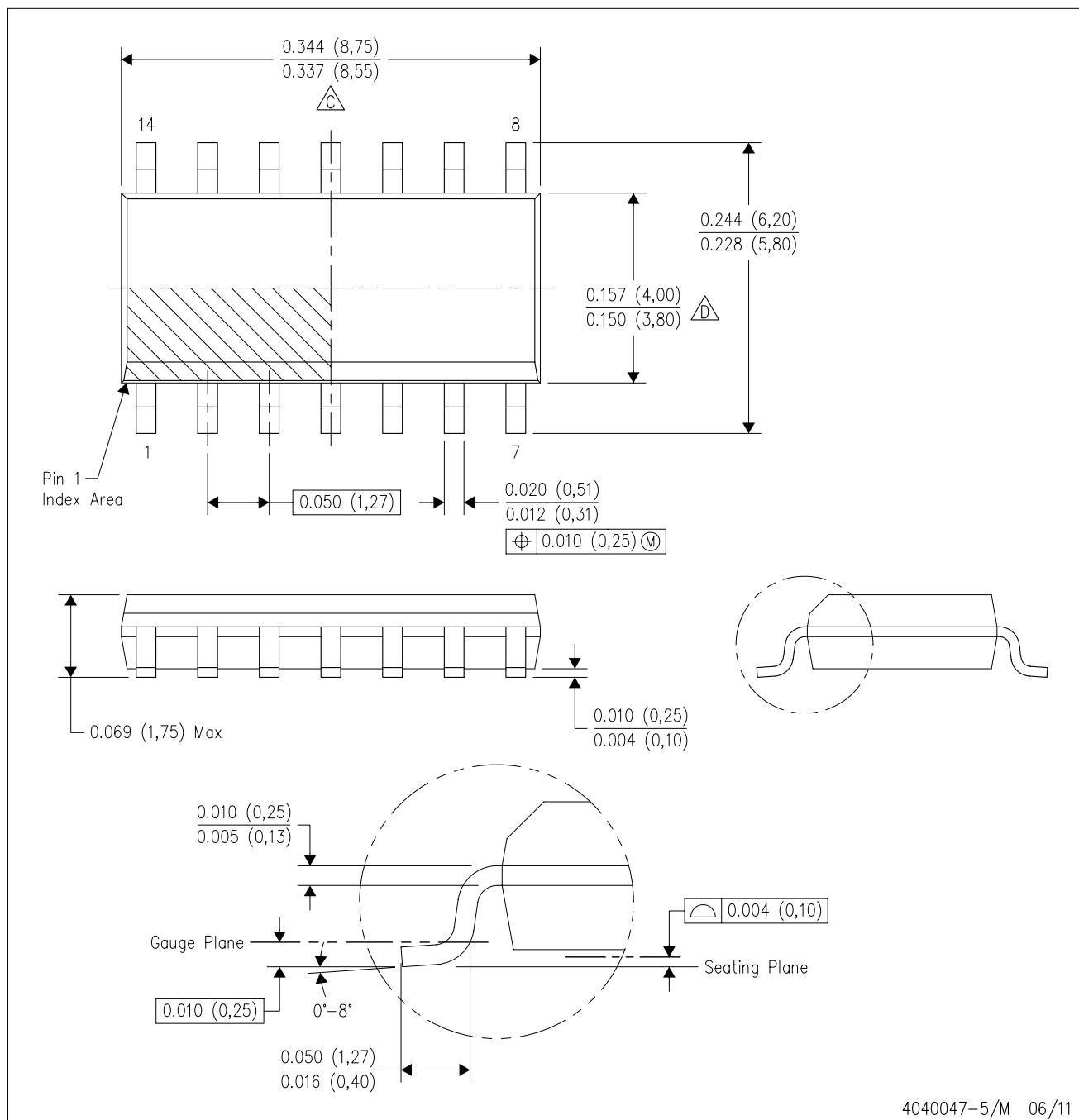


## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

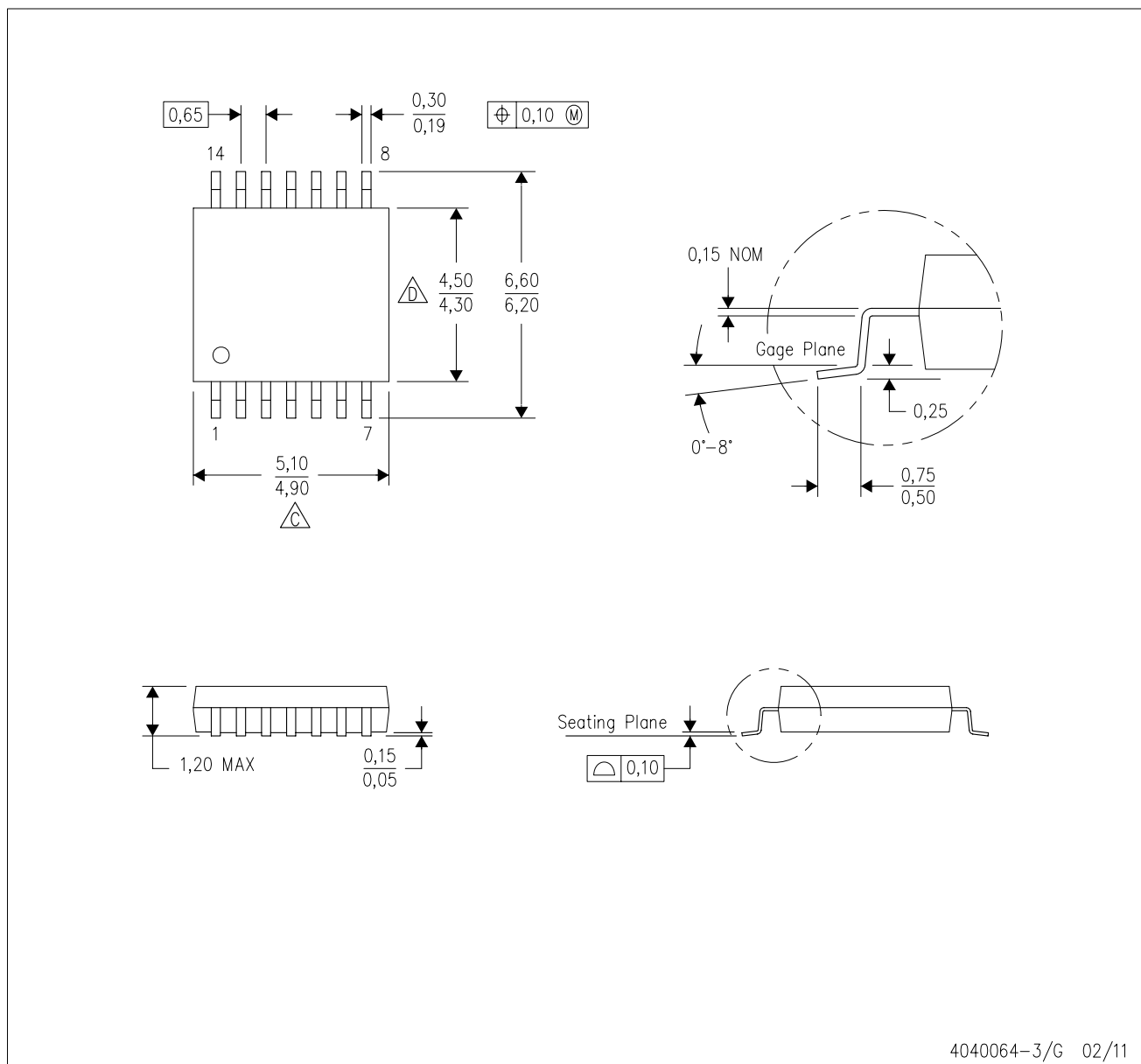


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

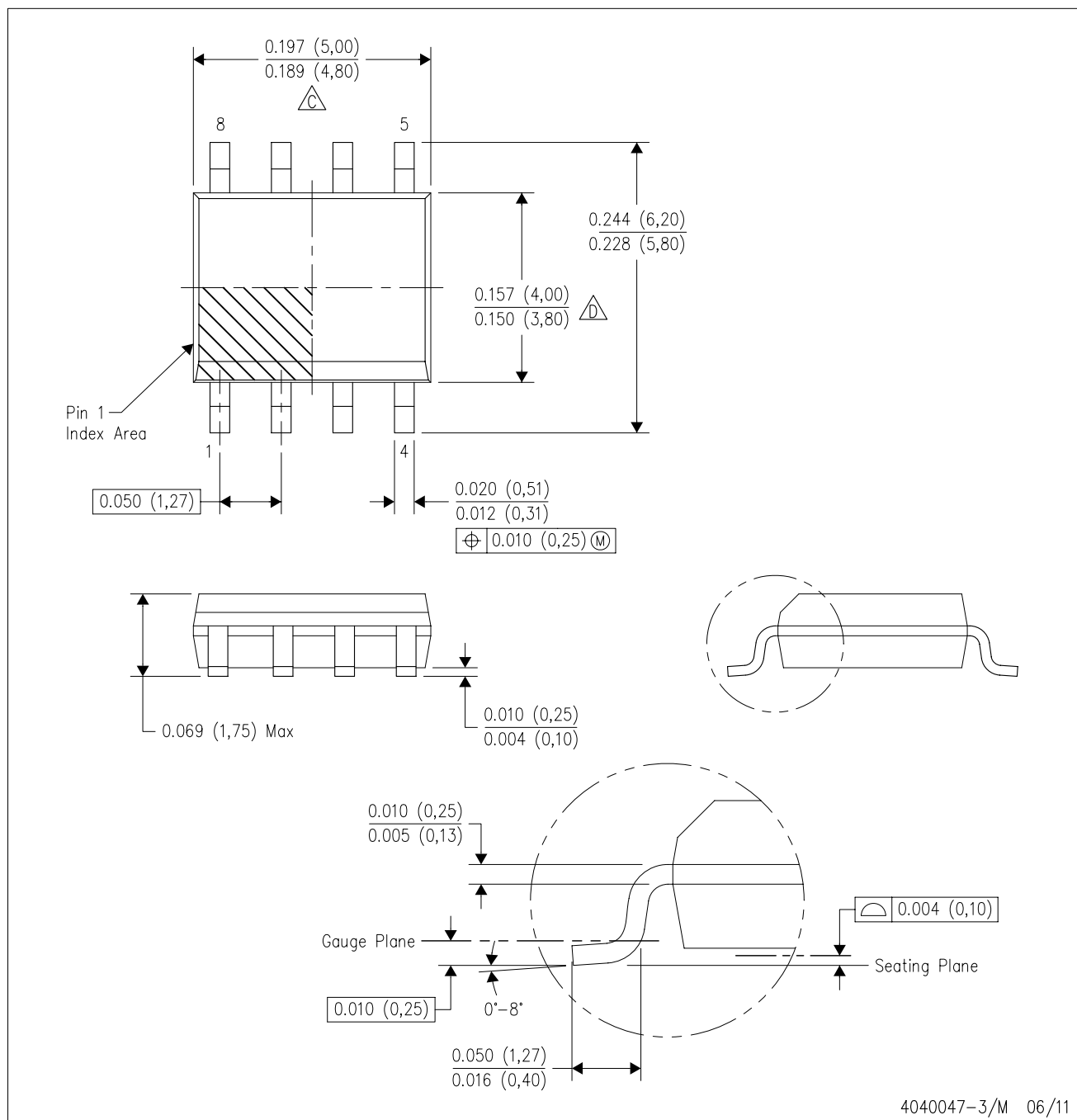
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
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