SGS LS045

LINEAR INTEGRATED CIRCUIT

CHANNEL AMPLIFIER

The LS 045 is a monolithic integrated circuit intended for use as channel amplifier in FDM and PCM telephone equipment. It features low quiescent power consumption, low distortion, high gain. The LS 045 is available in TO-99 metal case, while the hermetic gold chip (8000 series) is available in SO-8 (8-lead plastic micropackage). This last version is particularly suitable for professional and telecom applications wherever very high MTTF are required.

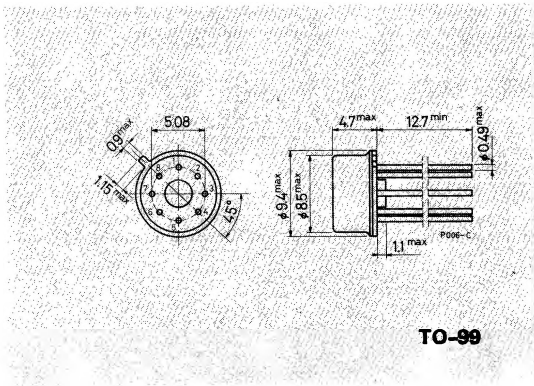
ABSOLUTE MAXIMUM RATINGS

		TO-99	μpackage
V_s	Supply voltage	± 18 V	
V_i(1)	Input voltage	± 12 V	
ΔV_i	Differential input voltage	± 30 V	
T_{op}	Operating temperature	-25 to 85 °C	
	Output short circuit duration (2)	indefinite	
P_{tot}	Power dissipation at T_{amb} = 70°C	520 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C

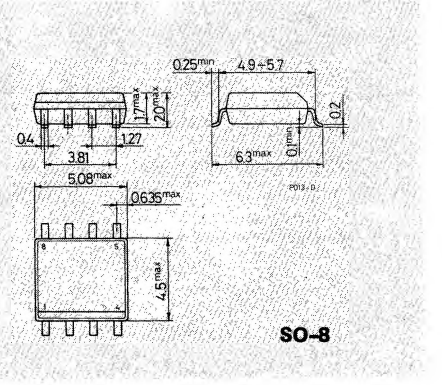
(1) For supply voltages less than ± 12V, input voltage is equal to supply voltage.
(2) The short circuit duration is limited by thermal dissipation.

MECHANICAL DATA

Dimensions in mm

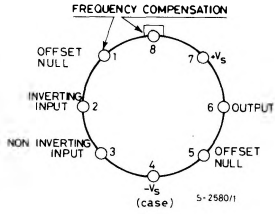


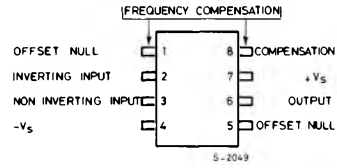
TO-99



SO-8

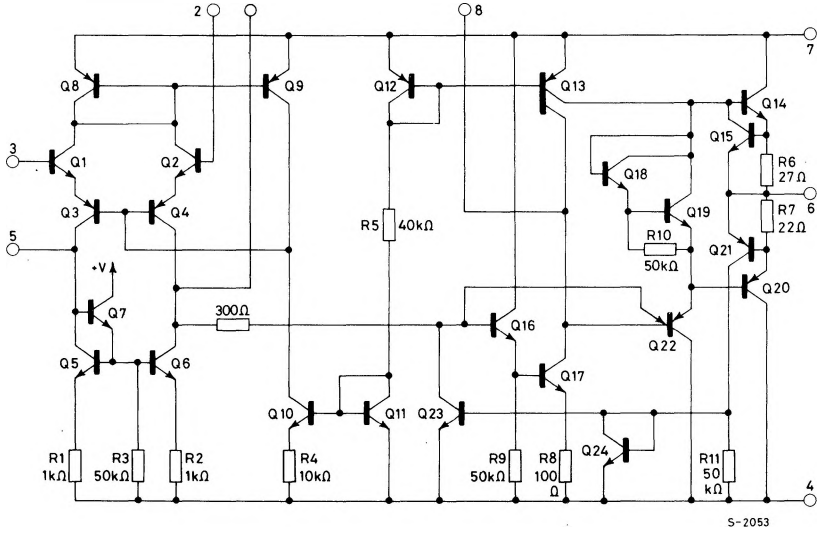
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-99	SO-8
LS 045	LS 045T	LS045M
LS 8045		LS 8045M

SCHEMATIC DIAGRAM



THERMAL DATA			TO-99	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	200* °C/W

* The thermal resistance is measured with the device mounted on a ceramic substrate (25x16x0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s= -20V, V_{bal}= -10V, T_{amb}= 25°C unless otherwise specified. For V_{bal} see fig. 7)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_{os}	Input offset voltage	R_g= 10 kΩ			± 1.5	± 10	mV
I_b	Input bias current				100	750	nA
R_i	Input resistance	Open loop			2		MΩ
R_o	Output resistance				75		Ω
G_V	Open loop voltage gain	R_L= 2 kΩ	f = 10 Hz	83	105		dB
d	Distortion	f = 1 kHz $Z_{L\,eq}$= 470Ω	G_V= 40 dB P_o= -5 dBm P_o= 8 dBm		 0.15 0.15	 0.3 0.3	 % %
P_{tot}	Quiescent power dissipation	P_o= 0			20	30	mW
P_o	Maximum output power	d = 1% G_V= 40 dB	Z_{Leq}= 470Ω	14	16		dBm
P_n	Noise power referred to input	R_g ⩽ 1.5 kΩ G_V= 40 dB	f = 1 kHz B = 100 Hz			-120.5	dBm
SVR	Supply voltage rejection referred to output	f = 1 kHz	G_V= 40 dB	30	36		dB

THE FOLLOWING SPECIFICATION APPLY FOR T_{amb} = -25 to 85°C

V_{os}	Input offset voltage	R_g= 10 kΩ			± 15	mV
I_b	Input bias current				1.5	μA
G_V	Open loop voltage gain	R_L= 2 kΩ	78			dB

Fig. 1 - Quiescent power dissipation vs. ambient temperature

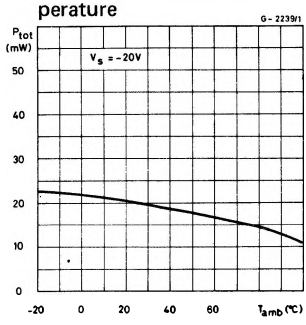


Fig. 2 - Quiescent power dissipation vs. supply voltage

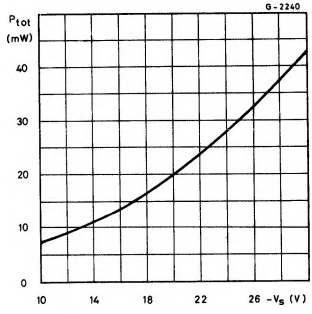


Fig. 3 - Voltage gain (open loop) vs. frequency

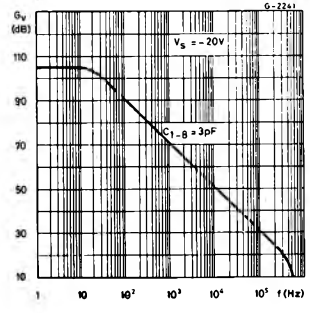


Fig. 4 - Maximum output power vs. load resistance

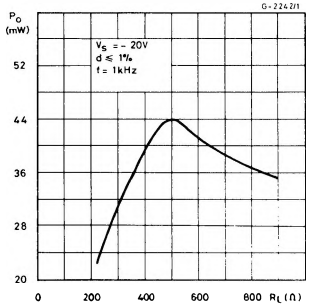


Fig. 5 - Distortion vs. output power

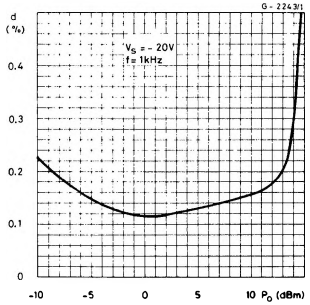
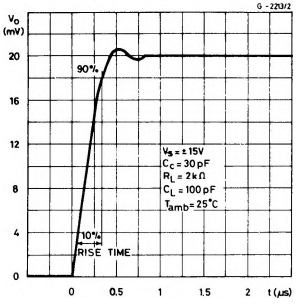


Fig. 6 - Transient response (unity gain)



APPLICATION INFORMATION

Fig. 7 - Channel amplifier circuit

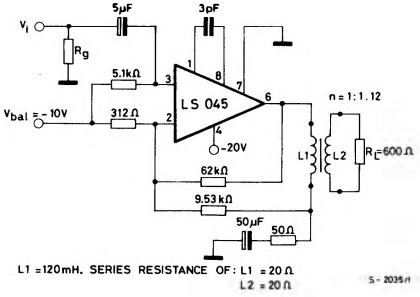


Fig. 8 - Return loss vs. frequency

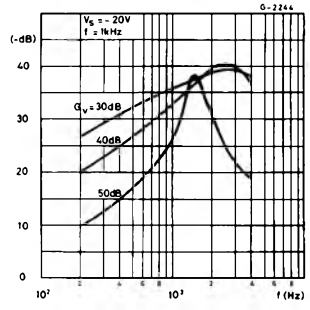


Fig. 9 - Return loss vs. voltage gain