LSI/CSI

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A3800

LS7166

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24-BIT MULTI-MODE COUNTER

FEATURES:

- Programmable modes are: Up/Down, Binary, BCD, 24 Hour Clock, Divide-by-N, X1 or X2 or X4 Quadrature and Single Cycle.
- DC to 20 MHz Count Frequency.
- 8-Bit I/O Bus for Microprocessor Communication and Control.
- 24-Bit comparator for pre-set count comparison.
- Readable status register.
- Input/Output TTL and CMOS compatible.
- 5 V operation.
- 20-Pin Plastic DIP, 20-Pin SOIC

PIN ASSIGNMENT - TOP VIEW

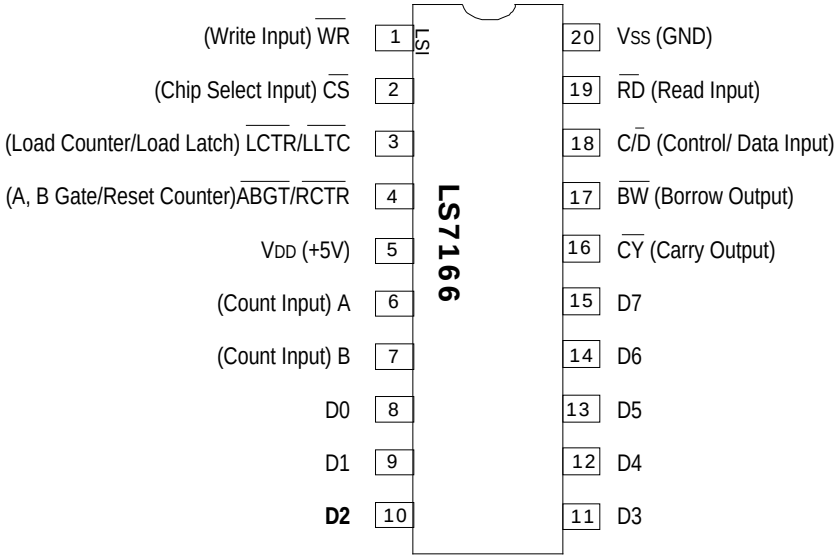


FIGURE 1

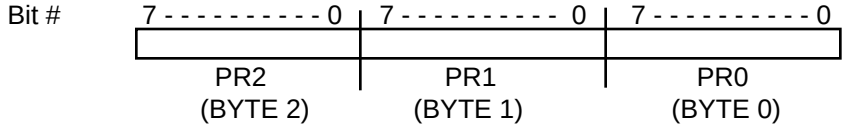
GENERAL DESCRIPTION:

The LS7166 is a monolithic, CMOS Silicon Gate, 24-bit counter that can be programmed to operate in several different modes. The operating mode is set up by writing control words into internal control registers (see Figure 8). There are three 6-bit and one 2-bit control registers for setting up the circuit functional characteristics. In addition to the control registers, there is a 5-bit output status register (OSR) that indicates the current counter status. The LS7166 communicates with external circuits through an 8-bit three state I/O bus. Control and data words are written into the LS7166 through the bus. In addition to the I/O bus, there are a number of discrete inputs and outputs to facilitate instantaneous hardware based control functions and instantaneous status indication.

REGISTER DESCRIPTION:

Internal hardware registers are accessible through the I/O bus (D0 - D7) for READ or WRITE when $\overline{CS}$ = 0. The C/$\overline{D}$ input selects between the control registers (C/D = 1) and the data registers (C/$\overline{D}$ = 0) during a READ or WRITE operation. (See Table 1)

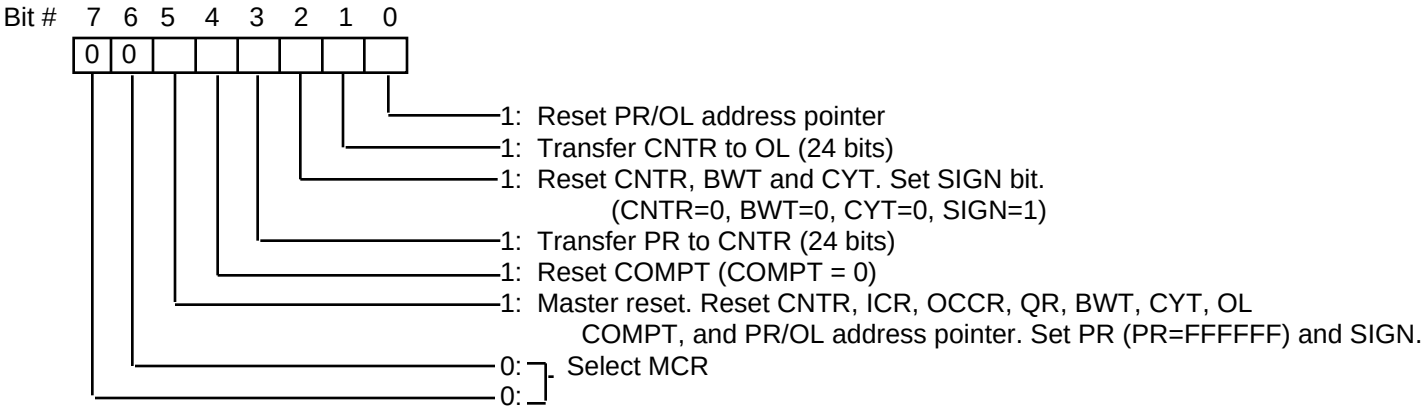
PR (Preset register). The PR is the input port for the CNTR. The CNTR is loaded with a 24 bit data via the PR. The data is first written into the PR in 3 WRITE cycle sequence of Byte 0 (PR0), Byte 1 (PR1) and Byte 2 (PR2).
The address pointer for PR0/PR1/PR2 is automatically incremented with each write cycle.
Accessed by**:** WRITE when C/$\overline{D}$ = 0, $\overline{CS}$ = 0.



Standard Sequence for Loading PR and Reading CNTR**:**

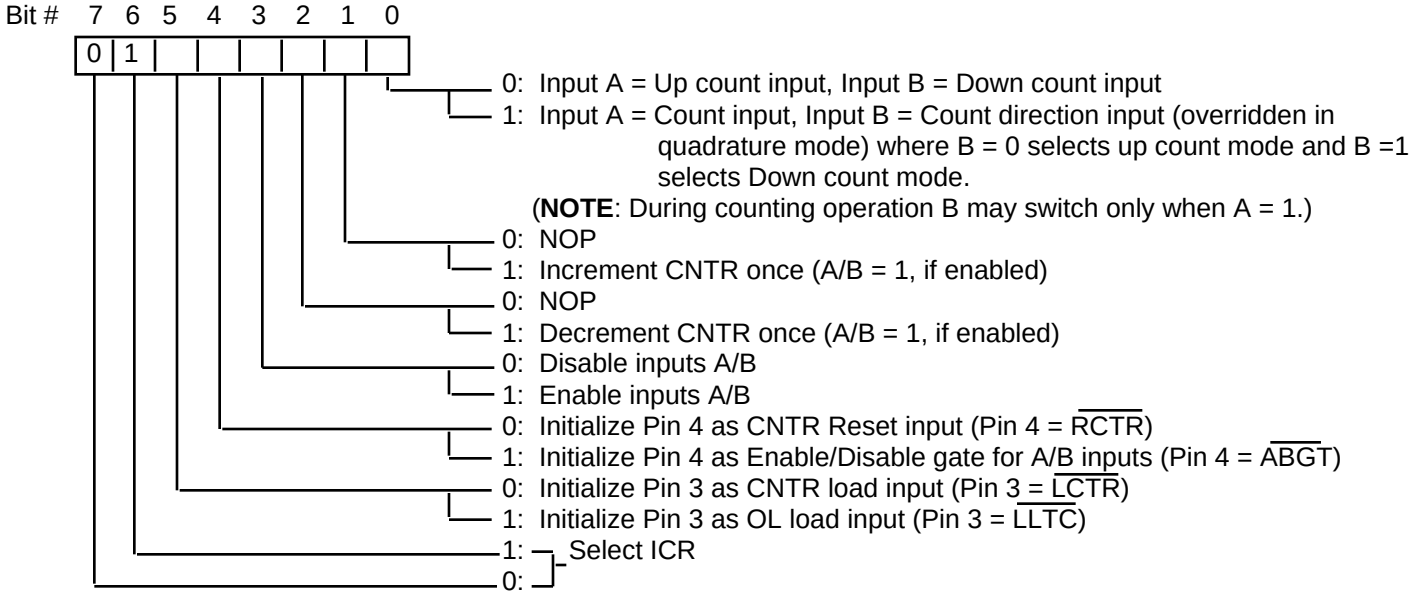
```
1 ⟶ MCR      ; Reset PR address pointer
WRITE PR     ; Load Byte 0 and into PR0 increment address
WRITE PR     ; Load Byte 1 and into PR1 increment address
WRITE PR     ; Load Byte 2 and into PR3 increment address
8 ⟶ MCR      ; Transfer PR to CNTR
```

MCR (Master Control Register). Performs register reset and load operations. Writing a "non-zero" word to MCR does not require a follow-up write of an "all-zero" word to terminate a designated operation.
Accessed by**:** WRITE when C/$\overline{D}$ = 1, $\overline{CS}$ = 0.



NOTE: Control functions may be combined.

ICR (Input Control Register). Initializes counter input operating modes.
Accessed by**:** WRITE when C/$\overline{D}$ = 1, $\overline{CS}$ = 0.



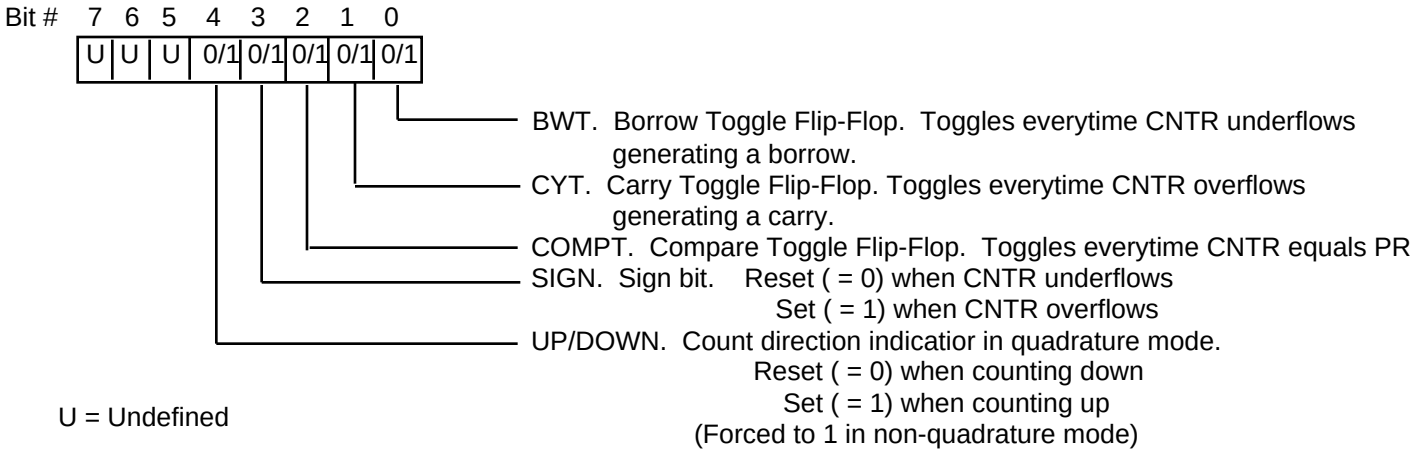
NOTE: Control functions may be combined.

TABLE 1 - Register Addressing Modes

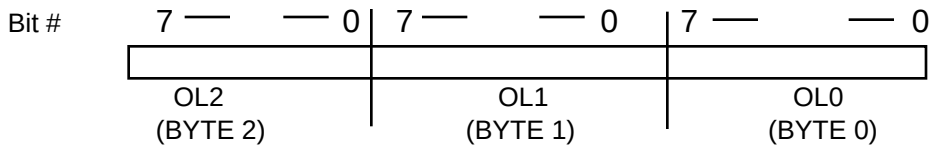
D7	D6	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	COMMENT
X	X	X	X	X	1	Disable Chip for READ/WRITE
0	0	1	1	⊓⊔⊓	0	Write to Master Control Register (MCR)
0	1	1	1	⊓⊔⊓	0	Write to input control register (ICR)
1	0	1	1	⊓⊔⊓	0	Write to output/counter control register (OCCR)
1	1	1	1	⊓⊔⊓	0	Write to quadrature register (QR)
X	X	0	1	⊓⊔⊓	0	Write to preset register (PR) and increment register address counter.
X	X	0	⊓⊔⊓	1	0	Read output latch (OL) and increment register address counter
X	X	1	⊓⊔⊓	1	0	Read output status register (OSR).

X = Don't Care

OSR (Output Status Register). Indicates CNTR status: Accessed by**:** READ when C/$\overline{D}$ = 1, $\overline{CS}$ = 0.



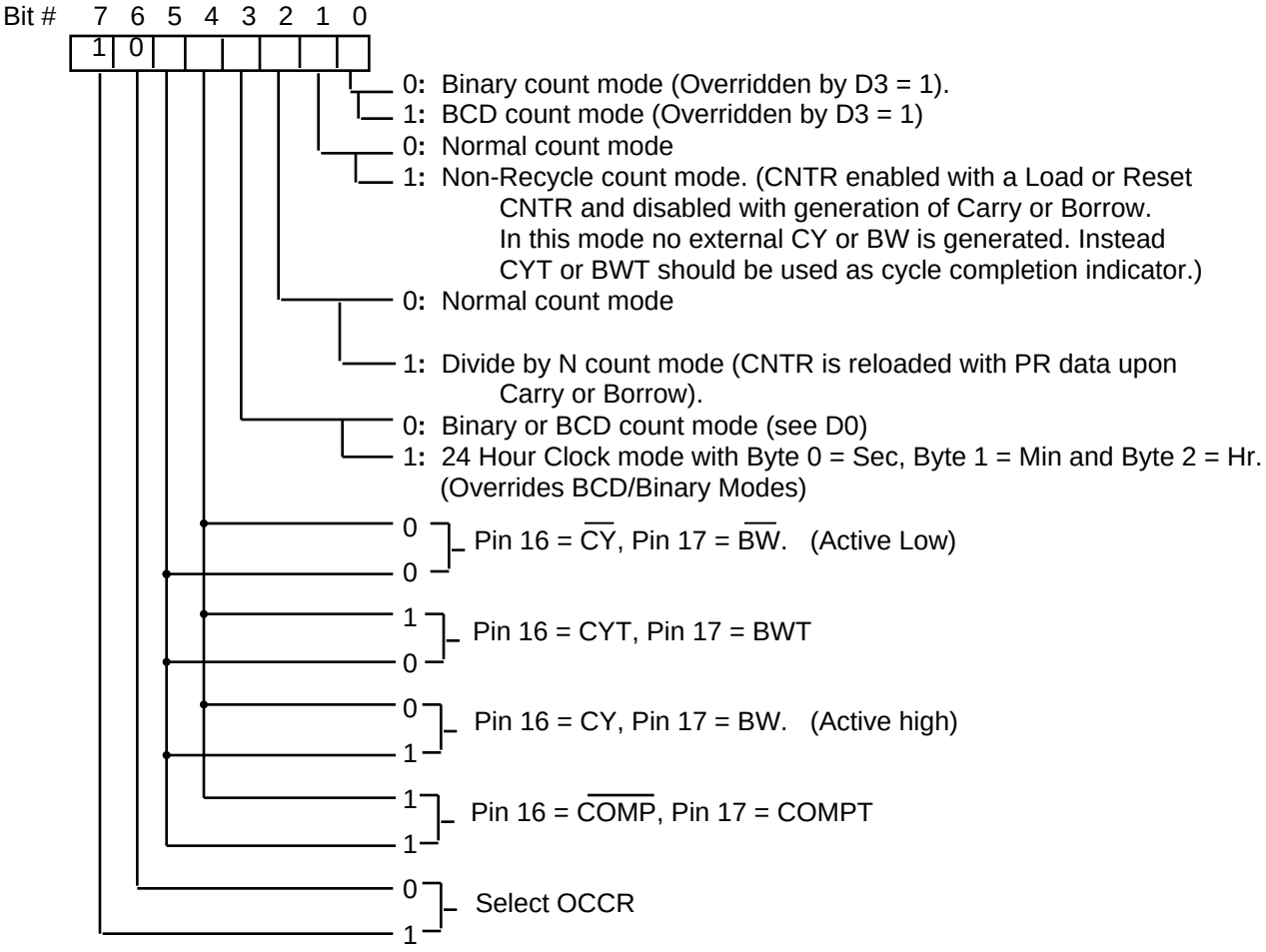
OL(Output latch). The OL is the output port for the CNTR. The 24 bit CNTR Value at any instant can be accessed by performing a CNTR to OL transfer and then reading the OL in 3 READ cycle sequence of Byte 0 (OL0), Byte 1 (OL1) and Byte 2 (OL2). The address pointer for OL0/OL1/OL2 is automatically incremented with each READ cycle. Accessed by**:** READ when C/$\overline{D}$ = 0, $\overline{CS}$ = 0.



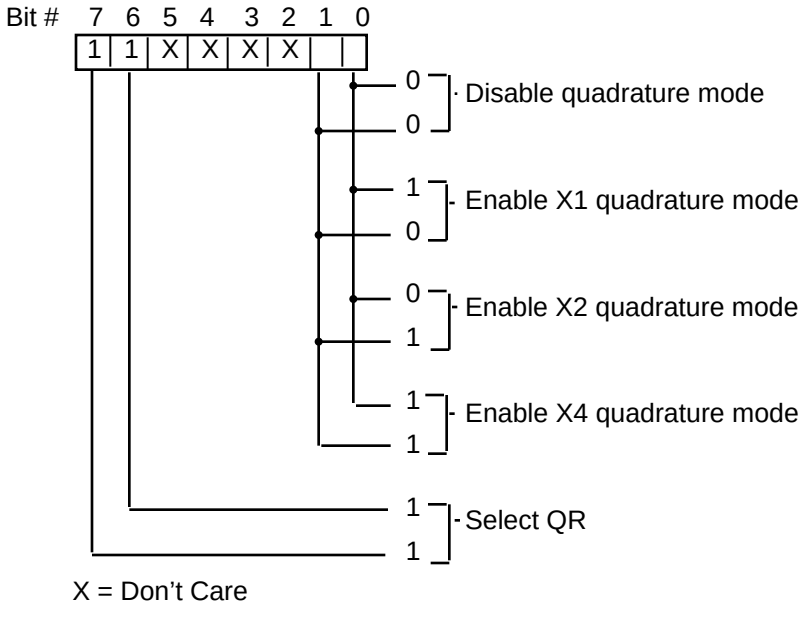
Standard Sequence for Loading and Reading OL**:**

```
3 ⟶ MCR     ; Reset OL address pointer and Transfer CNTR to OL
READ OL     ; Read Byte 0 and increment address
READ OL     ; Read Byte 1 and increment address
READ OL     ; Read Byte 2 and increment address
```

OCCR (Output Control Register) Initializes CNTR and output operating modes.
Accessed by **:** WRITE when C/$\overline{D}$ = 1, $\overline{CS}$ = 0.



QR (Quadrature Register). Selects quadrature count mode (See Fig. 7)
Accessed by**:** WRITE when C/$\overline{D}$ = 1, $\overline{CS}$ = 0.



X = Don't Care

I/O DESCRIPTION:
(See **REGISTER DESCRIPTION** for I/O Prgramming.)

Data-Bus (D0-D7) (Pin 8-Pin 15). The 8-line data bus is a three-state I/O bus for interfacing with the system bus.

$\overline{CS}$ (Chip Select Input) (Pin 2). A logical 0 at this input enables the chip for Read and Write.

$\overline{RD}$ (Read Input) (Pin 19). A logical 0 at this input enables the OSR and the OL to be read on the data bus.

$\overline{WR}$ (Write Input) (Pin 1). A logical 0 at this input enables the data bus to be written into the control and data registers.

C/$\overline{D}$ (Control/Data Input) (Pin 18). A logical 1 at this input enables a control word to be written into one of the four control registers or the OSR to be read on the I/O bus. A logical 0 enables a data word to be written into the PR, or the OL to be read on the I/O bus.

A (Pin 6). Input A is a programmable count input capable of functioning in three different modes, such as up count input, down count input and quadrature input.

B (Pin 7). Input B is also a programmable count input that can be programmed to function either as down count input, or count direction control gate for input A, or quadrature input. When B is programmed as count direction control gate, B = 0 enables A as the Up Count input and B = 1 enables A as the Down Count input. When programmed as the direction input, B can switch state only when A is high.

$\overline{ABGT}$/$\overline{RCTR}$ (Pin4). This input can be programmed to function as either inputs A and B enable gate or as external counter reset input. A logical 0 is the active level on this input.

In non-quadrature mode, if Pin 4 is programmed as A and B enable gate input, it may switch state only when A is high (if A is clock and B is direction) or when both A and B are high (if A and B are clocks). In quadrature mode, if Pin 4 is programmed as A and B enable gate, it may switch state only when either A or B switches.

$\overline{LCTR}$/$\overline{LLTC}$ (Pin 3). This input can be programmed to function as the external load command input for either the CNTR or the OL. When programmed as counter load input, the counter is loaded with the data contained in the PR. When programmed as the OL load input, the OL is loaded with data contained in the CNTR. A logical 0 is the active level on this input.

$\overline{CY}$ (Pin16). This output can be programmed to serve as one of the following:
A. $\overline{CY}$. Complemented Carry out (active 0).
B. CY. True Carry out (active 1).
C. CYT. Carry Toggle flip-flop out.
D. $\overline{COMP}$. Comparator out (active 0)

$\overline{BW}$ (Pin17). This output can be programmed to serve as one of the following:
A. $\overline{BW}$. Complemented Borrow out (active 0).
B. BW. True Borrow out (active 1).
C. BWT. Borrow Toggle flip-flop out.
D. COMPT. Comparator Toggle output.

V_{DD} (Pin 5). Supply voltage positive terminal.

Vss (Pin 20). Supply voltage negative terminal.

Absolute Maximum Ratings:

Parameter	Symbol	Values	Unit
Voltage at any input	V_{IN}	V_{SS}-.3 to V_{DD}+.3	V
Operating Temperature	T_A	0 to +70	^oC
Storage Temperature	T_{STG}	-65 to +150	^oC
Supply Voltage	V_{DD}-V_{SS}	+7.0	V

DC Electrical Characteristics. (All voltages referenced to V_{SS}.
TA = 0˚ to 70˚C, V_{DD} = 4.5V to 5.5V, fc = 0, unless otherwise specified)

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Supply Voltage	V_{DD}	4.5	5.5	V	-
Supply Current	I_{DD}	-	350	µA	Outputs open
Input Low Voltage	VIL	0	0.8	V	-
Input High Voltage	VIH	2.0	V_{DD}	V	-
Output Low Voltage	VOL	-	0.4	V	4mA Sink
Output High Voltage	VOH	2.5	-	V	200µA Source
Input Current	-	-	15	nA	Leakage Current
Output Source Current	ISRC	200	-	µA	VOH = 2.5V
Output Sink Current	ISINK	4	-	mA	VOL = 0.4V
Data Bus Off-State Leakage Current	-	-	15	nA	-

TRANSIENT CHARACTERISTICS

(See Timing Diagrams in Fig. 2 thru Fig. 7, V_{DD} = 4.5V to 5.5V, T_A = 0° to 70°C, unless otherwise specified)

Parameter	Symbol	Min.Value	Max.Value	Unit
Clock A/B low	T_{CL}	20	No Limit	ns
Clock A/B high	T_{CH}	30	No Limit	ns
Clock A/B Frequency (See NOTE 1)	fc	0	20	MHz
Clock UP/DN Reversal Delay	T_{UDD}	100	-	ns
LCTR Positive edge to the next A/B positive or negative edge delay	T_{LC}	100	-	ns
Clock A/B to CY/BW/COMP low propagation delay	T_{CBL}	-	65	ns
Clock A/B t CY/BW/COMP high propagation delay	T_{CBH}	-	85	ns
LCTR and LLTC pulse width	T_{LCW}	60	-	ns
Clock A/B to CYT, BWT and COMPT high propagation delay	T_{TFH}	-	100	ns
Clock A/B to CYT, BWT and COMPT low progagation delay	T_{TFL}	-	100	ns
WR pulse width	T_{WW}	60	-	ns
RD to data out delay (C_L=20pF)	T_R	-	110	ns
CS, RD Terminate to Data-Bus Tri-State	T_{RT}	-	30	ns
Data-Bus set-up time for WR	T_{DS}	15	-	ns
Data-Bus hold time for WR	T_{DH}	30	-	ns
C/D,CS set-up time for RD	T_{CRS}	0	-	ns
C/D, CS hold time for RD	T_{CRH}	0	-	ns
C/D set-up time for WR	T_{CWS}	15	-	ns
C/D hold time for WR	T_{CWH}	30	-	ns
CS set-up time for WR	T_{SWS}	15	-	ns
CS holdtime for WR	T_{SWH}	0	-	ns
Quadrature Mode:				
Clock A/B Validation delay (See NOTE 2)	T_{CQV}	-	160	ns
A and B phase delay	T_{PH}	208	-	ns
Clock A/B frequency	f_{CQ}	-	1.2	MHz
CY,BW,COMP pulse width	T_{CBW}	75	180	ns

NOTE 1: A) In Divide-by-N mode, the maximum clock frequency is 10 MHz.
B) The maximum frequency for valid CY, BW, CYT, BWT, COMP, COMPT is 10 MHz.

NOTE 2: In quadrature mode A/B inputs are filtered and required to be stable for at least T_{CQV} length to be valid.

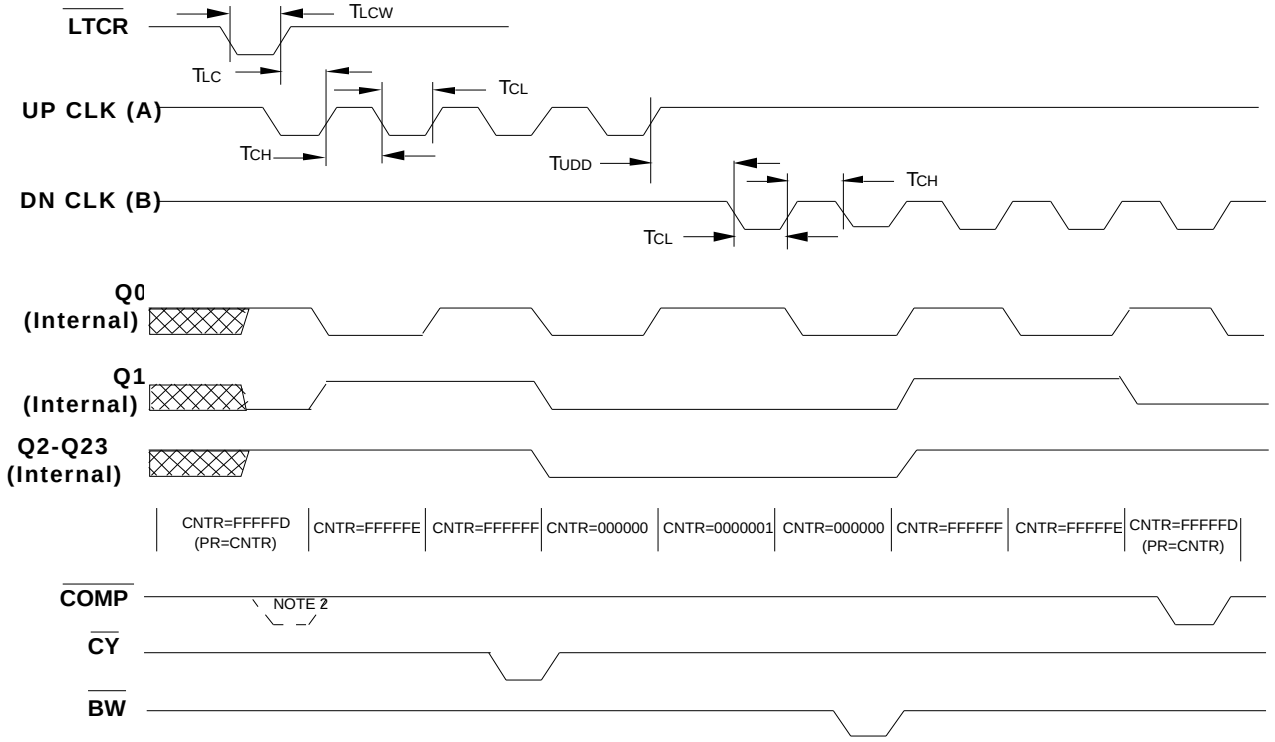


FIGURE 2 . LOAD COUNTER, UP CLOCK, DOWN CLOCK, COMPARE OUT, CARRY, BORROW

NOTE 1: The counter in this example is assumed to be operating in the binary mode.

NOTE 2: No COMP output is generated here, although PR=CNTR. COMP output is disabled with a counter load command and enabled with the rising edge of the next clock, thus eliminating invalid COMP outputs whenever the CNTR is loaded from the PR.

NOTE 3: When UP Clock is active, the DN Clock should be held high, and vice versa

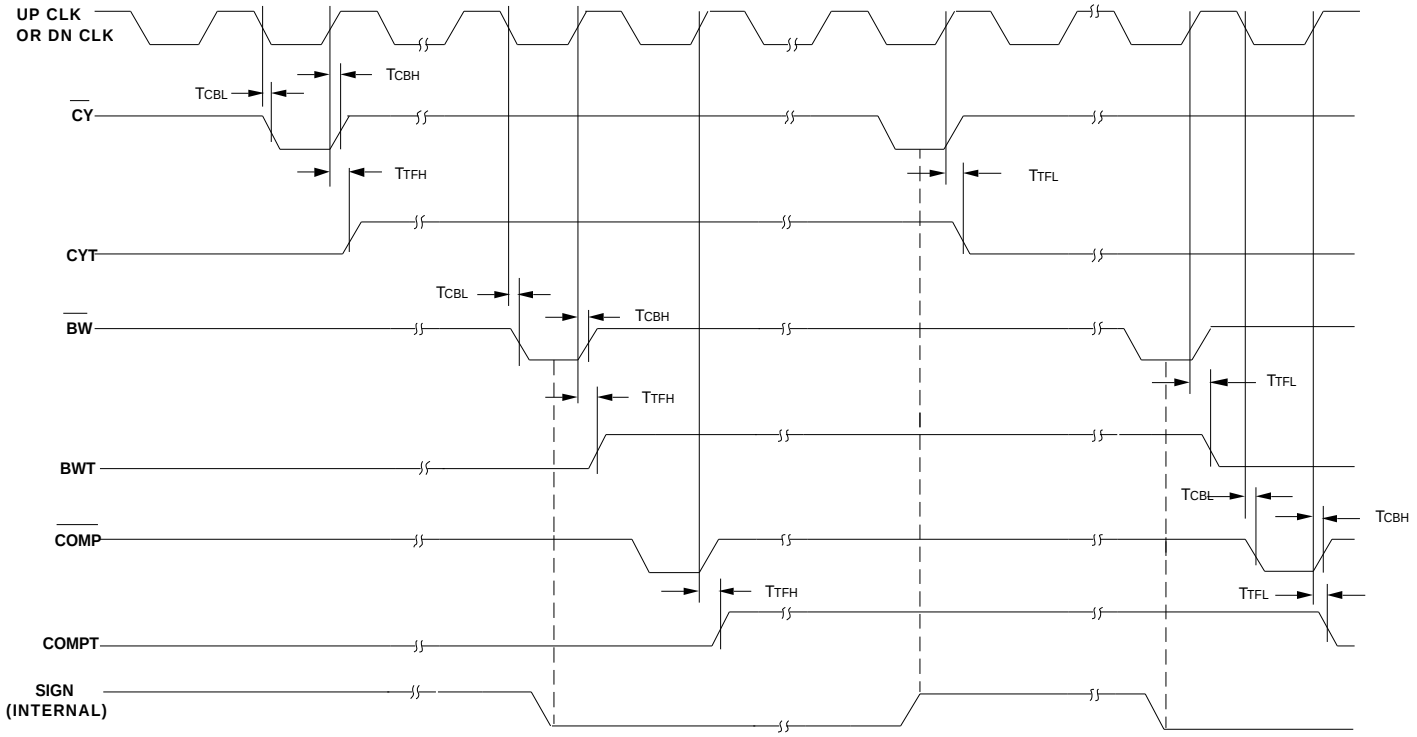


FIGURE 3. CLOCK TO CY/BW OUTPUT PROPAGATION DELAYS

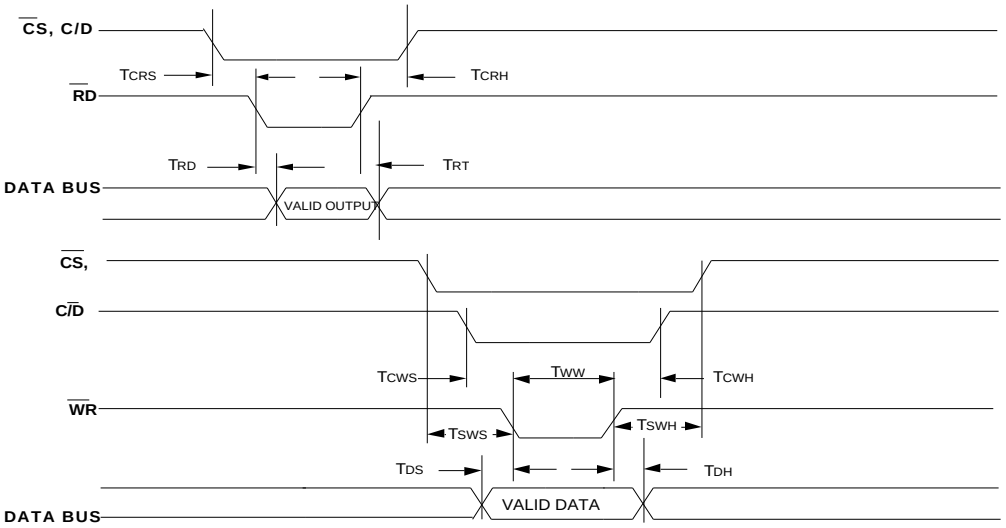
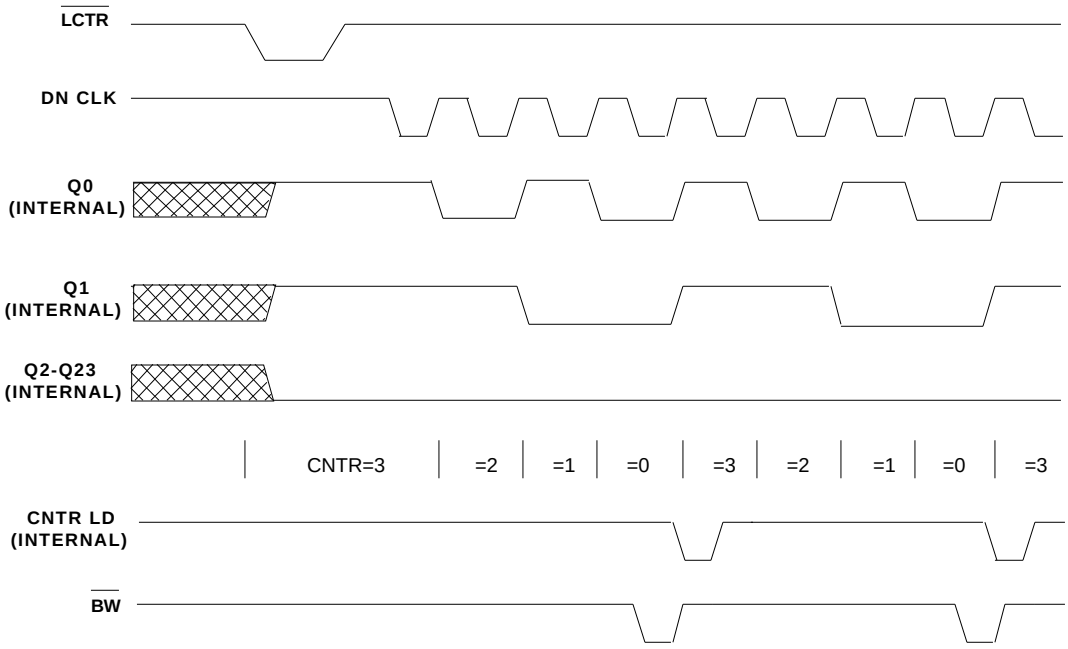


FIGURE 4. READ/WRITE CYCLES



NOTE: EXAMPLE OF DIVIDE BY 4 IN DOWN COUNT MODE

FIGURE 5. DIVIDE BY N MODE

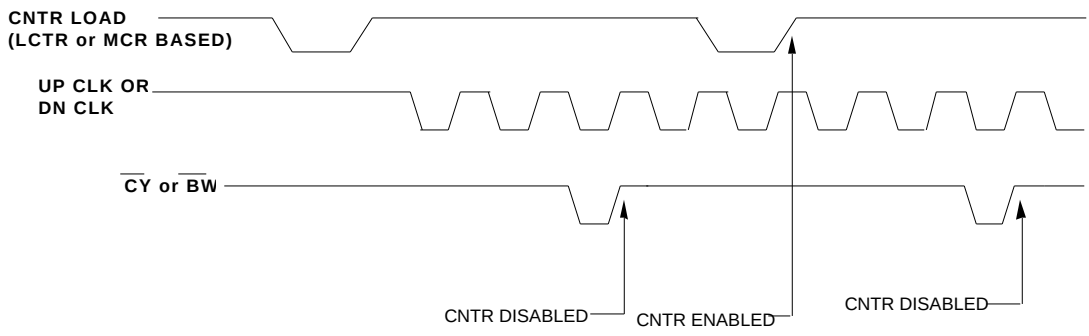


FIGURE 6 . CYCLE ONCE MODE

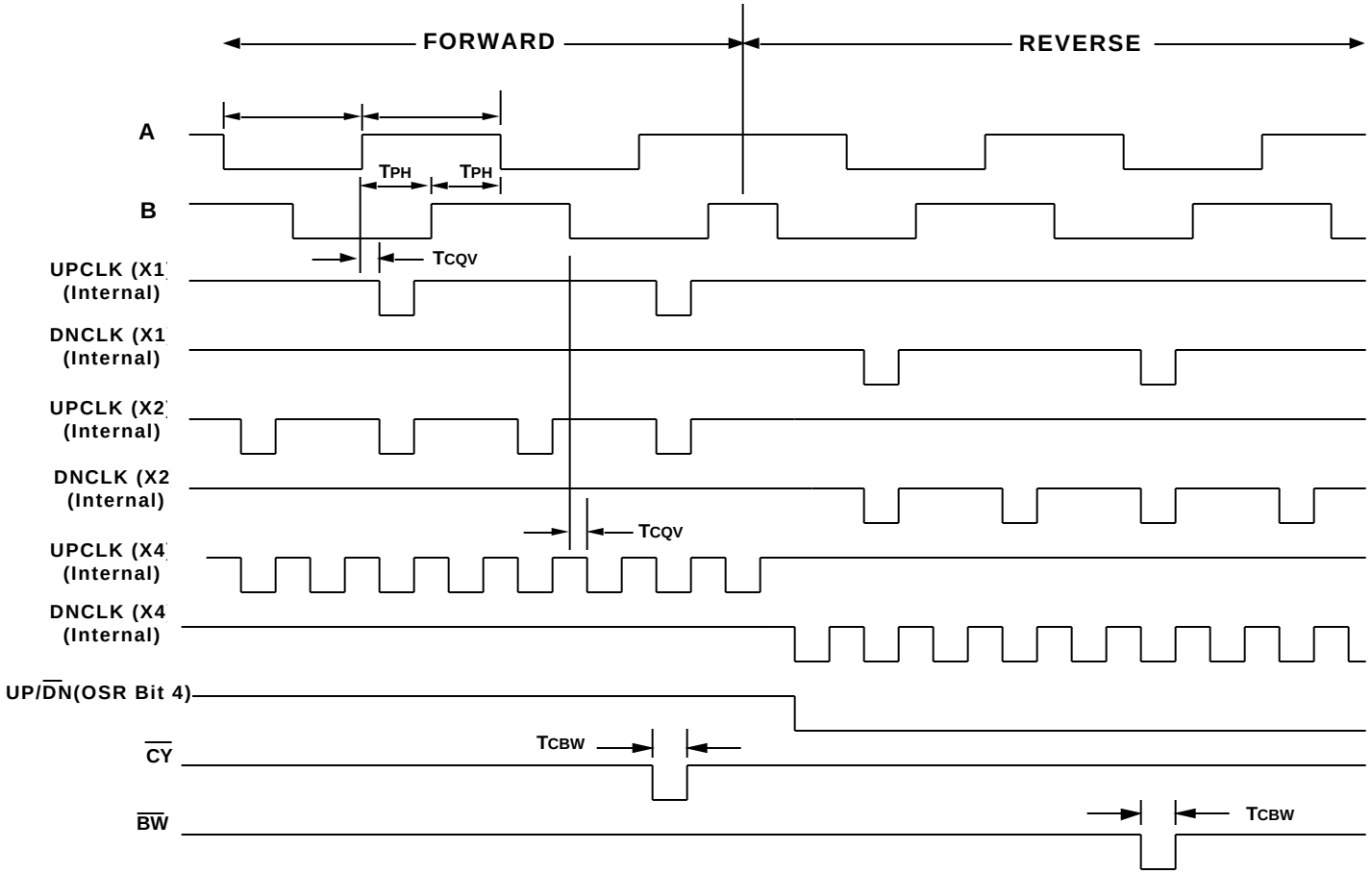


FIGURE 7.

QUADRATURE MODE INTERNAL CLOCKS

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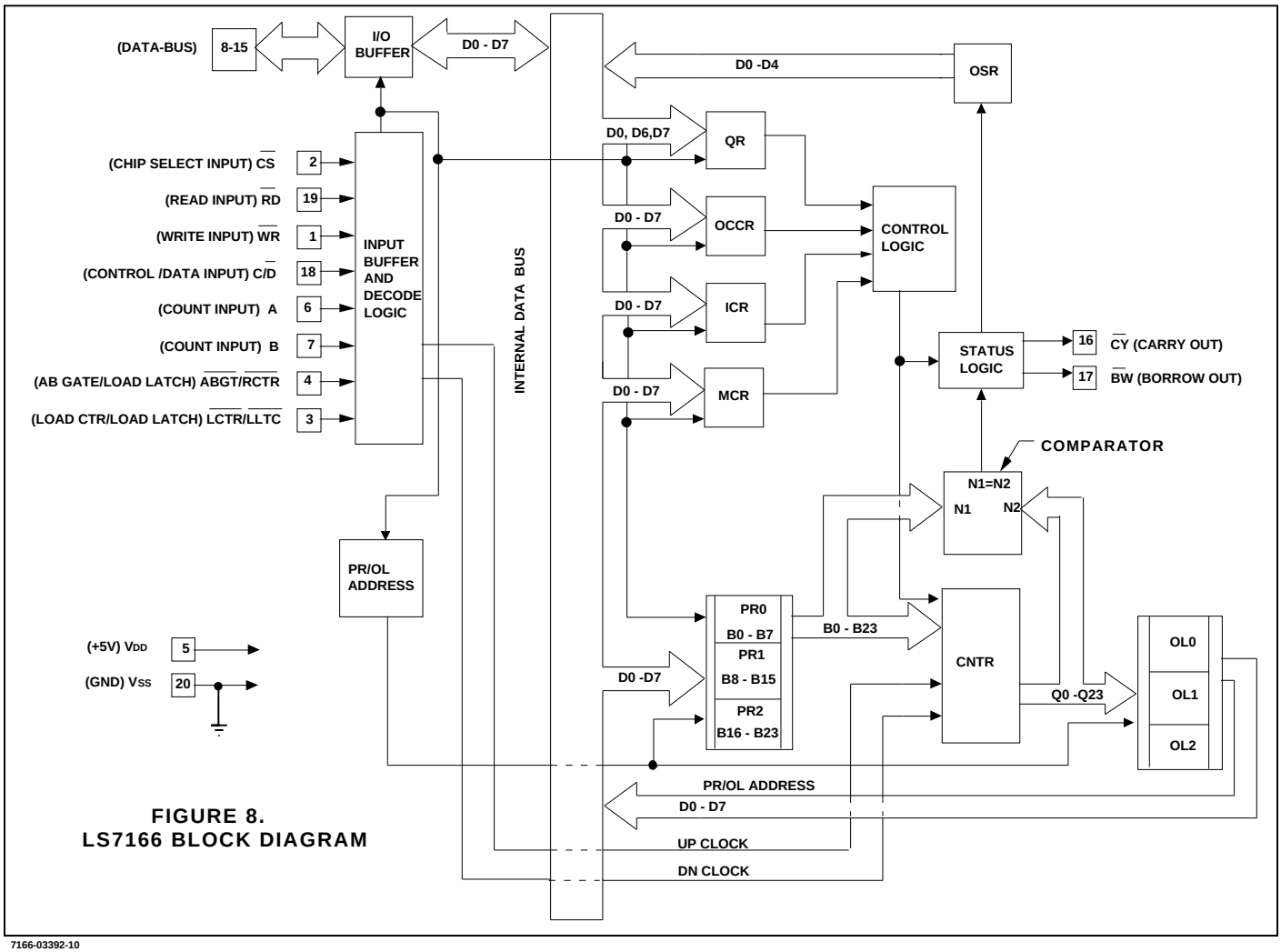

FIGURE 8.
LS7166 BLOCK DIAGRAM

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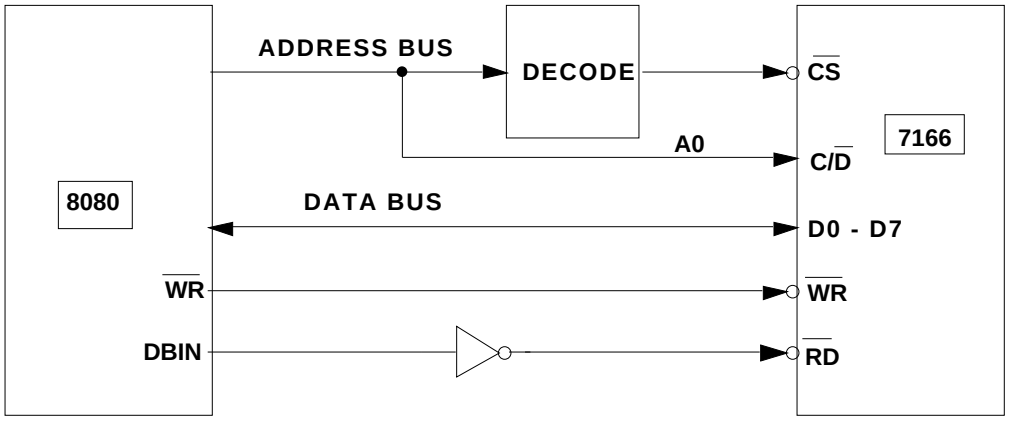
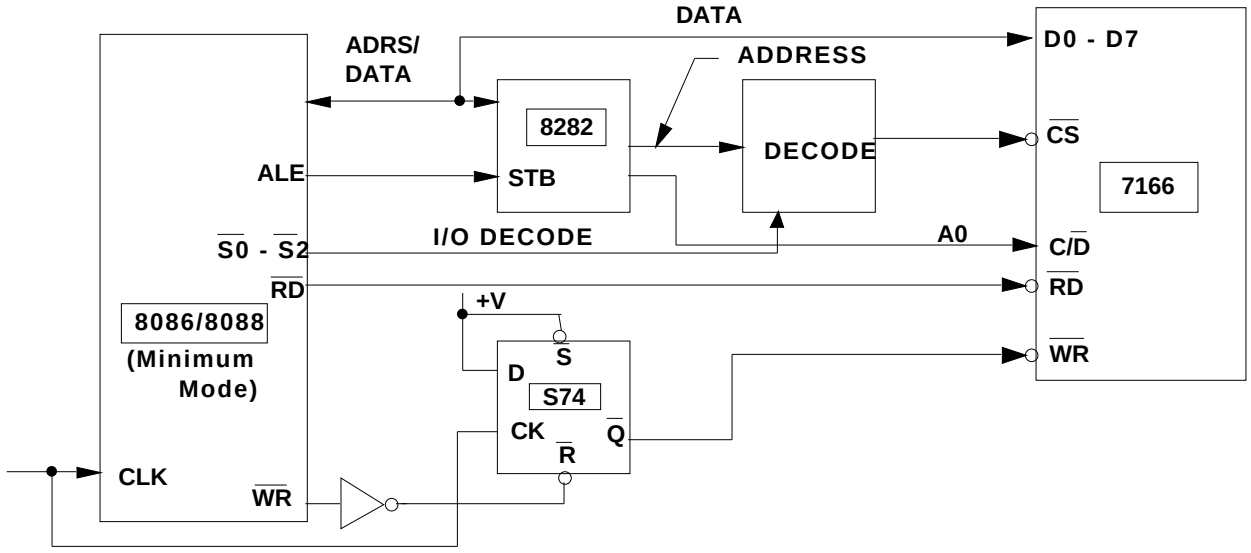
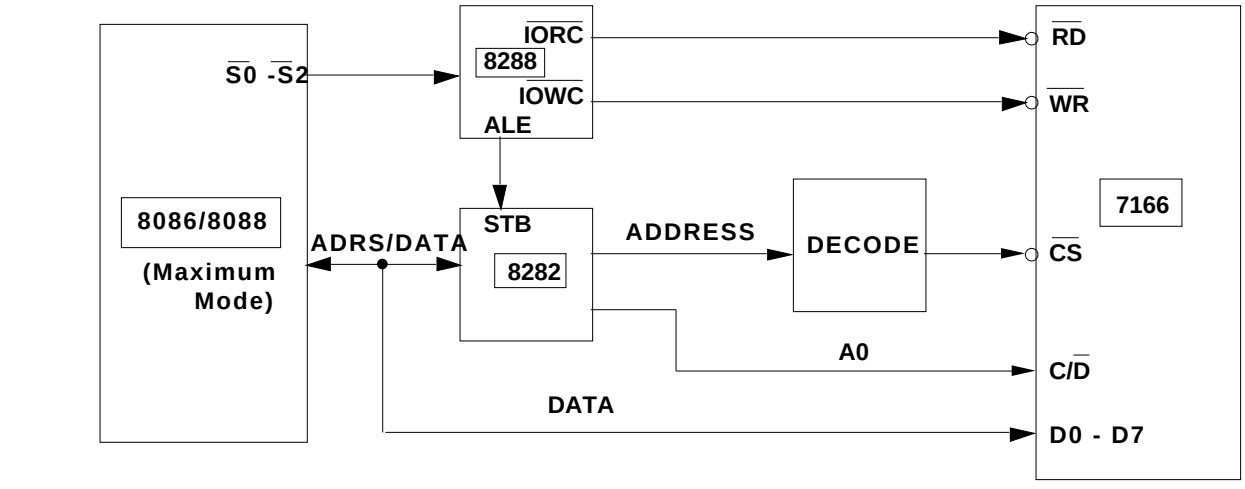
LS7166 INTERFACE EXAMPLES







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