Ordering number : ENN6074

Bi-CMOS IC

LV2200M

Cordless Telephone System IC

Overview

The LV2200M is a cordless telephone system IC that integrates a narrow-band FM IF system that includes an adjustment-free FM detection circuit, a dual-PLL frequency synthesizer, and audio signal-processing functions (compander) on a single chip. This IC is appropriate for compact design end products.

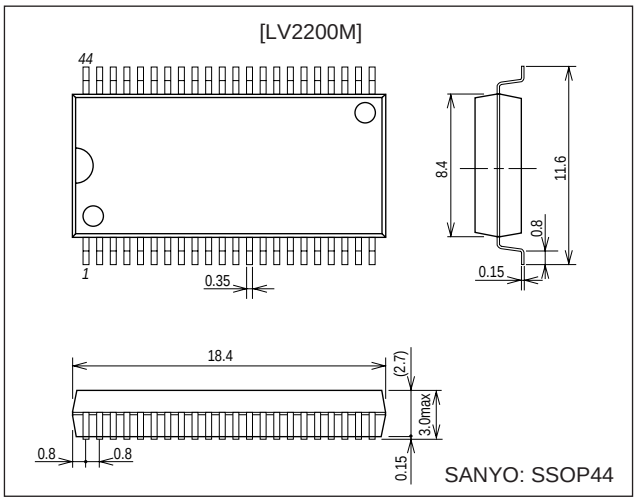
Functions

- IF system block
  - — First mixer, first local oscillator, second mixer, second local oscillator
  - — IF amplifier, limiter, RSSI
  - — FM detector
  - — Noise detection circuit (noise detection, Schmitt input, and noise filter operational amplifier)
- PLL system block (Supports all reception areas worldwide, except Japan.)
  - — Two built-in PLL systems, one for reception and one for transmission
  - — Programmable divider for the local oscillator
  - — Programmable divider for the reference frequency
  - — Built-in lock detection circuit (reception PLL)
  - — Transmitter and receiver PLL charge pump output current control circuits (PLL loop gain and time constant switching)
- Audio signal-processing block
  - — Compressor and expander
  - — Transmission audio signal limiter circuit (IDC)
  - — Splatter filter (SCF)
  - — Microphone amplifier
  - — Transmission and reception audio signal mute
  - — Reception system audio signal output level switching (low/high)
- Other functions
  - — Data input using serial data transmission (Controls all functions, including PLL circuits and muting.)
  - — Reception data input system filter (SCF)
  - — Reception data waveform shaper circuit (with hysteresis characteristics)
  - — Reception VCO regulator
  - — PLL regulator
  - — Battery check function
  - — Two standby modes

Package Dimensions

unit: mm

SSOP44



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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
Allowable power dissipation	Pd max	Ta ≤ 75°C	300	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		3	V
Operating supply voltage	V_{CC}op		2.4 to 5.5	V

Allowable Operating Ranges at Ta = –20 to 75°C, V_{CC} = 2.4 to 5.5 V

PLL block

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input voltage	V_{IH}	CL, DI, CE	$V_{CC} \times 0.7$		5.5	V
Low-level input voltage	V_{IL}	CL DI, CE	0		0.6	V
Output voltage	V_O	LD	0		5.5	V
Input frequency	f_{IN}	PI (TX)	1.0		60	MHz
Input amplitude	V_{IN}	PI (TX), f_{IN} = 10 M to 60 MHz	–12		10	dBm

Note : 50 Ω terminate (0 dBm = 0.224 mVrms)

Electrical Characteristics at Ta = 25°C, V_{CC} = 3 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current Drain]						
Quiescent current	I_{CCOP}	No signal input, all circuits active		17.3	24	mA
Standby current	Isb-1	No signal input, only latches active		0.01	10	µA
	Isb-2	No signal input, reception PLL and oscillators active		6.5	9.5	mA
	Isb-3	No signal input, RF system, reception PLL, and DTSH active		12.3	17.3	mA
[IF Block] fc = 49.830 MHz, fm = 1 kHz, fdev = ±3.0 kHz, AMmod = 30%						
First mixer conversion gain	$V_{CG}1$			20		dB
Second mixer conversion gain	$V_{CG}2$			22		dB
Mixer third intercept point	I_P3	First mixer		94		dBµ
Demodulator output	V_O	V_{IN} = 80 dBµEMF	138	175	222	mVrms
Total harmonic distortion	THD	V_{IN} = 80 dBµEMF		1.5	3	%
Signal-to-noise ratio	S/N	V_{IN} = 80 dBµEMF	43	48		dB
AM suppression ratio	AMR	V_{IN} = 80 dBµEMF	35	43		dB
RSSI output	$V_{REFI}1$	V_{IN} = 0 dBµEMF	0.1	0.3	0.55	V
	$V_{REFI}2$	V_{IN} = 20 dBµEMF	0.6	0.9	1.3	V
	$V_{REFI}3$	V_{IN} = 80 dBµEMF	1.6	2.0	2.4	V
Noise detector output	$V_{ND}1$	f_{IN} = 40 kHz, V_{IN} = –20 dBV	0.85	1.1	1.35	V
	$V_{ND}2$	f_{IN} = 40 kHz, V_{IN} = –10 dBV	1.4	1.7	2.0	V
Noise detection	$V_{NTH}1$	Schmitt circuit on		0.85		V
	$V_{NTH}2$	Schmitt circuit off		0.75		V
Schmitt output	$V_{SH}1$	V41 = 1.4 V			0.2	
	$V_{SH}2$	V41 = 0.2 V	2.8			V
[PLL Block]						
High-level output voltage	V_{OL}	LD, I_O = 2 mA			0.5	V
Output off leakage current	$I_{OFF}1$	LD, V_O = 3 V			3	µA
	$I_{OFF}2$	PDR PDT, V_O = 1.5 V			0.1	µA
High-level input current	I_H1	CL, DI, CE, V_I = 3 V			5	µA
Low-level input current	I_L1	CL, DI, CE, V_I = 0 V			5	µA

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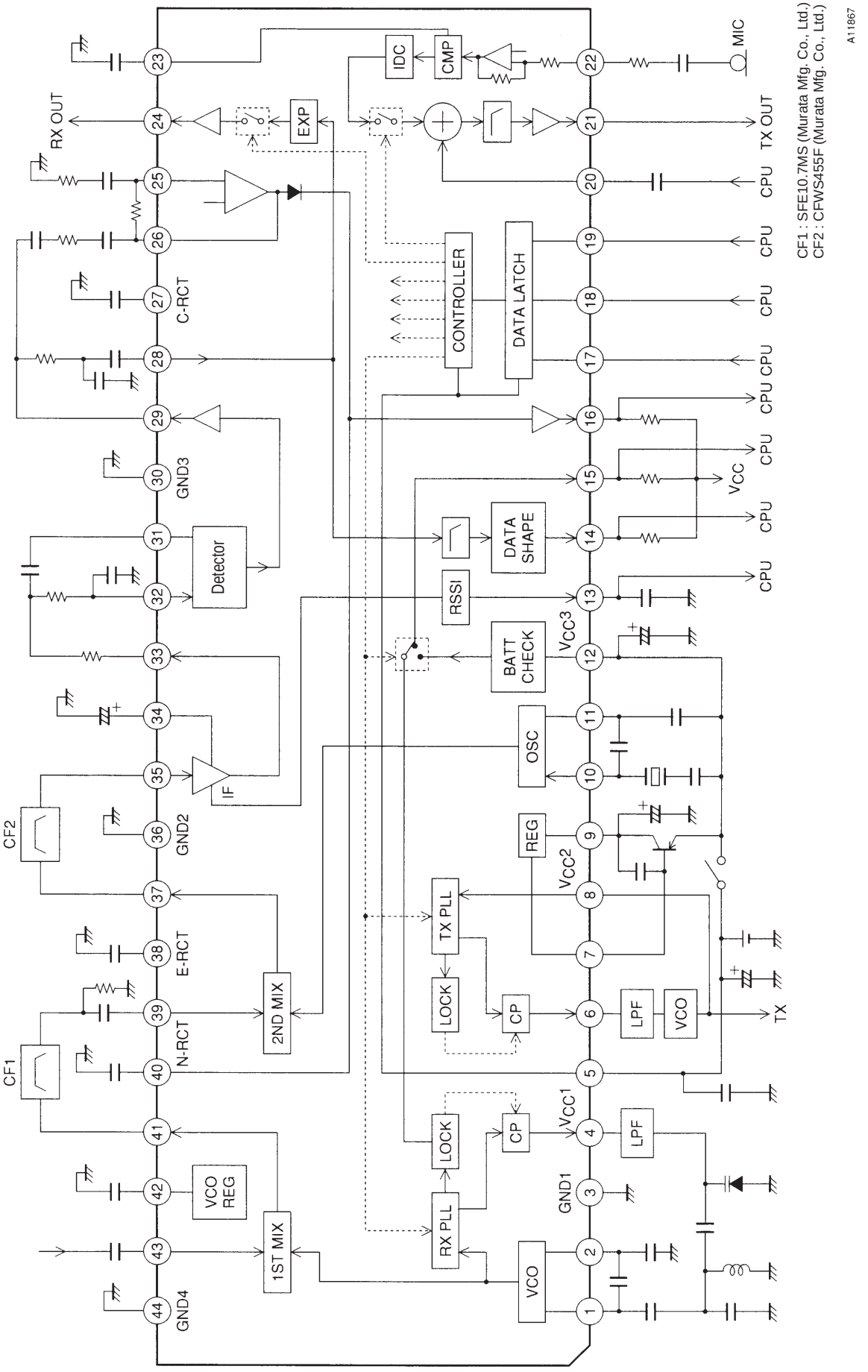
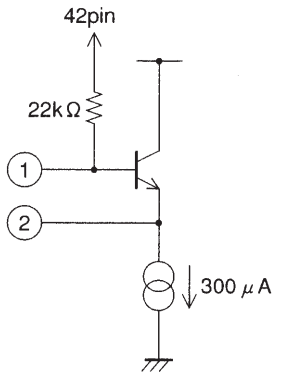
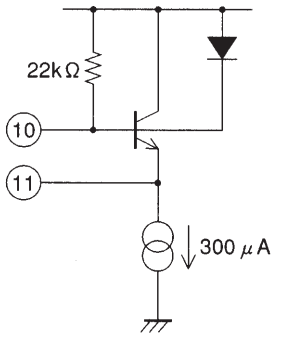
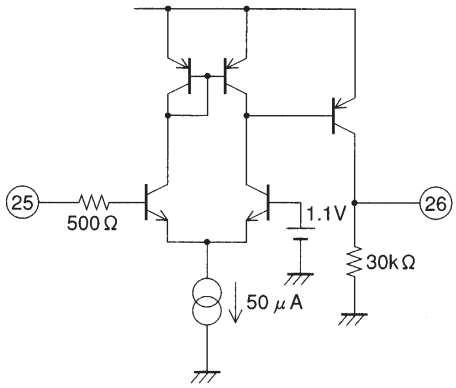
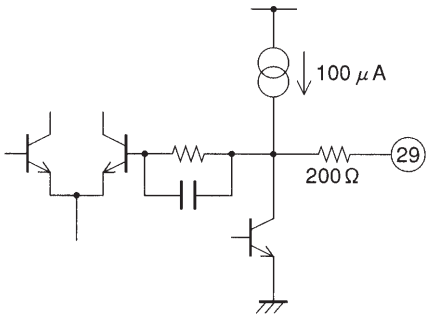
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Audio Signal-Processing Block]						
<Transmission System Audio Signal Processing> $V_{IN\ REFC}$ = –40 dBV = 0 dB, f_{IN} = 1 kHz, Pre-Amp Gain = 20 dB, R_L = 15 kΩ						
Output level	$V_O$tx	$V_{IN} = V_{IN\ REFC}$ = 0 dB	–15.1	–13.1	–11.1	dBV
Gain error	Gec	V_{IN} = –40 dB	–2	–0.6	+1.0	dB
Total harmonic distortion	THDtx	V_{IN} = 0 dB		0.45	1.0	%
Output noise voltage	VNtx	Rg = 620Ω, f = 20 Hz to 20 kHz		2.7	5.4	mVrms
Limiting voltage	V_{LT}	V_{IN} = +20 dB, 1 kHz-BPF	1.16	1.4	1.64	Vp-p
Maximum preamplifier voltage gain	$V_G$max		30			dB
Splatter filter attenuation	Gfil	f_{IN} = 5 kHz	–13.5	–11.5	–9.5	dB
Muting attenuation	ATTtx	V_{IN} = 0 dB, 1 kHz-BPF		–76	–60	dBV
Crosstalk	CTtx	EXp-V_{IN} = –20 dBV, 1 kHz-BPF		–60	–50	dBV
[Reception System Audio Signal Processing] $V_{IN\ REFE}$ = –20 dBV = 0 dB, f_{IN} = 1 kHz, R_L = 15 kΩ						
Output level	$V_O$rx	$V_{IN} = V_{IN\ REFE}$ = 0 dB	–22.2	–19.7	–17.2	dBV
Audio switching level difference	VLch	V_{IN} = 0 dB	6.5	7.4	8.4	dB
Gain error	Gee	V_{IN} = –30 dB	–1.5	+0.3	+2.0	dB
Total harmonic distortion	THDrx	V_{IN} = 0 dB		0.3	1	%
Output noise voltage	$V_N$rx	Rg = 620Ω, f = 20 Hz to 20 kHz		27	55	µVrms
Muting attenuation	ATTrx	V_{IN} = 0 dB, 1 kHz-BPF		–92	–70	dBV
Crosstalk	CTrx	Cmp-V_{IN} = –20 dBV, 1 kHz-BPF		–92	–70	dBV
[Data Shaper] V_{IN} = –20 dBV, f_{IN} = 1 kHz, R_L = 100 kΩ (pin 14)						
Duty ratio	Duty		43	50	57	%
Hysteresis	Hys			50		mVp-p
High-level output voltage	V_{DT}H		V_{CC} – 0.2	V_{CC}		V
Low-level output voltage	V_{DT}L			0.03	0.3	V
[Battery Check Function] R_L = 100 kΩ (pin 15)						
Supply voltage detection level	L_{BT}1	BT1 = 0, BT0 = 1	3.08	3.3	3.52	V
	L_{BT}2	BT1 = 1, BT0 = 0	2.83	3.05	3.27	V
	L_{BT}3	BT1= 1, BT0 = 1	2.63	2.85	3.03	V
High-level output voltage	V_{BC}H	$V_{CC} \le L_{BT}$	V_{CC} – 0.2	V_{CC}		V
Low-level output voltage	V_{BC}L	$V_{CC} \le L_{BT}$		0.03	0.3	V

Block Diagram



Pin Functions

Pin No.	Pin	Function	Equivalent circuit
1 2	VCO1 VCO2	VCO input VCO output	
3	GND1	MOS system ground	
10 11	OSC1 OSC2	Local oscillator input Local oscillator output	
25 26	NF_{IN} NF_{OUT}	Noise filter input Noise filter output	
29	AF_{OUT}	FM detector output	

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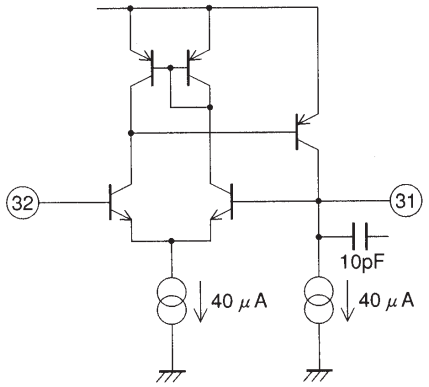
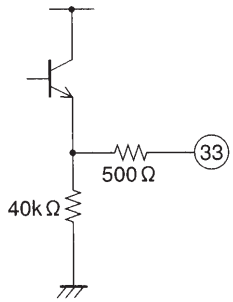
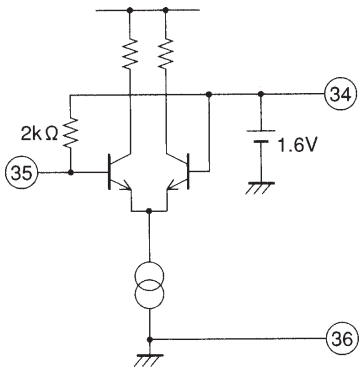
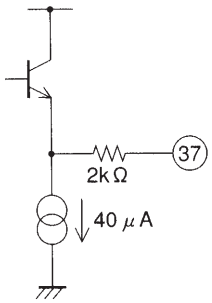
Pin No.	Pin	Function	Equivalent circuit
30	GND3	Low-frequency system ground	
31 32	P.S. 1 P.S. 2	Phase shifter operational amplifier output Phase shifter operational amplifier input	
33	IF_{OUT}	IF output	
34 35 36	$V_{REG}IF$ IF IN GND2	IF reference voltage IF input IF system ground	
37	2nd MIX OUT	Second mixer output	

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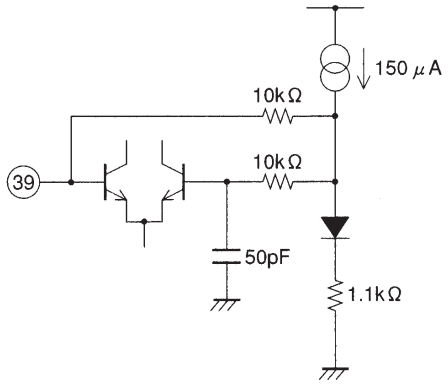
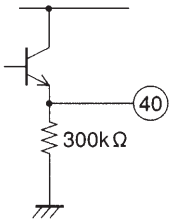
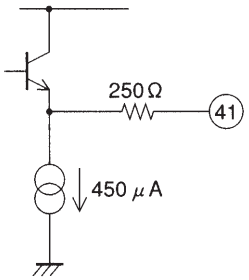
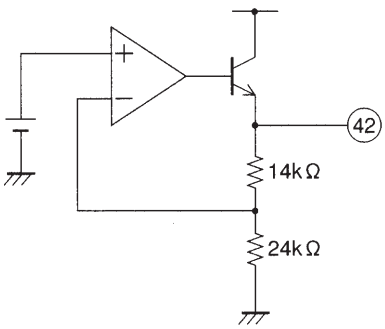
Pin No.	Pin	Function	Equivalent circuit
39	2nd MIX IN	Second mixer input	
40	N RCT	Noise detector	
41	1st MIX OUT	First mixer output	
42	VCO REG	VCO reference voltage	

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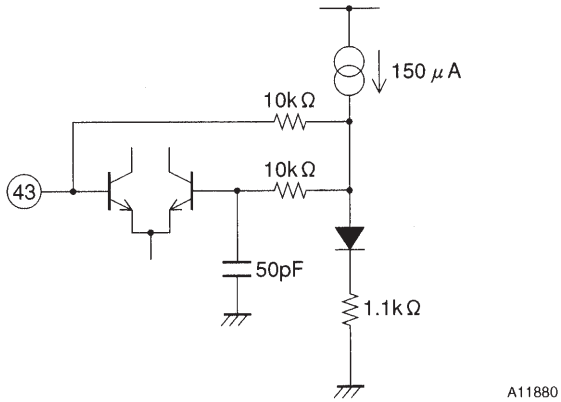
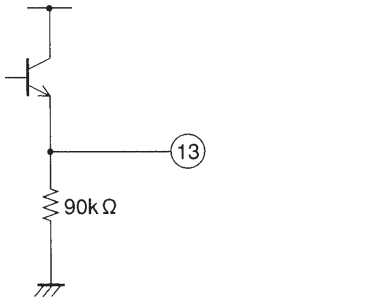
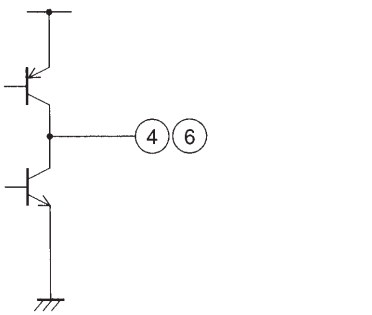
Pin No.	Pin	Function	Equivalent circuit
43	1st MIX IN	First mixer input	
44	GND4	VCO GND	
13	RSSI	RSSI output	
16	NS OUT		
4 6	RCP TCP	Receiver charge pump output Transmitter charge pump output	
5	$V_{CC}1$	MOS block latch power supply	

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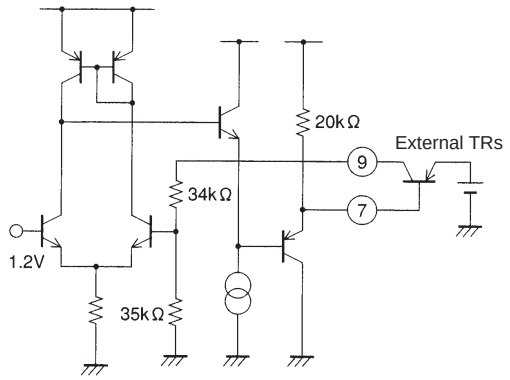
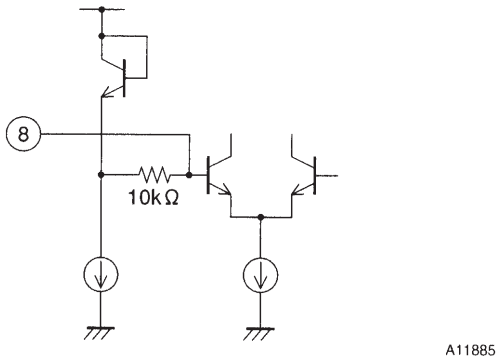
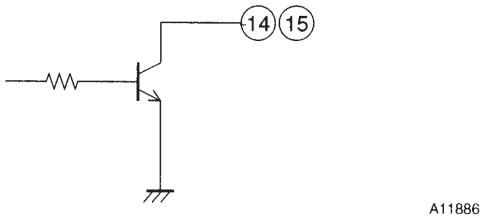
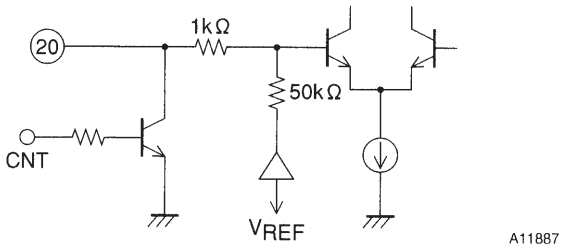
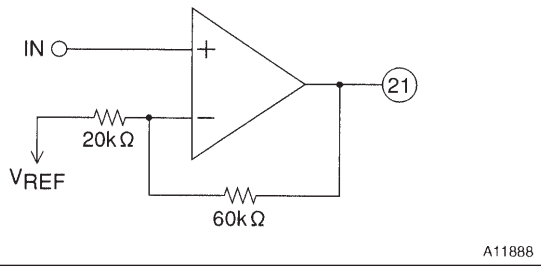
Pin No.	Pin	Function	Equivalent circuit
7 9	P-REG $V_{CC}2$	External transistor base input External transistor collector input (PLL power supply)	
8	PI	Transmitter comparison signal input	
12	$V_{CC}3$	Power supply	
14 15	FSK OUT LD OUT	FSK signal output Receiver unlock detection output	
17 18 19	CL DI CE	Data input CMOS input. Not built in pull-down resistor.	
20	TX DT IN	Transmitter data input	
21	TX OUT	Transmitter output Operational amplifier output (class A)	

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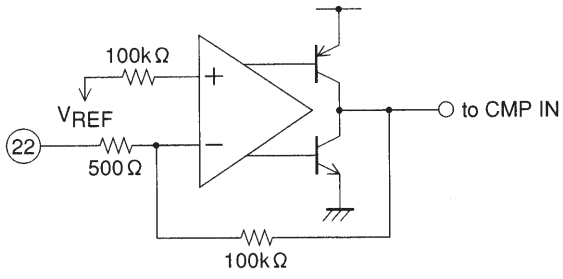
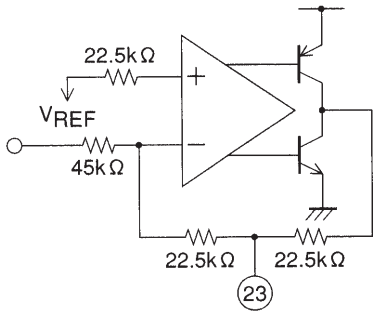
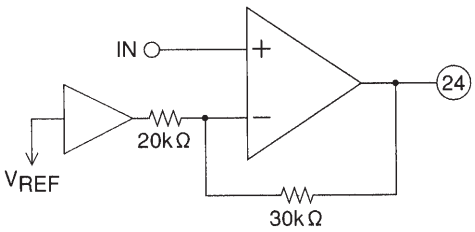
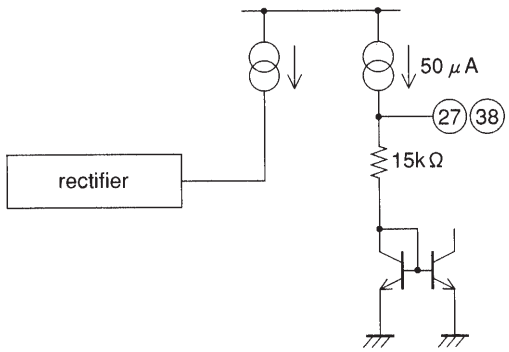
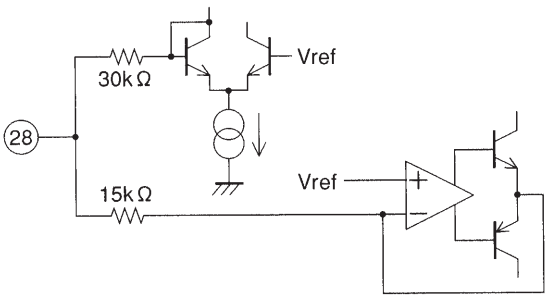
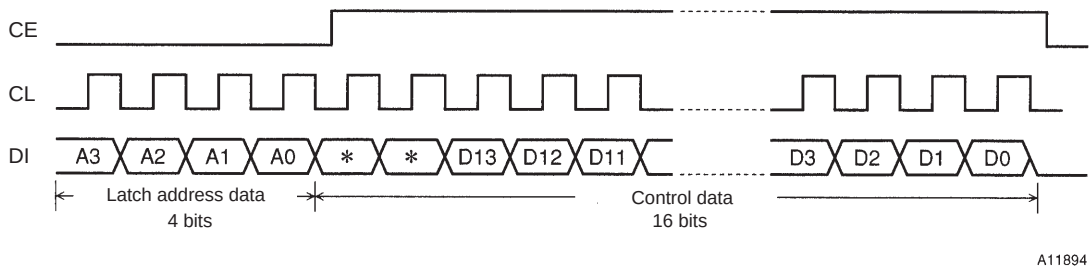
Pin No.	Pin	Function	Equivalent circuit
22	MIC IN	Microphone input	
23	CMP NF	Compressor noise filter connection	
24	RX OUT	Receiver output Operational amplifier output (class A)	
27 38	C RCT E RCT	Full-wave rectifier output	
28	RX IN	EXP input VCA/full-wave rectifier input block	

Serial Data Format



Latch address				Control data content
A3	A2	A1	A0	D13 to D0
1	0	0	0	12 bits: Reference divider counter value
0	1	0	0	14 bits: Receiver programmable divider counter value
1	1	0	0	14 bits: Transmitter programmable divider counter value
0	0	1	0	Control settings 1
1	0	1	0	Control settings 2

Latch address				Control data content													
A3	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
0	1	0	0	PR13	PR12	PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
1	1	0	0	PT13	PT12	PT11	PT10	PT9	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0
0	0	1	0	SB1	SB0	RMT	TMT	LVL	*	CR1	CR0	CT1	CT0	AR1	AR0	AT1	AT0
1	0	1	0	*	SCF2	SCF1	SCF0	SCFB	ULD	0	0	DZ	PE	ULT	CP	BT1	BT0

Control Data Function

- Reference divider counter value (R11 to R0)
  Binary value in which R0 is the lsb. The divisor can be set to a value in the range 32 to 4095. However, since there is a divide-by-2 circuit in the preceding stage, the actual divisor will be twice the set value.

  Example: With a 10.24 MHz crystal, to create a reference frequency fref of 5 kHz:
  10.24 MHz/5 kHz/2 gives a divisor of: 1024
  Set R11 to R0 to the value 1024 (0400 hexadecimal).

UK1	UK0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
0	0	0	1	0	0	0	0	0	0	0	0	0	0

- Receiver programmable divider counter value (PR13 to PR0)
  Binary value in which PR0 is the lsb. The divisor can be set to a value in the range 256 to 16383.

  Example: To create the receiver VCO frequency of 38.975 MHz when fref is 5 kHz:
  38.975/5 kHz gives a divisor of: 7795
  Set PR11 to PR0 to the value 7795 (1E73 hexadecimal).

PR13	PR12	PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
0	1	1	1	1	0	0	1	1	1	0	0	1	1

- Transmitter programmable divider counter value (PT13 to PT0)
  Binary value in which PT0 is the lsb. The divisor can be set to a value in the range 256 to 16383.

  Example: To create the transmitter VCO frequency of 46.610 MHz when fref is 5 kHz:
  46.610/5 kHz gives a divisor of: 9322
  Set PT11 to PT0 to the value 9322 (246A hexadecimal).

PT13	PT12	PT11	PT10	PT9	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0
1	0	0	1	0	0	0	1	1	0	1	0	1	0

- Power saving mode settings

SB1	SB0	Setting
0	0	1 st L0 VCO, 2 nd L0 OSC, RX-PLL blocks operate.
0	1	1 st L0 VCO, 2 nd L0 OSC, RX-PLL, 1 st mixer, 2 nd mixer, IF detect, Noise detect, Data shaper, SCF (data system) operate.
1	0	All blocks operate
1	1	All blocks operate

- Baseband muting control

  Receiver audio signal

RMT	State
0	Receiver system audio signal muted
1	Receiver system audio signal mute released

  Transmitter audio signal

TMT	State
0	Transmitter system audio signal muted
1	Transmitter system audio signal mute released

- Audio level control (receiver system output)

LVL	State
0	Standard level
1	Boosted level (boosted by about +7.4 dB)

• Charge pump output current control (manual switching)
The charge pump circuit output current is controlled manually.

(Receiver charge pump output current)
These control states are valid only when both AR0 and AR1 are set to 0.

CR1	CR0	State
0	0	CRA
0	1	CRB
1	0	CRC
1	1	CRD

Current level: CRA > CRB > CRC > CRD

(Transmitter charge pump output current)
These control states are valid only when both AT0 and AT1 are set to 0.

CT1	CT0	State
0	0	CTA
0	1	CTB
1	0	CTC
1	1	CTD

Current level: CTA > CTB > CTC > CTD

• Charge pump output current control (automatic switching)
The charge pump circuit output current is controlled automatically.
(Receiver charge pump output current)

AR1	AR0	State
0	0	Manual switching is enabled
0	1	The circuit operates in CRA mode until the receiver PLL locks, and then switches to CRC mode when the circuit locks
1	0	The circuit operates in CRB mode until the receiver PLL locks, and then switches to CRD mode when the circuit locks
1	1	Manual switching is enabled

Current level: CRA > CRB > CRC > CRD

(Transmitter charge pump output current)

AT1	AT0	State
0	0	Manual switching is enabled
0	1	The circuit operates in CTA mode until the transmitter PLL locks, and then switches to CTC mode when the circuit locks
1	0	The circuit operates in CTB mode until the transmitter PLL locks, and then switches to CTD mode when the circuit locks
1	1	Manual switching is enabled

Current level: CTA > CTB > CTC > CTD

• SCF clock frequency switching
Low-pass filter 1 (splatter filter)

SCF2	SCF1	SCF0	SCF clock divisor	Cutoff frequency
0	0	0	60	3.313 kHz
0	1	0	62	3.206 kHz
1	0	0	58	3.427 kHz
0	0	1	66	3.106 kHz
0	1	1	68	3.011 kHz
1	0	1	64	2.923 kHz

Low-pass filter 2 (Receiver data input filter)

SCFB	SCF clock divisor	Cutoff frequency
0	60	3.313 kHz
1	120	1.656 kHz

• Unlock detection width control

This bit sets the phase error detection width for PLL locked/unlocked discrimination. The unlocked state is detected when the phase error listed in the table below occurs.

ULD	Phase error detection width	When the second crystal frequency is 10.24 MHz
0	±4/2nd Xtal	390 ns
1	±8/2nd Xtal	780 ns

Note: If this bit is changed while the PLL circuit is locked, lock will be lost temporarily.

• Phase error output control

Controls whether the unlock output pin (pin 15) output is set to the post-unlock detection output, or directly outputs phase detector phase error without modification.

PE	State
0	The unlock detector result is output
1	The phase detector phase error is output without modification

• Dead zone control

Controls the phase comparator dead zone.

DZ	State
0	DZA
1	DZB

DZA < DZB

• Transmitter unlock detector function

Pin 20 normally functions as the data addition amplifier input. However, it operates as the transmitter system unlock detector output if ULT is set to 1.

ULT	State
0	Data addition amplifier input function enabled
1	Transmitter unlock detector output function enabled

• Charge pump circuit on/off function

CP	State
0	Charge pump circuit turned on
1	Charge pump circuit turned off

• Battery check function

Pin 15 normally outputs the receiver unlock detector output. However, it can be set to function as the battery tester with the following mode settings.

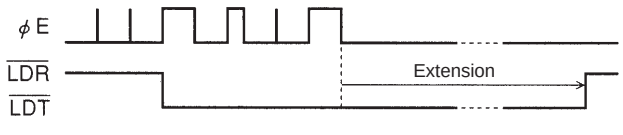
BT1	BT0	Mode
0	0	Receiver unlock detector output enabled
0	1	Supply voltage detection level 1 (V_{CC} ≈ 3.3 V)
1	0	Supply voltage detection level 2 (V_{CC} ≈ 3.05 V)
1	1	Supply voltage detection level 3 (V_{CC} ≈ 2.85 V)

• Phase error extension time

The time the detected phase error signal is extended.

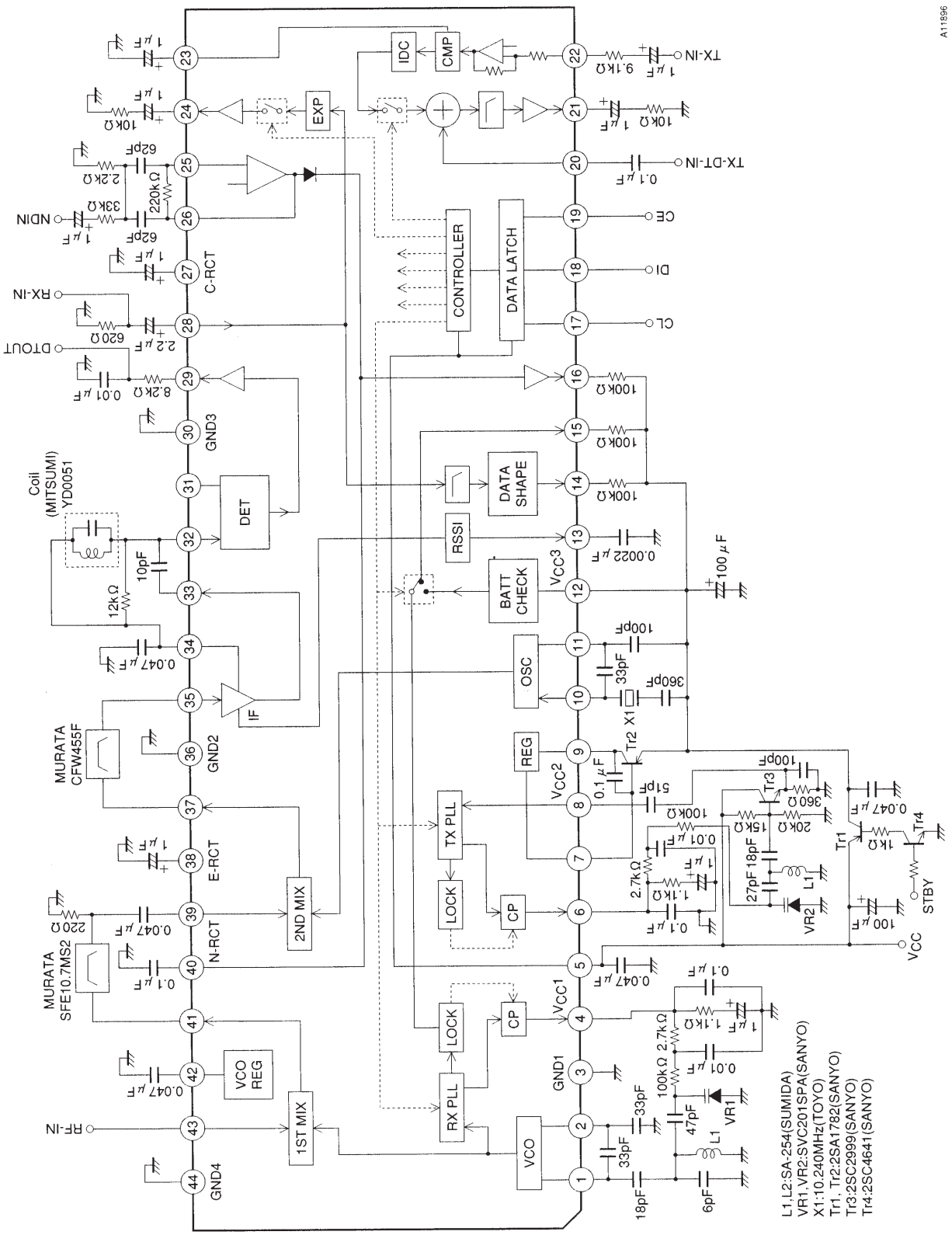
Extension time = 32 × (1/fref) = 32/5 kHz = 6.4 ms

(fref = reference frequency)

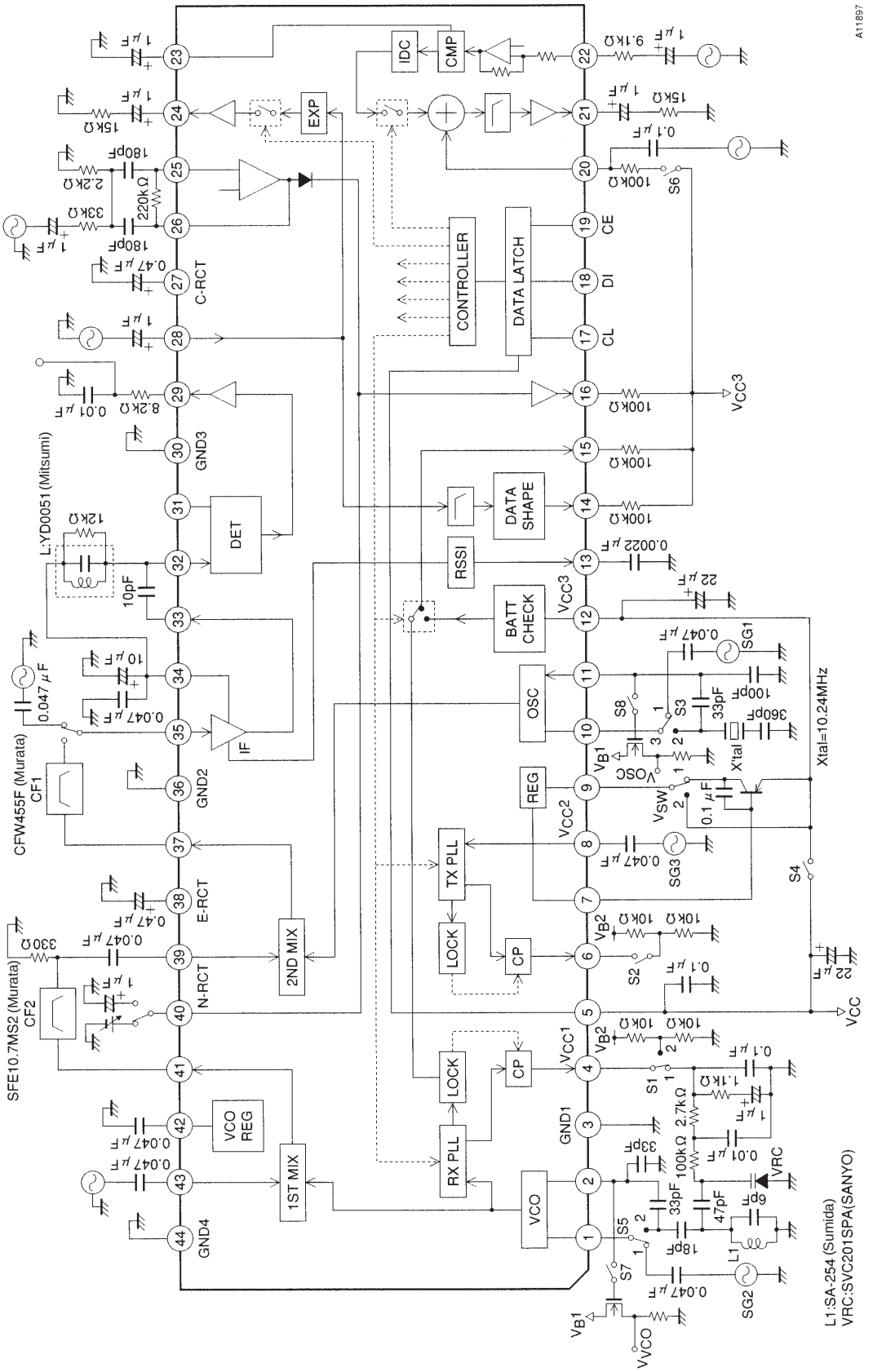


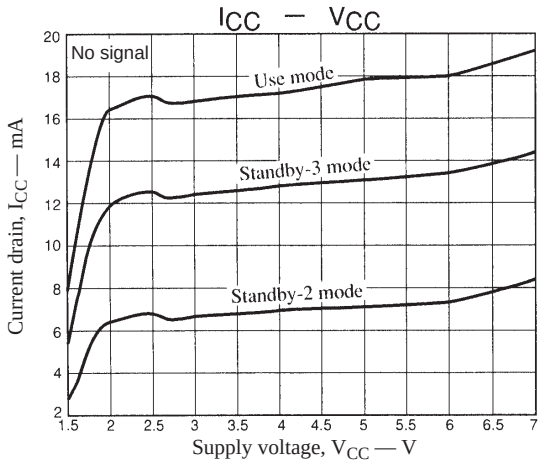
A11895

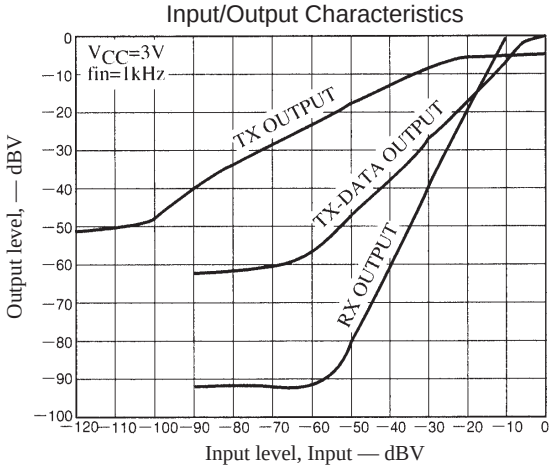
Sample Application Circuit

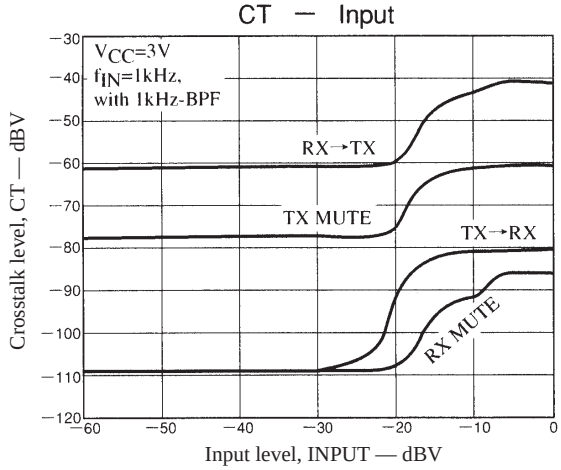


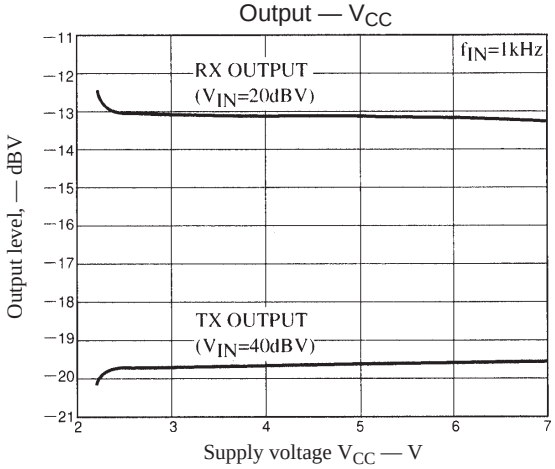
Test Circuit

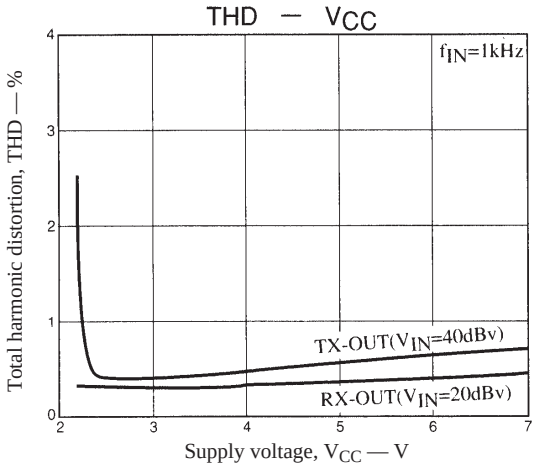


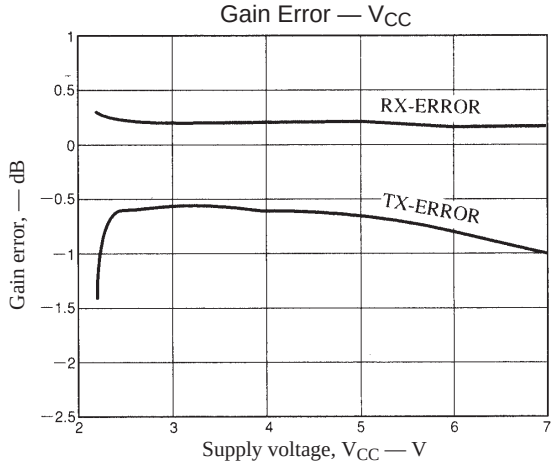

ICC — VCC
No signal
Use mode
Standby-3 mode
Standby-2 mode
Current drain, ICC — mA
Supply voltage, VCC — V

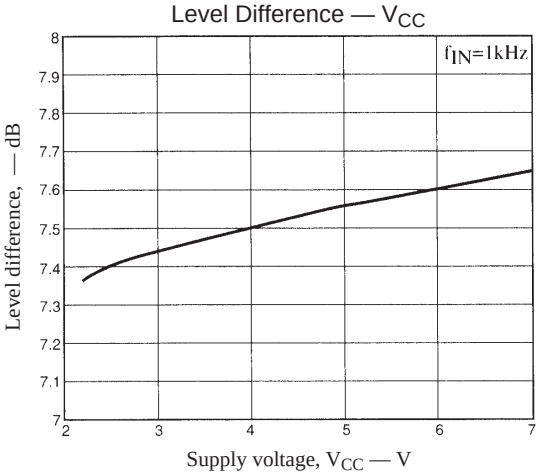

Input/Output Characteristics
VCC=3V
fin=1kHz
TX OUTPUT
TX-DATA OUTPUT
RX OUTPUT
Output level, — dBV
Input level, Input — dBV

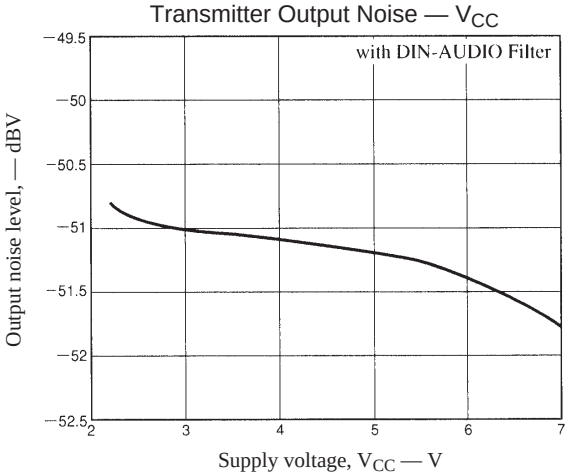

CT — Input
VCC=3V
fIN=1kHz,
with 1kHz-BPF
RX→TX
TX MUTE
TX→RX
RX MUTE
Crosstalk level, CT — dBV
Input level, INPUT — dBV


Output — VCC
fIN=1kHz
RX OUTPUT
(VIN=20dBV)
TX OUTPUT
(VIN=40dBV)
Output level, — dBV
Supply voltage VCC — V

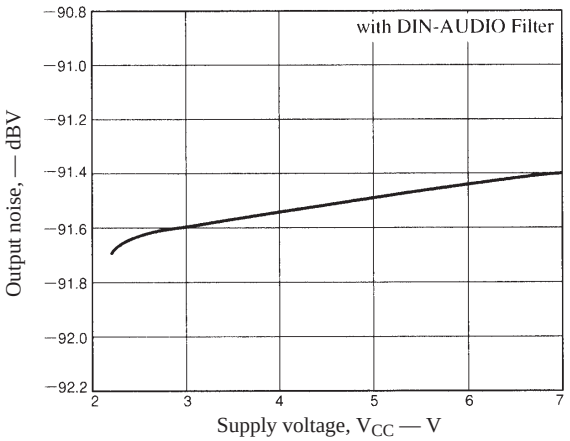

THD — VCC
fIN=1kHz
TX-OUT(VIN=40dBv)
RX-OUT(VIN=20dBv)
Total harmonic distortion, THD — %
Supply voltage, VCC — V


Gain Error — VCC
RX-ERROR
TX-ERROR
Gain error, — dB
Supply voltage, VCC — V

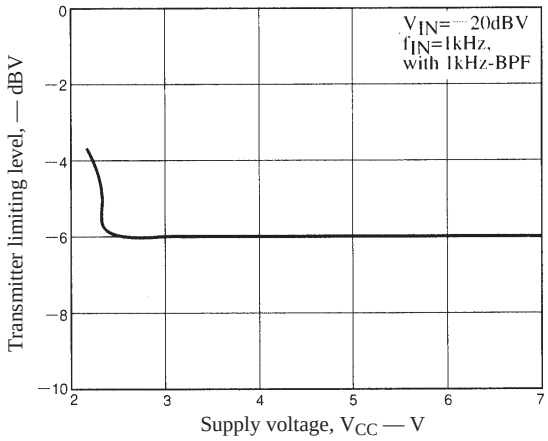

Level Difference — VCC
fIN=1kHz
Level difference, — dB
Supply voltage, VCC — V


Transmitter Output Noise — VCC
with DIN-AUDIO Filter
Output noise level, — dBV
Supply voltage, VCC — V

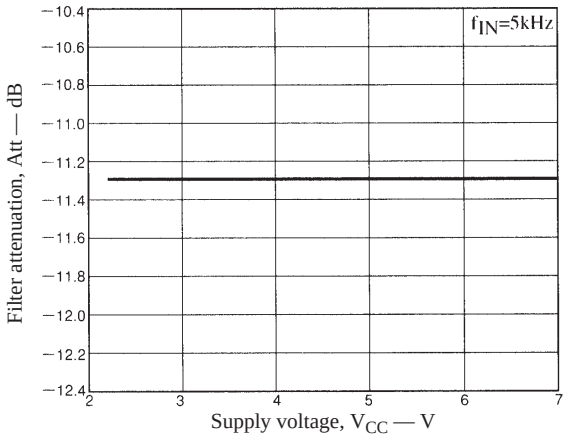
Receiver Output Noise — V_{CC}



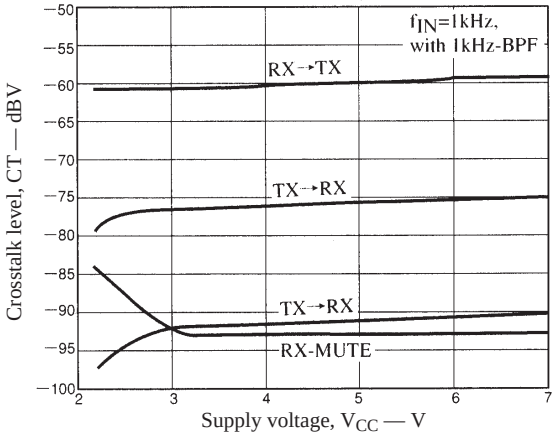
Transmitter Limiting Level — V_{CC}



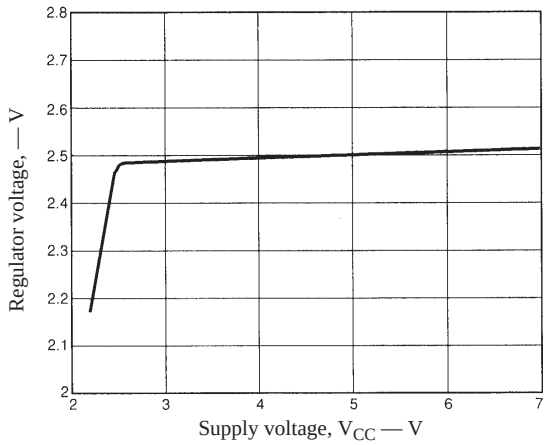
Splatter Filter Attenuation — V_{CC}



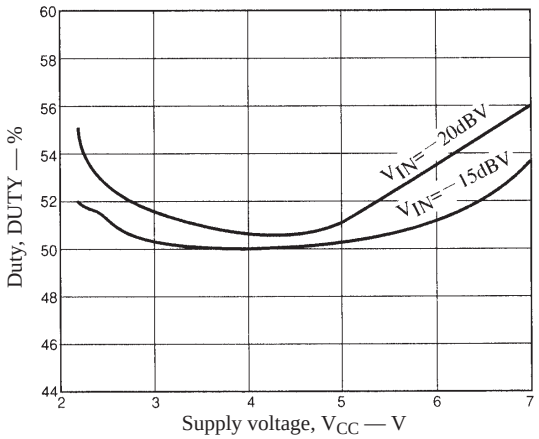
CT — V_{CC}



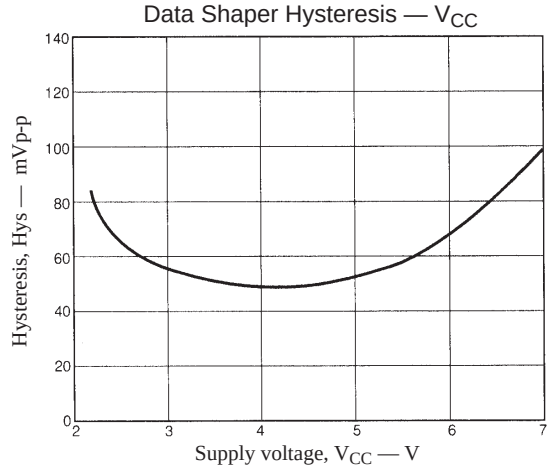
PLL Regulator Voltage — V_{CC}



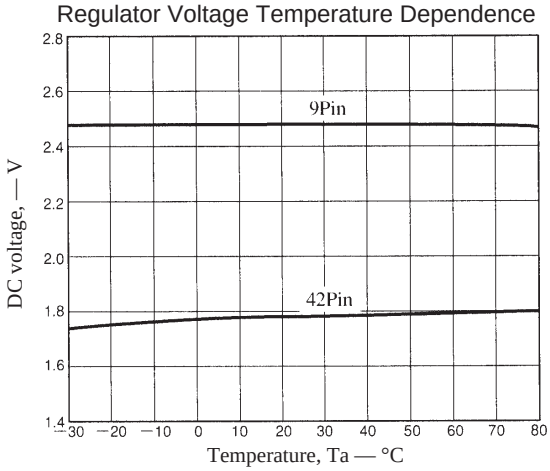
Data Shaper Duty



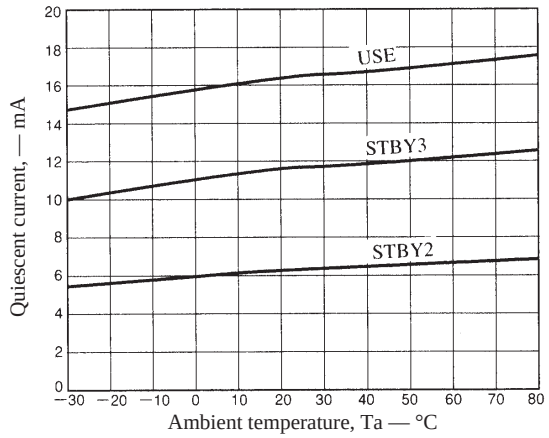
Data Shaper Hysteresis — V_{CC}



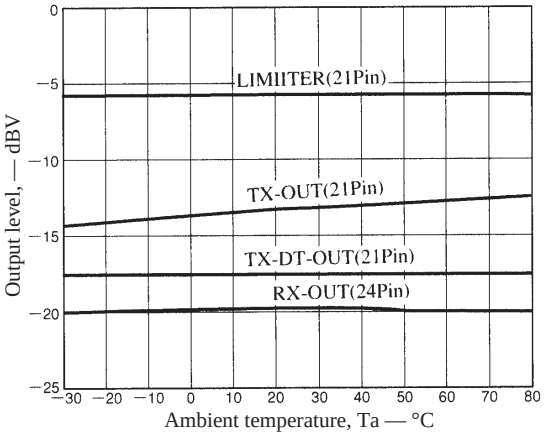
Regulator Voltage Temperature Dependence



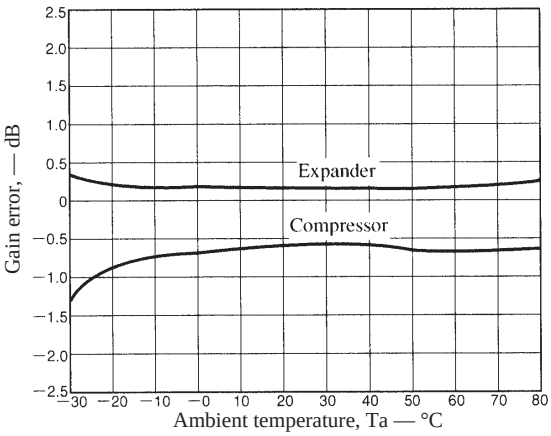
Quiescent Current Temperature Characteristics



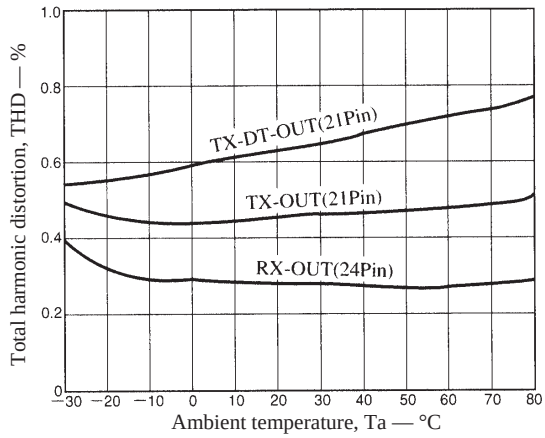
Output Level Temperature Characteristics



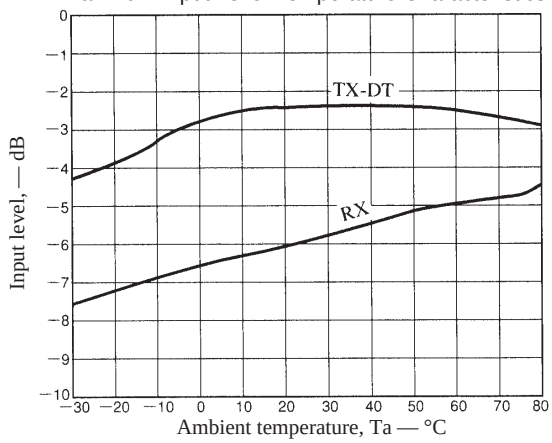
Compander Gain Error Temperature Characteristics



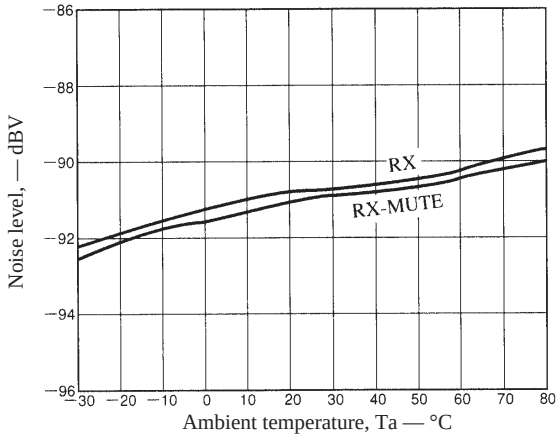
Output Distortion Temperature Characteristics



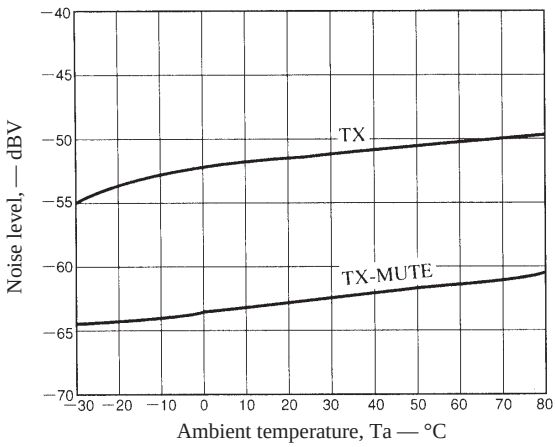
Maximum Input Level Temperature Characteristics



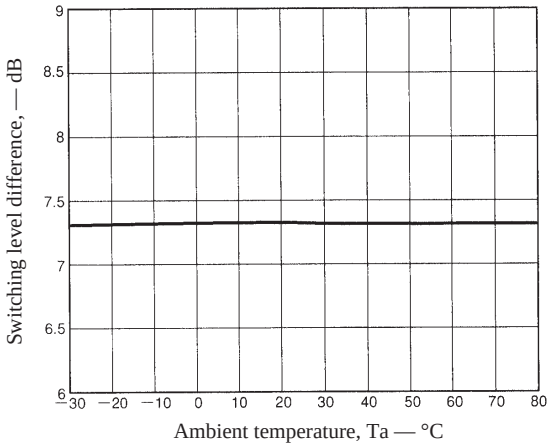
RX Noise Leval — Ta



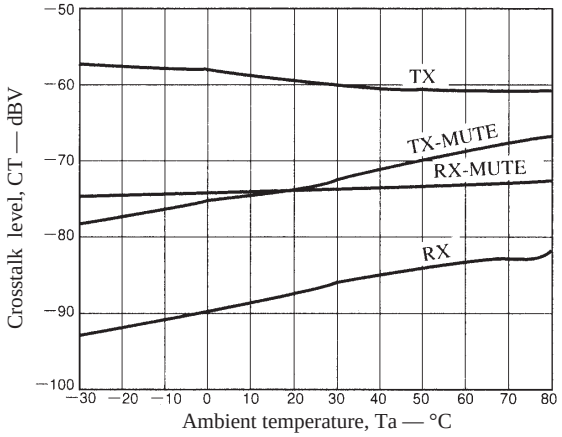
TX Noise Leval — Ta



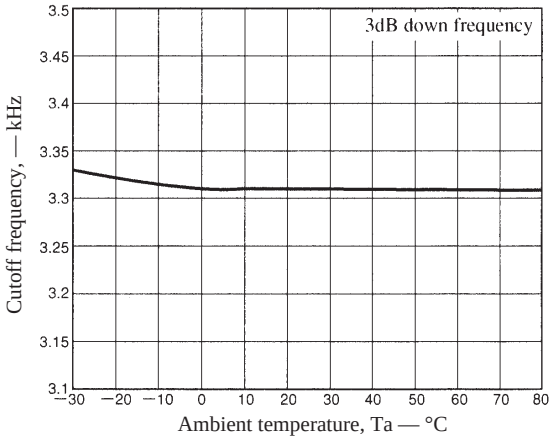
Receiver System Output Switching Level Difference Temperature Characteristics



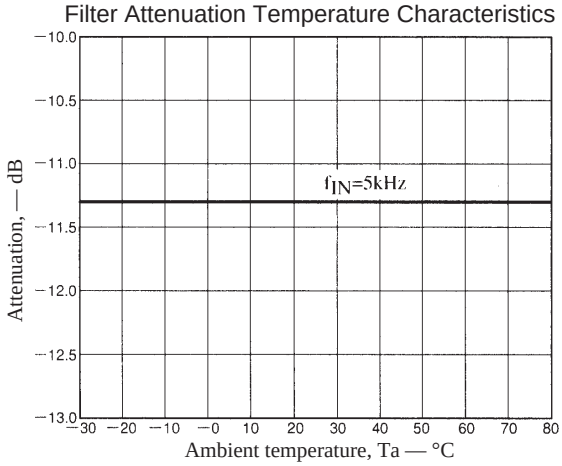
CT — Ta



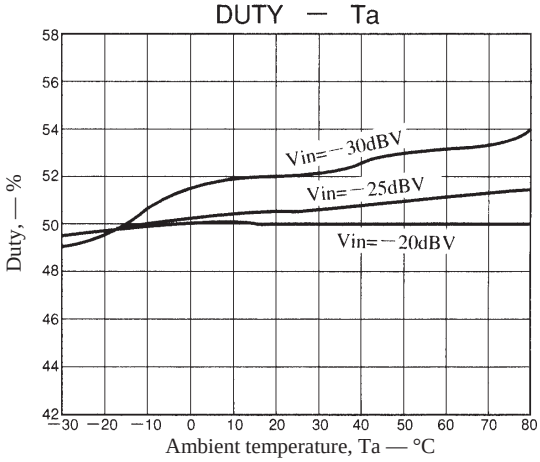
Filter Cutoff Frequency Temperature Characteristics



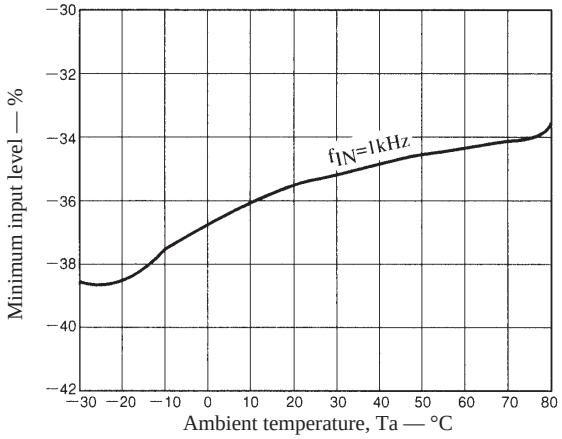
Filter Attenuation Temperature Characteristics



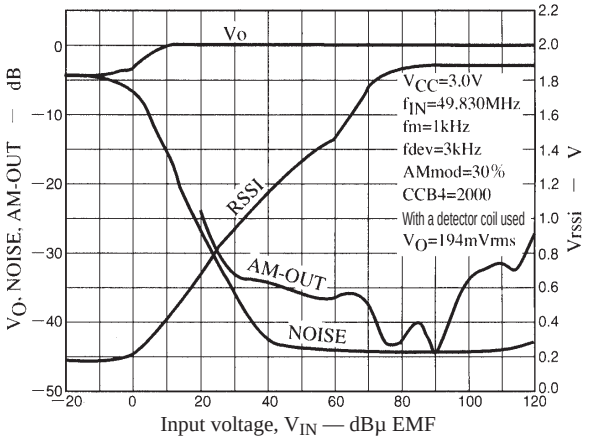
DUTY — Ta



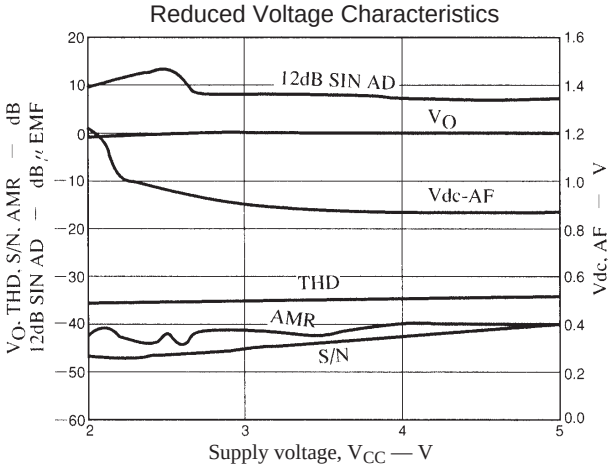
Data Shaper Input Sensitivity Temperature Characteristics



Input/Output Characteristics

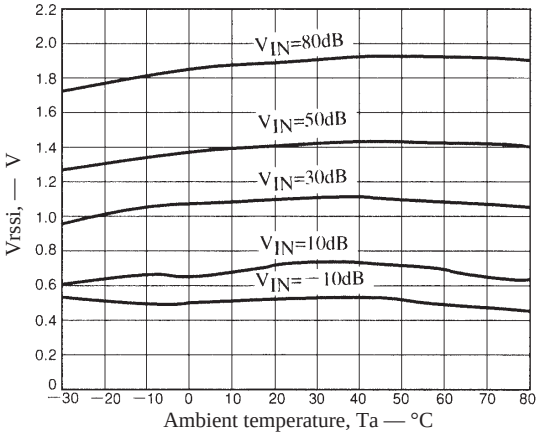


Reduced Voltage Characteristics



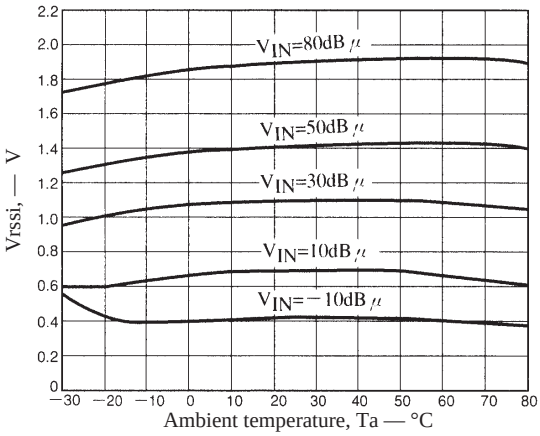
VCC=3.0V
fIN=49.830MHz
fm=1kHz
fdev=3kHz
AMmod=30%
CCB4=2000
With a detector coil used
VO=194mVrms

RSSI Temperature Dependence



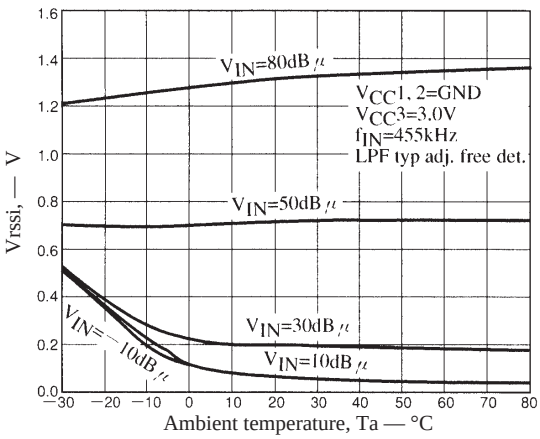
V_{CC}1, 2, 3=3.0V
f_{IN}=49.830MHz
CCB4=1000
V_{CC}1, 2=GND
V_{CC}3=3.0V
f_{IN}=49.830MHz
fm=1.0kHz
△f=±3kHz
V_{IN}=80dBμ EMF
fvco=39.135MHz
Vvco=100dBμ EMF
fosc=10.240MHz
Vosc=100mVrms
Logic-Block off
LPF typ adj.free det.

RSSI Temperature Characteristics

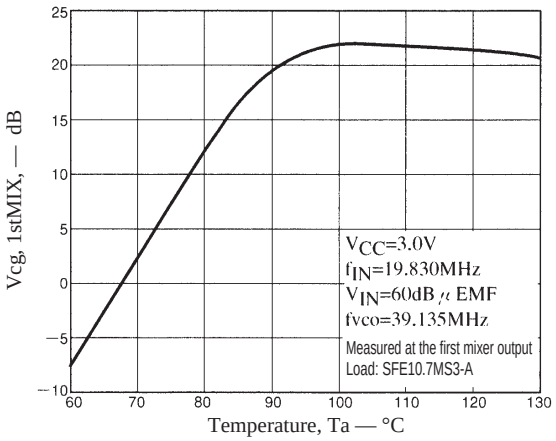


V_{CC}1, 2=GND
V_{CC}3=3.0V
f_{IN}=49.830MHz
fm=1.0kHz
△f=±3kHz
V_{IN}=80dBμ EMF
fvco=39.135MHz
Vvco=100dBμ EMF
fosc=10.240MHz
Vosc=100mVrms
Logic-Block off
LPF typ adj.free det.

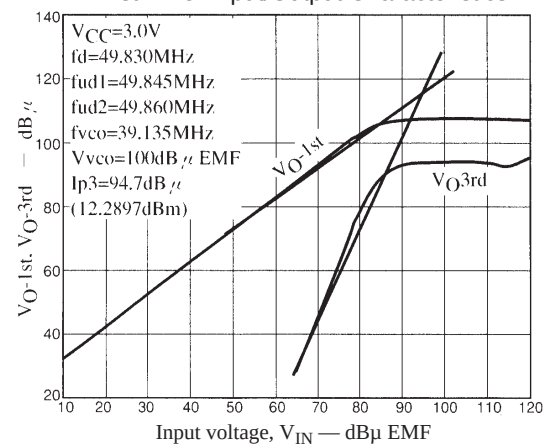
RSSI Temperature Characteristics



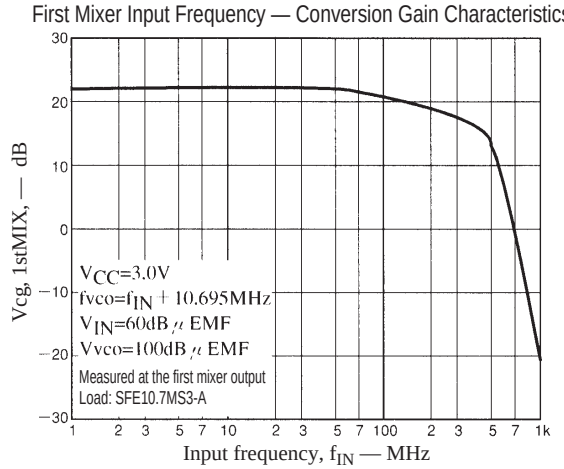
First Mixer Conversion Gain



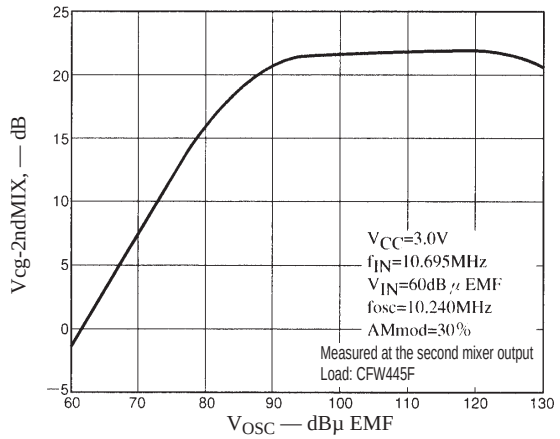
First Mixer Input/Output Characteristics



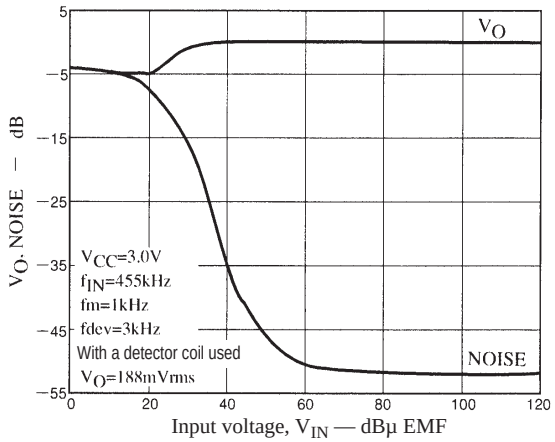
First Mixer Input Frequency — Conversion Gain Characteristics



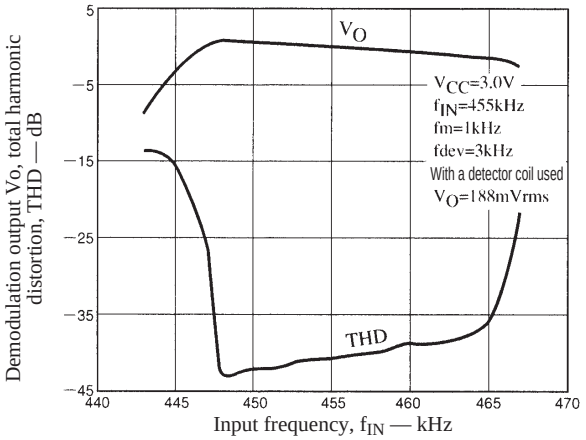
Second Mixer Conversion Gain



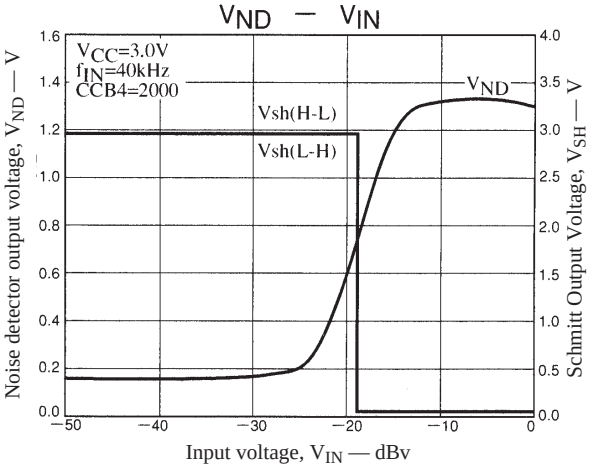
IF Amplifier Input/Output Characteristics



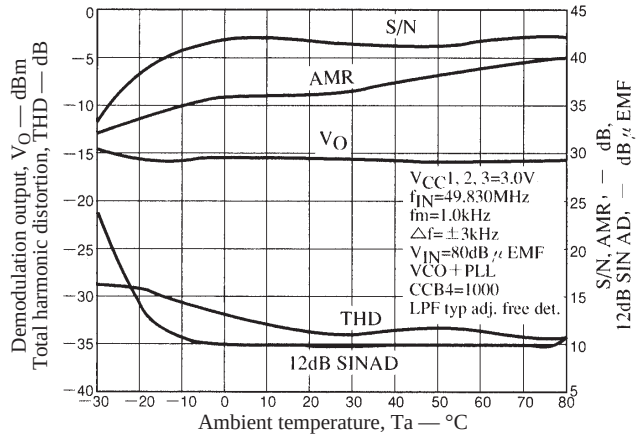
Detuning Characteristics



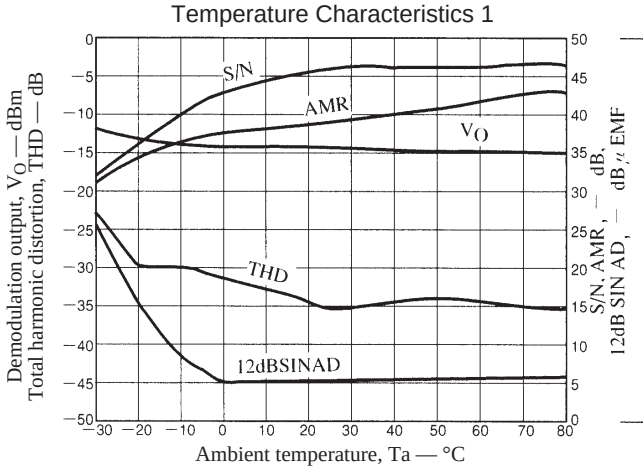
VND — VIN



Temperature Characteristics 1

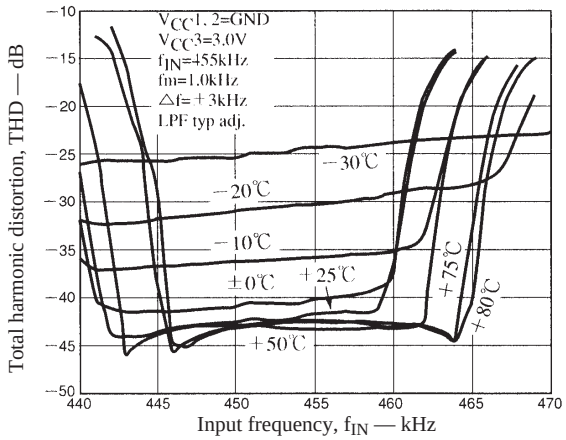


Temperature Characteristics 1

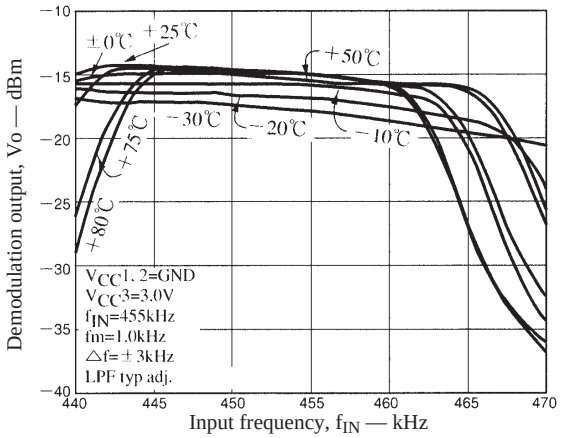


VCC1, 2=GND
VCC3=3.0V
fIN=49.830MHz
fm=1.0kHz
△f=±3kHz
VIN=80dB,μ EMF
fvco=39.135MHz
Vvco=100dB,μ EMF
fosc=10.240MHz
Vosc=100mVrms
Logic-Block off
LPF typ adj. free det.

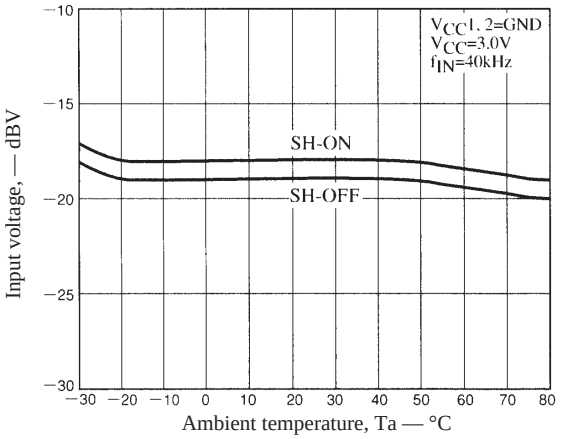
Detuning Characteristics



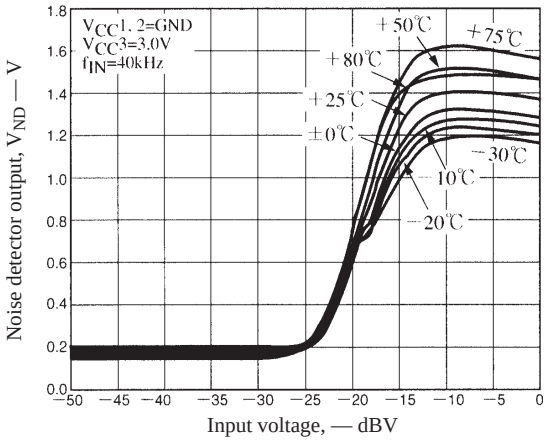
V_O Detuning Characteristics



Noise Schmitt Temperature Characteristics



Noise Detector Output Voltage



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