Bi-CMOS IC



http://onsemi.com

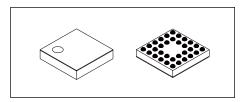
Blurring correction driver H bridge × 2-channel driver

Overview

LV8415XA is dual channel H-bridge driver IC for digital still camera.

Function

- Actuator driver (saturation drive H bridge) × 2-channel
- Hall Amplifier × 2-channel
- Constant current hall bias circuit × 2-channel
- General-purpose amplifier × 2-channel
- With built-in for PWM signal generation logic circuit × 2-channel
- 8-bit DAC for hall bias × 2-channel
- 8-bit DAC for hall amplifier offset adjustment × 2-channel
- Three line serial input
- Two systems in power supply (V_M: for actuator, V_{CC})
- With built-in thermal protection circuit
- With built-in low voltage malfunction prevention circuit



WLP32L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V _M max		6	V
Supply voltage 2	V _{CC} max		6	٧
Output peak current	I _O peak	OUT1 to 2 (t ≤ 10msec, duty ≤ 20%)	600	mA
Output current	I _O max	OUT1 to 2	350	mA
Hall bias current	I _{HB} max		5	mA
Allowable power dissipation	Pd max	On a specified board *	1	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

^{*} Specified board: 40.0mm×50.0mm×0.8mm, Four layers fiberglass epoxy circuit board.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	v _M		2.7 to 5.5	V
Supply voltage range 2	V _{CC}		2.7 to 5.5	V
Logic input voltage	V _{IN}		0 to V _{CC} +0.3	V

ORDERING INFORMATION

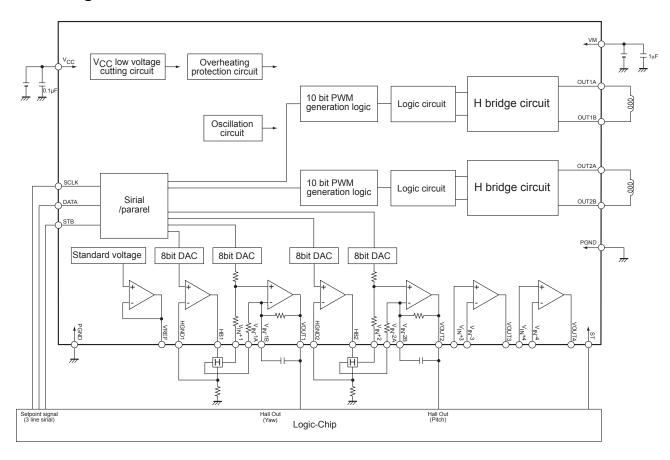
See detailed ordering and shipping information on page 13 of this data sheet.

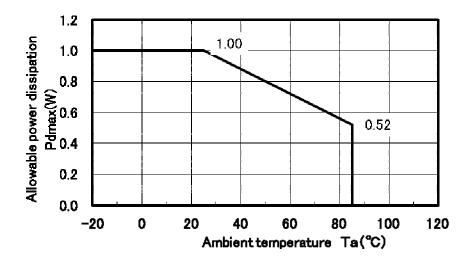
^{*2} Tjmax=150°C Please design PCB so that internal chip temperature does not exceed 150 °C.

Electrical Characteristics at $Ta=25^{\circ}C,\,V_{CC}=3.3V,\,V_{M}=5.0V$

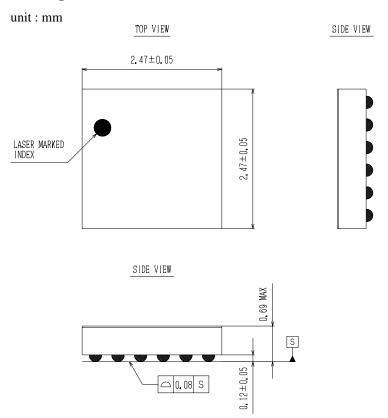
Parameter	Symbol	Conditions		Ratings		Unit
Farameter	Symbol	Conditions	min	typ	max	Offic
Current consumption when standing by	Icco	ST = "L"			1.0	μА
VM current consumption	I _M	V _M = 5.0V, ST = "H", no load			10	μА
V _{CC} current consumption	Icc	ST = "H", no load		2	3.2	mA
V _{CC} low voltage cutting voltage	VTHVCC		2.1	2.40	2.6	V
Low voltage hysteresis voltage	VTHHYS		100	150	200	mV
Thermal shutdown temperature	TSD	Design guarantee	155	175	195	°C
Thermal hysteresis width	ΔTSD	Design guarantee	15	35	55	°C
H bridge output (OUT1-2)		·		•		
Output on resistance	Ronu	I _O = 100mA, Upper-side on resistance		0.7	0.98	Ω
	Rond	I _O = 100mA, Under-side on resistance		0.5	0.7	Ω
Output leakage current	I _O leak				1	μА
Diode forward voltage	VD	ID = -100mA		0.7		V
Operational amplifier (OP-AMP	1-4)	•				
Input offset voltage	OP_VIO			±1	±5	mV
Input offset current	OP_IIO			±5	±50	nA
Input bias current	OP_IB			30	250	nA
Equal phase input voltage range	VICM		0		VCC	V
Equal phase signal removal ratio	CMR	R _L = 20kΩ, VIN = 1mV(open loop gain)	60	80		dB
Large amplitude voltage range	VG	R _L = 20kΩ	1	10		V/mV
Output voltage range	V _O H	R _L = 20kΩ	V _{CC} -0.2			V
	V _O L				0.2	V
Power supply change removal ratio	SVR		65	85		dB
Output current (sink/source)	OP_IO		1	2		mA
Hall bias (HB1-2)	I.			<u> </u>		
Output current	IHB	RHG = 1kΩ, VHBIN = 1.0V	0.95	1.00	1.05	mA
Output saturation voltage	VSATHB	I _{HB} = 1mA	V _{CC} -0.2			V
Reference voltage	•			•		
Reference voltage	VREF		1.60	1.65	1.70	V
Reference voltage load	VRref	I _{REF} = 100μA	1.60	1.65	1.70	V
characteristic						
Internal CLK frequency for PWI	/I drive					
CLK frequency	Fclk		13.5	15	17.25	MHz
Control pin (ST, SCLK, DATA, S	ТВ)					
Built-in pull-down resistance	Rin		50	100	200	kΩ
Input current	I _{IN} L	V _{IN} = 0V			1.0	μΑ
	I _{IN} H	V _{IN} = 3.3V	20	33	50	μА
Input "L" level voltage	V _{IN} L				1.0	V
Input "H" level voltage	V _{IN} H		2.5			V

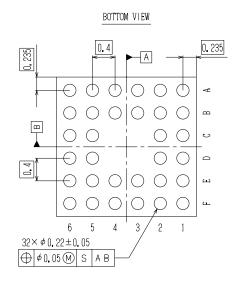
Block Diagram



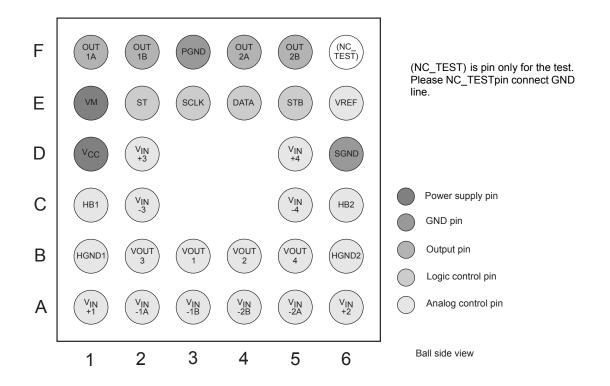


Package Dimensions





Pin Assignment



Pin function

Pin fund			
Pin No.	Pin name	Pin function	Equivalent Circuit
E2 E3 E4 E5	ST SCLK DATA STB	Input pin. High level 2V to (V _{CC} = 3.3V) Low level 0 to 0.5V (V _{CC} = 3.3V) Output pin. (PWM output)	30kΩ VCC 30kΩ GND
F2 F4 F5 E1 F3	OUT1B OUT2A OUT2B VM PGND	VM : POWER – Power supply pin. PGND : POWER – GND pin.	
D1 D6	V _{CC} SGND	Signal system power supply pin Signal system GND pin	
C1 B1 C6 B6	HB1 HGND1 HB2 HGND2	HB1, 2 pin Hall bias source pin HGND1, 2 pin Hall bias current setting pin	VCC IN HGND GND HB
A1 A2 A3 A6 A5 A4	V _{IN} +1 V _{IN} -1A V _{IN} -1B V _{IN} +2 V _{IN} -2A V _{IN} -2B	Hall amplifier input pin VIN+ Hall amplifier+ input pin VIN-A Hall amplifier- input pin VIN-B LPF formation pin (The filter is formed for the noise removal.)	$\begin{array}{c} \text{VCC} \\ \text{NB} \\ 3.6 \text{k} \Omega \\ 3 \text{k} \Omega \end{array}$
B3 B4	VOUT1 VOUT2	Hall amplifier output pin. VOUT1 : Hall amplifier 1ch output pin. VOUT2 : Hall amplifier 2ch output pin.	OT OT

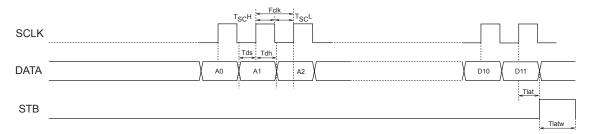
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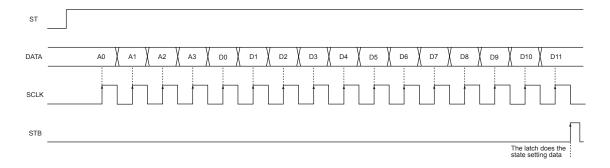
Pin No.	Pin name	Pin function	Equivalent Circuit
D2 C2 D5 C5	V _{IN} +3 V _{IN} -3 V _{IN} +4 V _{IN} +4	General purpose amplifier input pin. VIN+3: 3ch general purpose amplifier+ input pin VIN-3: 3ch general purpose amplifier- input pin VIN+4: 4ch general purpose amplifier+ input pin VIN-4: 4ch general purpose amplifier- input pin	VCC 3kΩ 1NN
B2 B5	VOUT3 VOUT4	General purpose amplifier output pin. VOUT3 : 3ch general purpose amplifier output pin VOUT4 : 4ch general purpose amplifier output pin	WCC TOTO
E6	VREF	Internal standard voltage pin V _{CC} /2 output	VCC 3kΩ VREF GND
F6	NC-TEST	N.C. pin TEST pin Please NC_TEST pin connect GND line.	VCC 1kΩ 10kΩ § GND

3 line serial communication electrical Characteristics at Ta = 25°C, V_{CC} = 3.3V, V_{M} = 5.0V

D l	O what	Q IV		Ratings		11.2
Parameter	Symbol	Conditions	min	typ	max	Unit
Serial data forwarding pin						
Logic pin input current	I _{IN} L	V _{IN} =0V(SCLK, DATA, STB)			1.0	μА
	I _{IN} H	V _{IN} =3.3V(SCLK, DATA, STB)		33	50	μА
Input "H" level voltage	V _{IN} H	SCLK, DATA, STB	2.5			V
Input "L" level voltage	V _{IN} L	SCLK, DATA, STB			1.0	V
Minimum SCLK "H" pulse width	T _{SC} H		0.1			μS
Minimum SCLK "L" pulse width	T _{SC} L		0.1			μS
STB regulation time	Tlat		0.1			μS
Minimum STB pulse width	Tlatw		0.1			μS
Data set-up time	Tds		0.1			μS
Data hold time	Tdh		0.1			μS
maximum CLK frequency	Fclk				4	MHz



Serial data timing condition Serial data input timing chart



It inputs it from A0 in order of D11. The data transfer is done by the rising edge, and after all data transfers, the latch does all data to SCLK by the STB signal standing up. The STB signal accepts and the internal logic of IC doesn't accept the SCLK signal during "H".

Serial logic map

PWMh - bridge relation serial map

						3 01141		nput										
A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	Setting mode	Set content	Remarks
0	0	0	0	*	*	0	0	0	0	0	0	0	0	0	0		100%	
0	0	U	U	*	*	1	0	0	0	0	0	0	0	0	0		511/512 × 100%	
				*	*	0	1	0	0	0	0	0	0	0	0		510/512 × 100%	
				•	-	U	1	U	U	U	U	U	U	U	U			Reverse
				*	*	0	1	1	1	1	1	1	1	1	0		2/512 1000/	
				*	*	0	1	1	1	1	1	1	1	1	0		2/512 × 100%	
				*	*	1	1	1	1	1	1	1	1	1	0		1/512 × 100%	2011
				*	*	0	0	0	0	0	0	0	0	0	1	1ch PWM Duty set	0%	Middle point
				*	*	1	0	0	0	0	0	0	0	0	1		1/512 × 100%	
				*	*	0	1	0	0	0	0	0	0	0	1		2/512 × 100%	
																		Normal
				*	*	1	0	1	1	1	1	1	1	1	1		509/512 × 100%	rotation
				*	*	0	1	1	1	1	1	1	1	1	1		510/512 × 100%	
				*	*	1	1	1	1	1	1	1	1	1	1		511/512 × 100%	
1	0	0	0	*	*	0	0	0	0	0	0	0	0	0	0		100%	
				*	*	1	0	0	0	0	0	0	0	0	0		511/512 × 100%	
				*	*	0	1	0	0	0	0	0	0	0	0		510/512 × 100%	D
																		Reverse
				*	*	0	1	1	1	1	1	1	1	1	0		2/512 × 100%	
				*	*	1	1	1	1	1	1	1	1	1	0		1/512 × 100%	
				*	*	0	0	0	0	0	0	0	0	0	1	2ch PWM Duty set	0%	Middle point
				*	*	1	0	0	0	0	0	0	0	0	1		1/512 × 100%	point
				*	*	0	1	0	0	0	0	0	0	0	1		2/512 × 100%	
						-	-	0	0						1		2/312 × 100/0	Normal
				*	*	1	0	1	1	1	1	1	1	1	1		509/512 × 100%	rotation
				*	*	0	1	1	1	1	1	1	1	1	1		510/512 × 100%	
				*	*	1	1	1	1	1	1	1	1	1	1		511/512 × 100%	
0	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*		0V	
				1	0	0	0	0	0	0	0	*	*	*	*		1/255 × VREF	
				0	1	0	0	0	0	0	0	*	*	*	*		2/255 × VREF	
												*	*	*	*	1ch hall bias set		
				1	0	1	1	1	1	1	1	*	*	*	*	(8bit DAC)	253/255 × VREF	
				0	1	1	1	1	1	1	1	*	*	*	*		254/255 × VREF	
				1	1	1	1	1	1	1	1	*	*	*	*		VREF	
1	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*		0V	
				1	0	0	0	0	0	0	0	*	*	*	*		1/255 × VREF	
				0	1	0	0	0	0	0	0	*	*	*	*	2.1.1.1111	2/255 × VREF	
												*	*	*	*	2ch hall bias set (8bit DAC)		
				1	0	1	1	1	1	1	1	*	*	*	*	(out DAC)	253/255 × VREF	
				0	1	1	1	1	1	1	1	*	*	*	*		254/255 × VREF	
				1	1	1	1	1	1	1	1	*	*	*	*		VREF	
0	0	1	0	0	0	0	0	0	0	0	0	*	*	*	*		0V	
				1	0	0	0	0	0	0	0	*	*	*	*		$1/255 \times V_{CC}$	
				0	1	0	0	0	0	0	0	*	*	*	*	1ch hall amplifier	2/255 × V _{CC}	
												*	*	*	*	offset adjustment		
				1	0	1	1	1	1	1	1	*	*	*	*	(8bit DAC)	253/255 × V _{CC}	
				0	1	1	1	1	1	1	1	*	*	*	*		254/255 × V _{CC}	
	_			1	1	1	1	1	1	1	1	*	*	*	*		V _{CC}	
1	0	1	0	0	0	0	0	0	0	0	0	*	*	*	*		0V	
				1	0	0	0	0	0	0	0	*	*	*	*		1/255 × V _{CC}	
				0	1	0	0	0	0	0	0	*	*	*	*	2ch hall amplifier	2/255 × V _{CC}	
				,		.		1				*	*	*	*	offset adjustment	252/255 **	
				1	0	1	1	1	1	1	1	*	*	*	*	(8bit DAC)	253/255 × V _{CC}	
				0	1	1	1	1	1	1	1	*	*	*	*		254/255 × V _{CC}	
				1	1	1	1	1	1	1	1	*	*	*	*		v_{CC}	

The PWMh-bridge driver's ON/OFF operation is done with the ST pin.

Hall amplifier gain setting range Hall amplifier relation serial map

			Inj	out					Hall amplifier magnification
A0	A1	A2	A3	D0	D1	D2	D3	Setting mode	()Inside: Resistance
0	0	0	1	0	0	0	0	1ch hall amplifier gain setting	10 (36k//3.6k)
				1	0	0	0	("3" Resistance ÷ "2"	20 (72k//3.6k)
				0	1	0	0	Resistance)	40 (144k//3.6k)
				1	1	0	0		50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0		70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		100 (360k//3.6k)
				0	0	0	1		110 (396k//3.6k)
				1	0	0	1		120 (432k//3.6K)
				0	1	0	1		140 (504k//3.6k)
				1	1	0	1	<u> </u>	150 (540k//3.6k)
				0	0	1	1	<u> </u>	160 (570k//3.6k)
				1	0	1	1	<u> </u>	170 (612k//3.6k)
				0	1	1	1	<u> </u>	190 (684k//3.6k)
				1	1	1	1		200 (720k//3.6k)
1	0	0	1	0	0	0	0	2ch hall amplifier gain setting	10 (36k//3.6k)
				1	0	0	0	("3" Resistance ÷ "2"	20 (72k//3.6k)
				0	1	0	0	Resistance)	40 (144k//3.6k)
				1	1	0	0		50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0		70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		100 (360k//3.6k)
				0	0	0	1		110 (396k//3.6k)
				1	0	0	1		120 (432k//3.6K)
				0	1	0	1		140 (504k//3.6k)
				1	1	0	1		150 (540k//3.6k)
				0	0	1	1		160 (570k//3.6k)
				1	0	1	1		170 (612k//3.6k)
				0	1	1	1		190 (684k//3.6k)
				1	1	1	1		200 (720k//3.6k)
0	1	0	1	0	0	0	0	1ch hall amplifier offset	10 (36k//3.6k)
				1	0	0	0	resistance / input resistance	20 (72k//3.6k)
				0	1	0	0	("1" Resistance ÷ "2"	40 (144k//3.6k)
				1	1	0	0	Resistance)	50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0		70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		100 (360k//3.6k)
				0	0	0	1		110 (396k//3.6k)
				1	0	0	1		120 (432k//3.6K)
				0	1	0	1		140 (504k//3.6k)
				1	1	0	1		150 (540k//3.6k)
				0	0	1	1		160 (570k//3.6k)
				1	0	1	1		170 (612k//3.6k)
				0	1	1	1		190 (684k//3.6k)
				1	1	1	1		200 (720k//3.6k)
1	1	0	1	0	0	0	0	2ch hall amplifier offset	10 (36k//3.6k)
-	1		•	1	0	0	0	resistance / input resistance	20 (72k//3.6k)
				0	1	0	0	("1" Resistance ÷ "2"	40 (144k//3.6k)
				1	1	0	0	Resistance)	50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0		70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		
	ı								100 (360k//3.6k)
		1		0	0	0	1		110 (396k//3.6k)
				1	0	0	1		120 (432k//3.6K)
				^	1				
				0	1	0	1		140 (504k//3.6k)
				1	1	0	1		150 (540k//3.6k)
				1 0	1 0	0	1	-	150 (540k//3.6k) 160 (570k//3.6k)
				1 0 1	1 0 0	0 1 1	1 1 1		150 (540k//3.6k) 160 (570k//3.6k) 170 (612k//3.6k)
				1 0	1 0	0	1		150 (540k//3.6k) 160 (570k//3.6k)

General-purpose amplifier ON/OFF setting

		Inj	put			C-44: 1-	C-ttt	Dl
A0	A1	A2	A3	D0	D1	Setting mode	Set content	Remarks
0	0	1	1	0	*	General-purpose	Stand-by	
				1	*	amplifier 1	Operate	
				*	0	General-purpose	Stand-by	
				*	1	amplifier 2	Operate	

PWM circuit accuracy setting

		Inj	out			C-44: 1-	C-4 4	Dl
A0	A1	A2	A3	D0	D1	Setting mode	Set content	Remarks
1	0	1	1	0	0		10bit resolution	Initial value
				0	1	DW/M	11bit resolution	
				1	0	PWM accuracy setting	12bit resolution	
				*	*		-	

PWM pulse width of moving

1ch (X axis side)

				[3:0]	I			Setting mode	Moving pulse
A0	A1	A2	A3	D0	D1	D2	D3		number
0	1	1	1	0	0	0	0	1ch (X axis) side width of	0 (Initialization)
				1	0	0	0	moving	1
				0	1	0	0		2
				1	1	0	0		3
				0	0	1	0		4
				1	0	1	0		5
				0	1	1	0		6
				1	1	1	0		7
				0	0	0	1		8
				1	0	0	1		9
				0	1	0	1		10
				1	1	0	1		11
				0	0	1	1		12
				1	0	1	1		13
				0	1	1	1		14
				1	1	1	1		15

Note: 1 pulse = 1CLK

2ch (Y axis side)

2CH (1		,	Input	[7:4]				Catting made	Moving pulse
A0	A1	A2	A3	D4	D5	D6	D7	Setting mode	number
0	1	1	1	0	0	0	0	2ch (Y axis) side width of	0 (Initialization)
				1	0	0	0	moving	1
				0	1	0	0		2
				1	1	0	0		3
				0	0	1	0		4
				1	0	1	0		5
				0	1	1	0		6
				1	1	1	0		7
				0	0	0	1		8
				1	0	0	1		9
				0	1	0	1		10
				1	1	0	1		11
				0	0	1	1		12
				1	0	1	1		13
				0	1	1	1		14
				1	1	1	1		15

Note: 1 pulse = 1CLK

The ON/OFF operation of the hall amplifier and the hall bias is done with the ST pin.

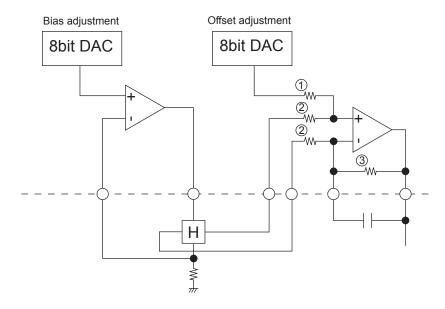
Note: An initial value of A0 to A3 = 1111 is a static test mode. Use it specifying data D0 for one.

TEST mode setting

in the setting									
Input					C-44: 1-	Comtant	Damada		
A0	A1	A2	A3	D0	Setting mode	Content	Remarks		
1	1	1	1	0	NC pin _ TEST mode	External CLK	It uses it by the shipment inspection.		
				1		Internal CLK	Internal CLK operation		

Note: External CLK mode is for the shipment inspection. Use it with internal CLK. Use it after it internal CLK switches because default is external CLK mode.

Hall bias, Offset adjustment circuit configuration



Hall amplifier, Hall bias equivalent circuit

About the gain adjustment

The resistance ratio of "2" and "3" is adjusted in figure and the gain is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

About the Offset adjustment

The resistance ratio of "1" and "2" is adjusted in figure and the Offset is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

Note in design

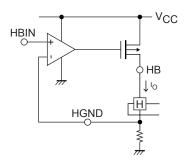
• Stand-by function

IC becomes a stand-by state at ST = "L", and IC enters the state of operation at ST = "H". Moreover, the register in IC is reset as for ST = "L" at times.

• Hall bias

The constant current output is built into for the hall element drive. The constant current value is set from detection resistance (RHG) connected from the HBIN pin impression voltage and the HGND pin between GND.

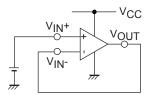
Constant current value (I_O) = HBIN voltage \div Detection resistance



Constant current value (IO) becomes about 1mA when assuming HBIN pin impressed voltage =1.0V and detection resistance = 1 $k\Omega$ from the above-mentioned calculation type. Moreover, the HGND pin must connect with the HB pin, and connect the detection resistance of a large value as much as possible when you do not use the hall bias circuit.

• Operation amplifier

Impress the bias to the V_{IN} + pin, and compose the buffer by the connection to the VOUT pin in the V_{IN} - pin in the operational amplifier not used.



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV8415XA-MH	WLP32L (2.47mm × 2.47mm) (Pb-Free / Halogen Free)	5000 / Tape & Reel

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