DESCRIPTION

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin (9) connected to pin (14), pins (10), (11) open) an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

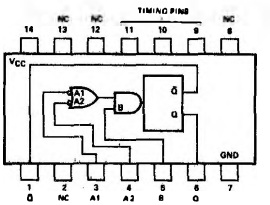
Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T - 40kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

PIN CONFIGURATIONS

A, F, W PACKAGE



TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

$1 = V_{in(1)} \geq 2V$ $\quad$ $0 = V_{in(0)} \leq 0.8V$

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
3. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of 30ns is obtained typically.
4. To use the internal timing resistor (2kΩ nominal), connect pin (9) to pin (14).
5. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
6. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.
7. t_n = time before input transition.
8. t_{n+1} = time after input transition.
9. x indicates that either a logical 0 or 1, may be present.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:				V
N74121 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Input Pulse Rise/Fall Time: Schmitt Input (B)			1	V/s
Logic Inputs (A1, A2)			1	V/μs
Input Pulse Width	50			ns
External Timing Resistance Between Pins (11) and (14) (Pin (9) open)	1.4			kΩ
External Timing Resistance: S54121			30	kΩ
N74121			40	kΩ
Timing Capacitance	0		1000	μF
Output Pulse Width			40	s
Duty Cycle: R_T = 2kΩ			67%	
R_T = 30kΩ (S54121) or			90%	
R_T = 40kΩ (N74121)				

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN				1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN			0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN				1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN			0.8	1.35		V
V_{out} (0)	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
V_{out} (1)	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.3		V
I_{in} (0)	Logical 0 level input current at A_1 of A_2	V_{CC} = MAX,	V_{in} = 0.4V			-1	-1.6	mA
I_{in} (0)	Logical 0 level input current at B	V_{CC} = MAX,	V_{in} = 0.4V			-2	-3.2	mA
I_{in} (1)	Logical 1 level input current at A_1 of A_2	V_{CC} = MAX,	V_{in} = 2.4V			2	40	μA
		V_{CC} = MAX,	V_{in} = 5.5V			0.05	1	mA
I_{in} (1)	Logical 1 level input current at B	V_{CC} = MAX,	V_{in} = 2.4V			4	80	μA
		V_{CC} = MAX,	V_{in} = 5.5V			0.05	1	mA
I_{OS}	Short circuit output current at Q or $\overline{Q}$†	V_{CC} = MAX		S54121	-20	-25	-55	mA
				N74121	-18	-25	-55	mA
I_{CC}	Power supply current in quiescent (unfired) state	V_{CC} = MAX				13	25	mA
I_{CC}	Power supply current in fired state	V_{CC} = MAX				23	40	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from B input to Q output	C_L = 15pF,	C_T = 80pF	15	35	55	ns
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to Q output	C_L = 15pF,	C_T = 80pF	25	45	70	ns
t_{pd0}	Propagation delay time to logical 0 level from B input to $\overline{Q}$ output	C_L = 15pF,	C_T = 80pF	20	40	65	ns
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output	C_L = 15pF,	C_T = 80pF	30	50	80	ns
$t_{p(out)}$	Pulse width obtained using internal timing resistor	C_L = 15pF, R_T = Open,	C_T = 80pF Pin (9) to V_{CC}	70	110	150	ns
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	C_L = 15pF, R_T = Open,	C_T = 0. Pin (9) to V_{CC}	20	30	50	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	C_L = 15pF, R_T = 10kΩ	C_T = 100pF, Pin (9) Open	600	700	800	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	C_L = 15pF, R_T = 10kΩ	C_T = 1μF, Pin (9) Open	6	7	8	ms
t_{hold}	Minimum duration of trigger pulse	C_L = 15pF, R_T = Open,	C_T = 80pF, Pin (9) to V_{CC}		30	50	ns

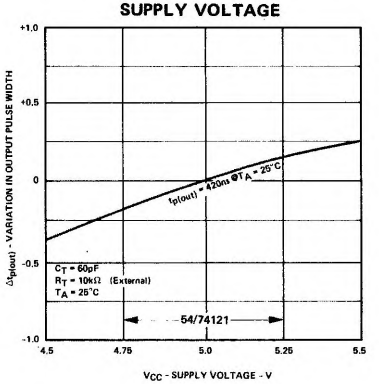
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

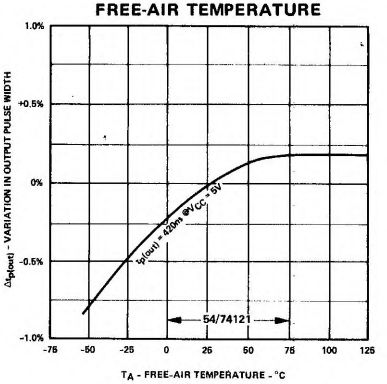
† Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS

VARIATION IN OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

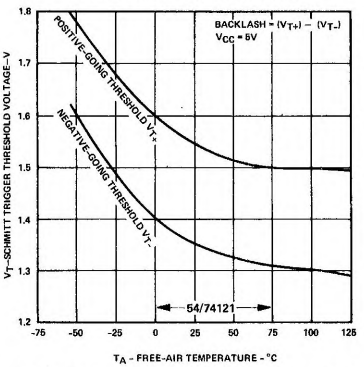


VARIATION IN OUTPUT PULSE WIDTH VERSUS FREE-AIR TEMPERATURE

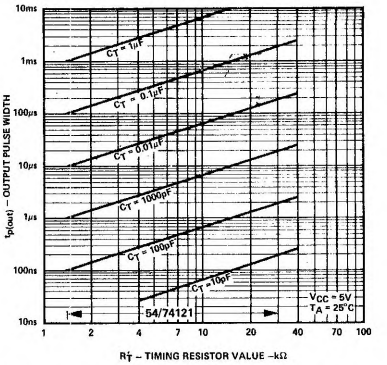


TYPICAL CHARACTERISTICS (Cont'd)

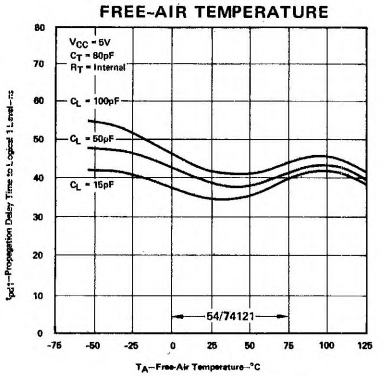
SCHMITT TRIGGER THRESHOLD VOLTAGE VERSUS FREE-AIR TEMPERATURE



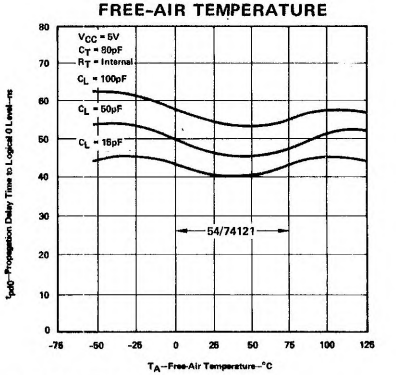
OUTPUT PULSE WIDTH VERSUS TIMING RESISTOR VALUE



PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL (B INPUT TO Q OUTPUT) VERSUS FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL (B INPUT TO Q OUTPUT) VERSUS FREE-AIR TEMPERATURE



VARIATION IN INTERNAL TIMING RESISTOR VALUE VERSUS FREE-AIR TEMPERATURE