SYNCHRONOUS 4-BIT COUNTER

S54160 N74160
S54161 N74161
S54162 N74162
S54163 N74163

S54160–B,F,W • S54161–B,F,W • S54162–B,F,W • S54163–B,F,W
N74160–B,F • N74161–B,F • N74162–B,F • N74163–B,F

DIGITAL 54/74 TTL SERIES

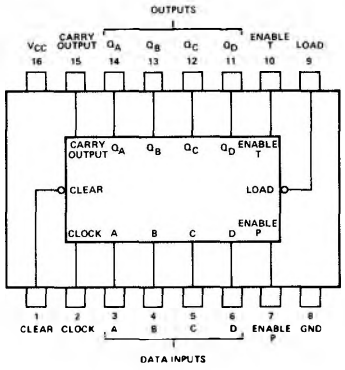
DESCRIPTION

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The S54160, S54162, N74160, and N74162 are decade counters and the S54161, S54163, N74161, and N74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs and power dissipation is typically 325 milliwatts.

PIN CONFIGURATION

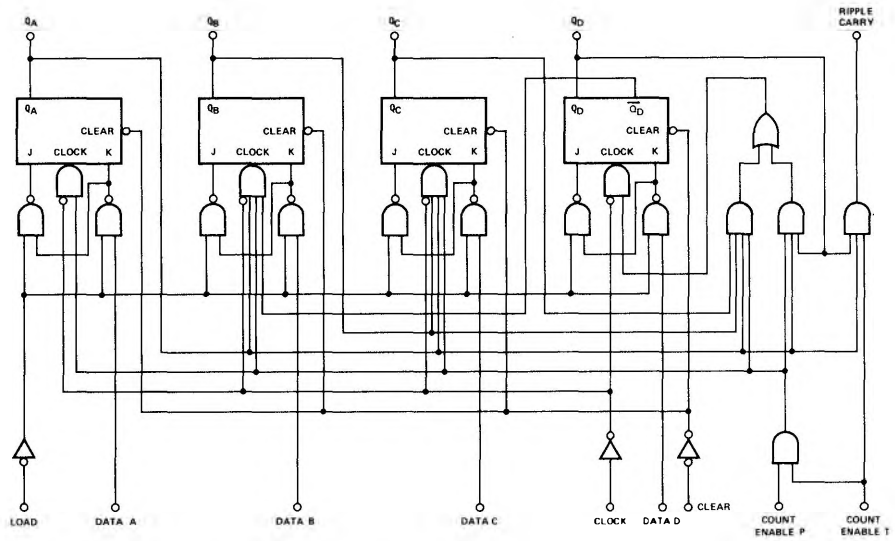
B,F,W PACKAGE



LOGIC DIAGRAM

S54160/N74160 SYNCHRONOUS DECADE COUNTERS

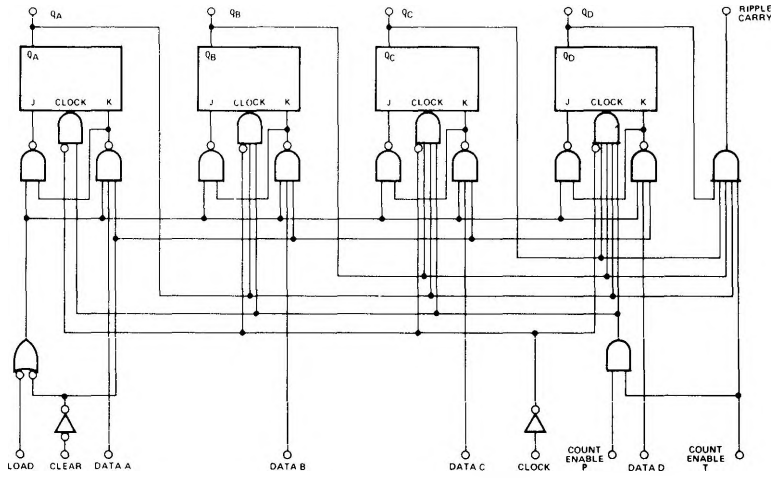
(S54162/N74162 synchronous decade counters are similar; however the clear is synchronous as shown for the S54163/N74163 binary counters).



LOGIC DIAGRAM (Cont'd)

S54163/N74163 SYNCHRONOUS BINARY COUNTERS

S54161/N74161 synchronous binary counters are similar; however the clear is asynchronous as shown for the S54160/N74160 decade counters).



RECOMMENDED OPERATING CONDITIONS

	S54160, S54161 S54162, S54163			N74160, N74161 N74162, N74163			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock Pulse, $t_{w(clock)}$	25			25			ns
Width of Clear Pulse, $t_{w(clear)}$	20			20			ns
Setup Time, t_{setup}: Data Inputs, A,B,C,D	15			15			
Enable P	20			20			
Load	15			15			ns
Clear	20			20			
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise specified)

PARAMETER		TEST CONDITIONS*		S54160,S54161 S54162,S54163			N74160,N74161 N74162,N74163			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage	V_{CC} = MAX,				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current: Clock or enable T	V_{CC} = MAX,	V_I = 2.4V			80			80	μA
	Other inputs					40			40	
I_{IL}	Low-level input current: Clock or enable T	V_{CC} = MAX,	V_I = 0.4V			-3.2			-3.2	mA
	Other inputs					-1.6			-1.6	
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-57	-18		-57	mA
I_{CCL}	Supply current, all outputs high	V_{CC} = MAX,	See Note 3		59	85		59	94	mA
	Supply current, all outputs low	V_{CC} = MAX,	See Note 4		63	91		63	101	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15pF, R_L = 400Ω	25	32		MHz
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock			13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock			15	23	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T			8	13	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear			20	30	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

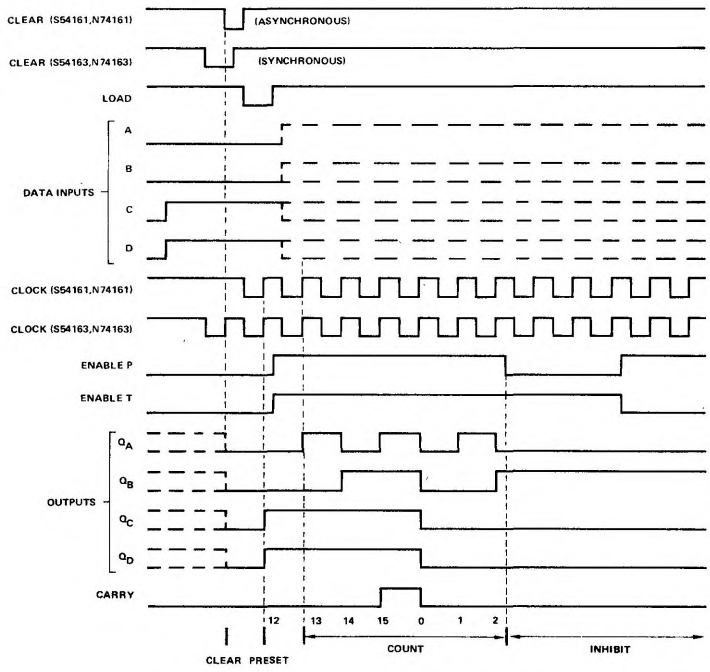
NOTES:

3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

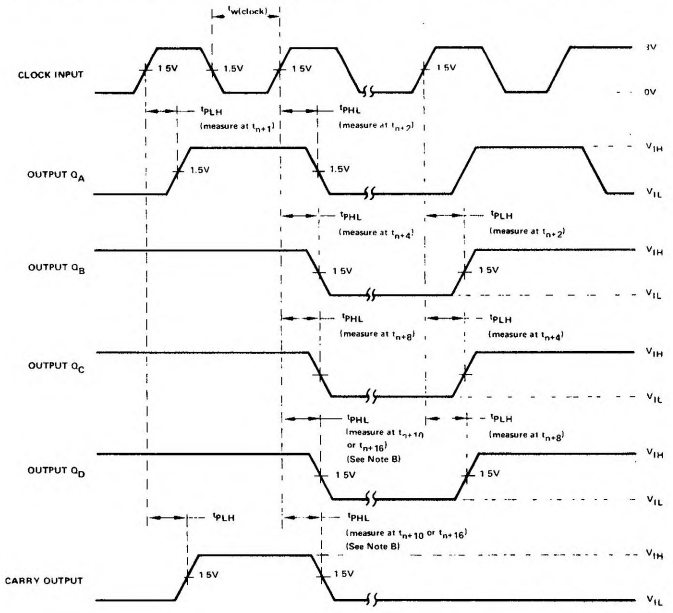
TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



PARAMETER MEASUREMENT INFORMATION

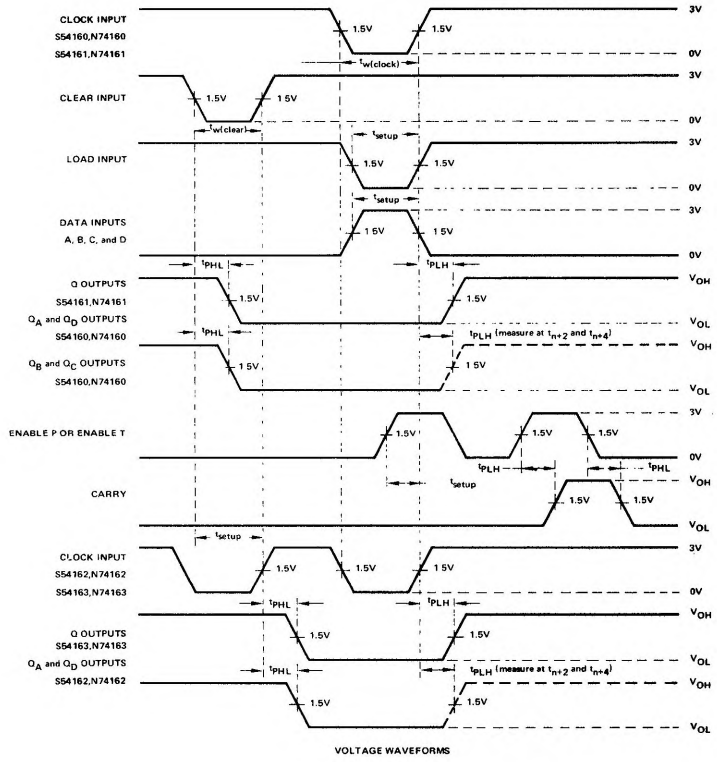


VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ns; $t_f \leq 10$ns. PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\Omega$. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the S54160, S54162, N74160, and N74162, and at t_{n+16} for the S54161, S54163, N74161, and N74163, where t_n is the bit time when all outputs are low.



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ns; $t_f \leq 10$ns; PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%; $Z_{out} \approx 50\Omega$.

B. Enable P and enable T setup times are measured at $t_n = 0$.