

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54181 and 74181 are high-speed arithmetic logic units (ALU)/function generators which have a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the 54181/74181 for fast, simultaneous carry generation with a group carry propagate (P) and carry generate (G) for the 4 bits in the package. When used in conjunction with the 54182 or 74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. For example, the typical addition time for the 54181/74181 is 24 nanoseconds for 4 bits. When expanding to 16-bit addition with the 54182/74182, only 13 nanoseconds, further delay is added so that the total addition time is 35 nanoseconds, or 2.2 nanoseconds per bit. One 54182/74182 is needed for every 16 bits (four 54181/74181 circuits).

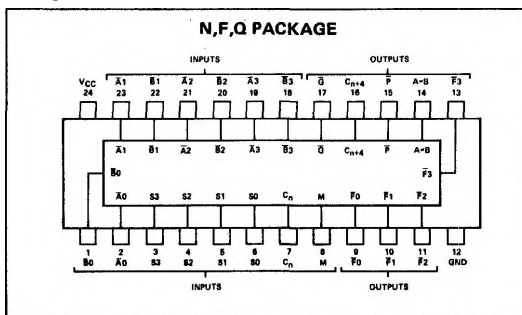
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry. The typical delay for the ripple carry is 12 nanoseconds for four bits, addition of two 8-bit words is accomplished typically in 36 nanoseconds when employing the ripple carry.

The 54181/74181 will accommodate active-high or active-low data if the pin-designations are reinterpreted as follows:

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR and OR functions.

The 54181/74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time. All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs.

PIN CONFIGURATION



PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data	A ₀	B ₀	A ₁	B ₁	A ₂	B ₂	A ₃	B ₃	F ₀	F ₁	F ₂	F ₃	C _n	C _{n+4}	X	Y
Active-low data	A ₀	B ₀	A ₁	B ₁	A ₂	B ₂	A ₃	B ₃	F ₀	F ₁	F ₂	F ₃	C _n	C _{n+4}	P	G

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1 which requires an end-around or forced carry to provide A-B.

The 54181 is characterized for operation over the full military temperature range of -55°C to 125°C; the 74181 is characterized for operation from 0°C to 70°C.

TRUTH TABLE FOR COMPARATOR APPLICATION

	Input C _n	Output C _{n+4}	Indicates
Active-high Data	H	H	A < B
	L	H	A < B
	H	L	A > B
	L	L	A > B
Active-low Data	L	L	A < B
	H	L	A < B
	L	H	A > B
	H	H	A > B

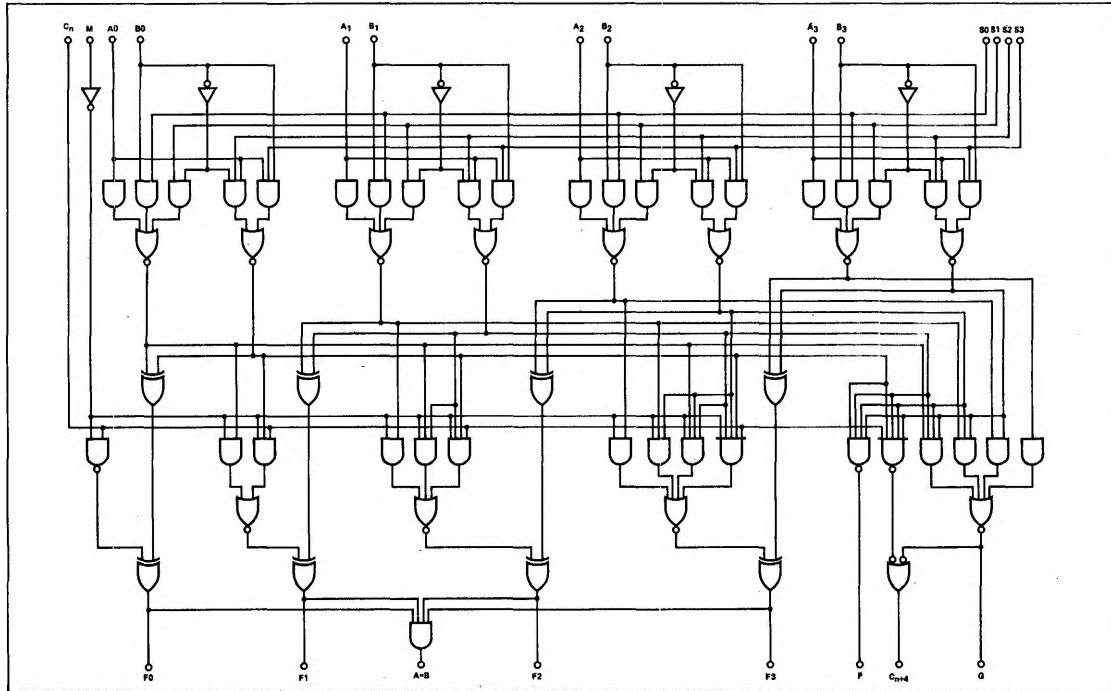
The 54181/74181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high-level state to indicate equality (A = B). The 54181/74181 should be in the subtract mode when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the control lines at LHHH.

FUNCTION TABLES

SELECTION S ₃ S ₂ S ₁ S ₀	M-H LOGIC FUNCTIONS	ACTIVE-HIGH DATA	
		M = L: ARITHMETIC OPERATIONS	
		C _n = 0	C _n = 1
		C _n - 1 = H	C _n = 0 = L
L L L L	F = \bar{A}	F = A	F = A PLUS 1
L L L L	F = $A + \bar{B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $\bar{A} \cdot \bar{B}$	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L L H L	F = $\bar{A} \cdot B$	F = A PLUS $\bar{A} \cdot B$	F = A PLUS $\bar{A} \cdot B$ PLUS 1
L H L H	F = \bar{B}	F = (A + B) PLUS $\bar{A} \cdot \bar{B}$	F = (A + B) PLUS $\bar{A} \cdot \bar{B}$ PLUS 1
L H L H	F = $A \odot B$	F = A MINUS B MINUS 1	F = A MINUS B
L H H L	F = $\bar{A} \cdot \bar{B}$	F = $\bar{A} \cdot \bar{B}$ MINUS 1	F = $\bar{A} \cdot \bar{B}$
L H H L	F = $\bar{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L L	F = $\bar{A} + \bar{B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L L H	F = $\bar{A} \odot \bar{B}$	F = (A + \bar{B}) PLUS AB	F = (A + \bar{B}) PLUS AB PLUS 1
H L H L	F = B	F = AB MINUS 1	F = AB
H L H H	F = AB	F = AB PLUS 1	F = A PLUS A PLUS 1
H H L L	F = 1	F = A PLUS A	F = (A + \bar{B}) PLUS A PLUS 1
H H L H	F = $\bar{A} + \bar{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = $\bar{A} + B$	F = (A + \bar{B}) PLUS A	F = (A + \bar{B}) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

SELECTION S ₃ S ₂ S ₁ S ₀	M-H LOGIC FUNCTIONS	ACTIVE LOW DATA	
		M = L: ARITHMETIC OPERATIONS	
		C _n = 0	C _n = 1
		C _n = 0 = L	C _n = 1 = H
L L L L	F = \bar{A}	F = A MINUS 1	F = A
L L L H	F = $\bar{A} \cdot \bar{B}$	F = AB MINUS 1	F = AB
L L H L	F = $\bar{A} + \bar{B}$	F = $\bar{A} \cdot \bar{B}$ MINUS 1	F = $\bar{A} \cdot \bar{B}$
L L H H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO
L L H L	F = $\bar{A} + B$	F = A PLUS (A + \bar{B}) PLUS 1	F = A PLUS (A + \bar{B}) PLUS 1
L H L H	F = \bar{B}	F = AB PLUS (A + \bar{B})	F = AB PLUS (A + \bar{B}) PLUS 1
L H L H	F = $A \odot B$	F = A MINUS B MINUS 1	F = A MINUS B
L H H L	F = $\bar{A} + \bar{B}$	F = A + \bar{B}	F = A + \bar{B} PLUS 1
L H L L	F = $\bar{A} \cdot B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = $\bar{A} \odot B$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = $\bar{A} \cdot \bar{B}$ PLUS (A + B)	F = $\bar{A} \cdot \bar{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A	F = A PLUS A PLUS 1
H H L H	F = $\bar{A} \cdot \bar{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = $\bar{A} \cdot \bar{B}$ PLUS A	F = $\bar{A} \cdot \bar{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

LOGIC DIAGRAM



RECOMMENDED OPERATING CHARACTERISTICS

	S54181			N74181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:							
High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

DIGITAL 54/74 TTL SERIES ■ S54181, N74181

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OH} = -800\mu A$	2.4			V
V_{OL} Low-level output voltage any output except A=B	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OL} = 16\text{mA}$			0.4	V
I_{OH} High-level output current A=B only	$V_{CC} = \text{MIN}, V_{IN} = 2V$ $V_{IL} = 0.80, V_{OH} = 5.5V$			250	μA
I_{IH} High-level input current (mode input)				40	μA
I_{IH} High-level input current (any A or B input)				120	μA
I_{IH} High-level input current (any S input)	$V_{CC} = \text{MAX}, V_I = 2.4V$			160	μA
I_{IH} High-level input current (carry input)				200	μA
I_{IH} High-level input current (any input)	$V_{CC} = \text{MAX}, V_I = 5.5V$			1	mA
I_{IL} Low-level input current (mode input)				-1.6	mA
I_{IL} Low-level input current (any A or B input)	$V_{CC} = \text{MAX}, V_I = 0.4V$			-4.8	mA
I_{IL} Low-level input current (any S input)				-6.4	mA
I_{IL} Low-level input current (carry input)				-8	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	S54181 -20 N74181 -18		-55 -57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$	S54181 88 N74181 88	88	127 140	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$	S54181 94 N74181 94	94	135 150	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5V, T_A = 25^\circ C, N = 10 (C_L = 15\text{pF}, R_L = 400\Omega)$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	C_n	C_{n+4}			12 13	18 19	ns
t_{PLH} t_{PHL}	C_n	Any F	M = 0V (SUM or DIFF mode)		13 12	19 18	ns
t_{PLH} t_{PHL}	Any A or B	G	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)		13 13	19 19	ns
t_{PLH} t_{PHL}	Any A or B	G	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)		17 17	25 25	ns
t_{PLH} t_{PHL}	Any A or B	P	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)		13 17	19 25	ns
t_{PLH} t_{PHL}	Any A or B	P	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)		17 17	25 25	ns
t_{PLH} t_{PHL}	Any A or B	Any F	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)		28 21	42 32	ns
t_{PLH} t_{PHL}	Any A or B	Any F	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)		32 23	48 34	ns
t_{PLH} t_{PHL}	Any A or B	Any F	M = 4.5V (logic mode)		32 23	48 34	ns
t_{PLH} t_{PHL}	Any A or B	A = B	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)		35 32	50 48	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC} = 5V, T_A = 25^\circ C$.

† t_{PLH} = propagation delay time, low-to-high-level output t_{PHL} = propagation on delay time, high-to-low-level output

§ Not more than one output should be shorted at a time

TYPICAL APPLICATION DATA

Typical addition times for various configurations are given in the table below. Subtraction times are in the same range as summation times.

TYPICAL ADDITION TIMES

NO. OF BITS	TOTAL ADDITION TIME (ns)	ADD TIME PER BIT (ns)	PACKAGE COUNT	
			S54181/ N74181	S54182 N74182
4	24	6.0	1	
8	36	4.5	2	
12	48	4.0	3	
12	36	3.0	3	1
16	60	3.8	4	
16	36	2.2	4	1
32	120	3.8	8	
32	96	3.0	8	1
32	72	2.2	8	2
32	60	1.9	8	3
48	165	3.4	12	
48	148	3.1	12	1
48	132	2.7	12	2
48	108	2.2	12	3
48	60	1.25	12	4
64	220	3.5	16	
64	192	3.0	16	2
64	172	2.7	16	3
64	144	2.2	16	4
64	60	0.94	16	5

