4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

S54194
N74194

S54194–B,F,W • N74194–B, F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

	MODE CONTROL S1	S0
Parallel (Broadside) Load	H	H
Shift Right (In the direction Q_A toward Q_D)	L	H
Shift Left (In the direction Q_D toward Q_A)	H	L
Inhibit Clock (Hold)	L	L

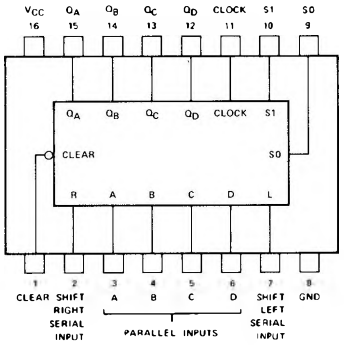
In the parallel-load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode controls should be changed only while the clock input is high.

These 4-bit shift registers are compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 36 megahertz and power dissipation is typically 195mW.

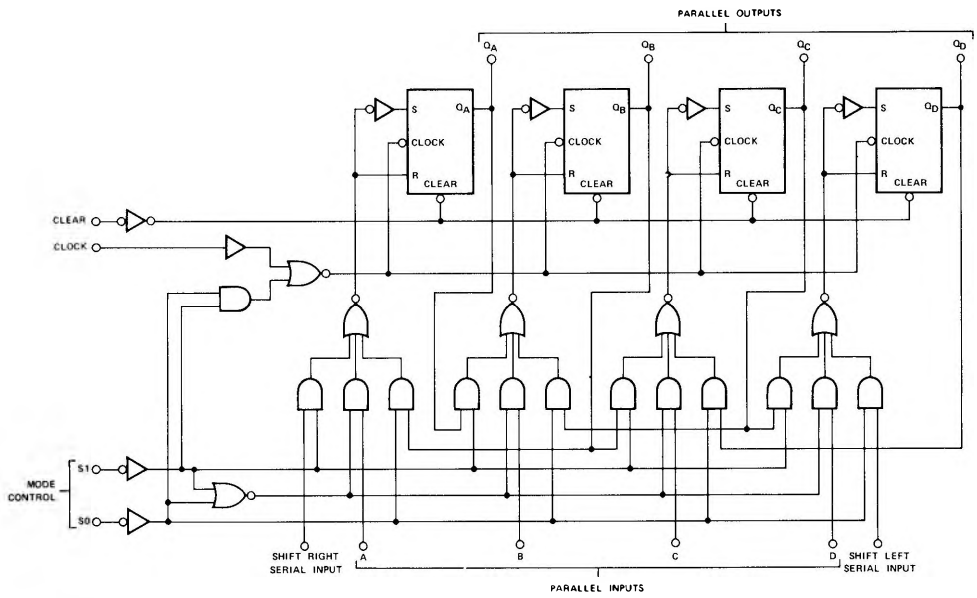
The S54194 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74194 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54194			N74194			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Setup Time, t_{setup}: Mode control	30			30			ns
Serial and parallel data	20			20			ns
Clear inactive-state	25			25			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12mA				-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX		S54194	-20		-57	mA
				N74194	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			39	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15pF,	R_L = 400Ω	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear				19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			7	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			7	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.