signetics

QUADRUPLE BISTABLE LATCH

S5475
N7475

S5475-B • N7475-B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5475B/N7475B is a monolithic, quadruple, bistable latch with complementary Q and $\overline{Q}$ outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

TRUTH TABLE

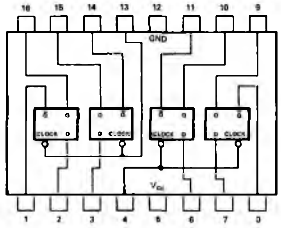
LOGIC

(Each Latch)		
t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1

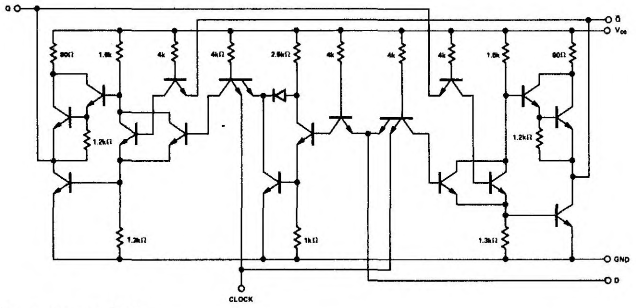
NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse
3. These voltages are with respect to network ground terminal.

PIN CONFIGURATIONS

B PACKAGE



SCHEMATIC (each latch)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): S5475 Circuits	4.5	5	5.5	V
N7475 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Outputs			10	
Operating Free-Air Temperature Range, T_A: S5475 Circuits	-55	25	125	°C
N7475 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	$I_{load} = -400\mu A$	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current at D	V_{CC} = MAX,	V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,				-6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX,	V_{in} = 2.4V			80	µA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX	V_{in} = 2.4V			160	µA
		V_{CC} = MAX	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	S5475	-20		-75	mA
		V_{out} = 0	N7475	-18		-75	mA
I_{CC}	Supply current	V_{CC} = MAX,	S5475		32	46	mA
			N7475		32	53	mA

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS NOTE A		MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	6¶		ns
$t_{pd1(D\text{-}Q)}$	Propagation delay time to logical 1 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(D\text{-}Q)}$	Propagation delay time to logical 0 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		14	25	ns
$t_{pd1(D\text{-}\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		24	40	ns
$t_{pd0(D\text{-}\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd1(C\text{-}Q)}$	Propagation delay time to logical 1 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C\text{-}Q)}$	Propagation delay time to logical 0 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd1(C\text{-}\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C\text{-}\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		7	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

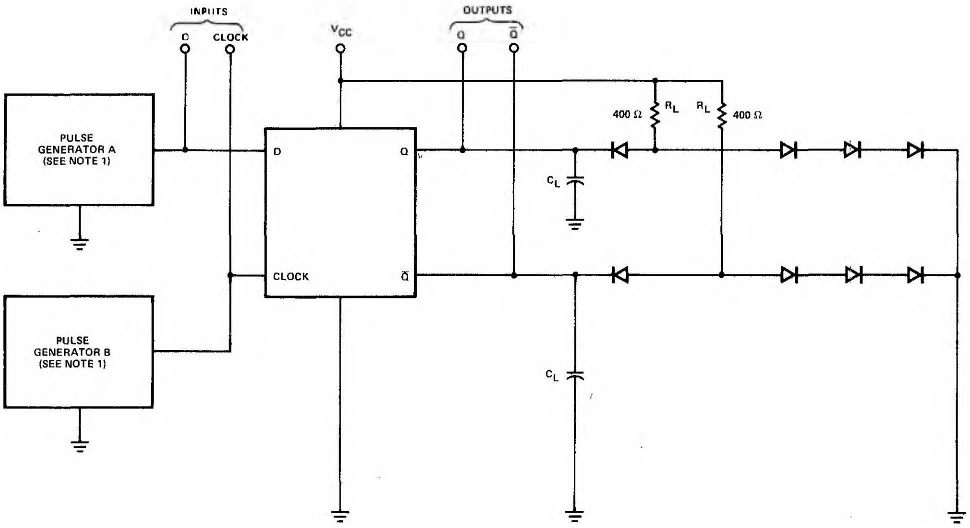
† Not more than one output should be shorted at a time.

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

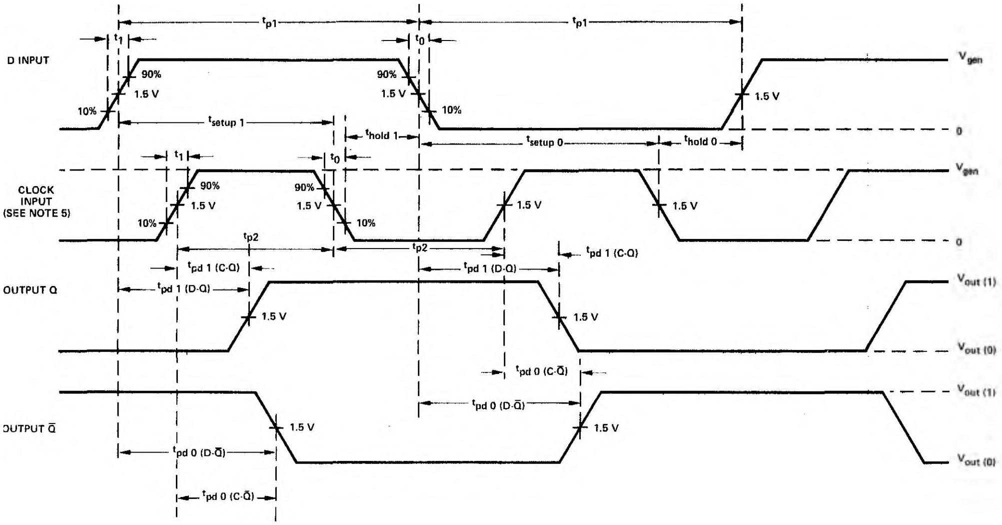
Note A AC Test circuit, voltage waveforms and switching times are given on page 2-76.

SWITCHING CHARACTERISTICS*

TEST CIRCUIT



VOLTAGE WAVEFORMS AND SWITCHING TIMES



NOTES:
1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leqslant 10$ ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A t_{p1} = 1 μs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.
5. When measuring $t_{pd1(D\text{-}Q)}$ and $t_{pd0(D\text{-}Q)}$ (or $t_{pd0(D\text{-}\bar{Q})}$ and $t_{pd1(D\text{-}\bar{Q})}$ for the S5474/N7475), clock input must be held at logical 1.

†Complementary Q outputs are on the S5475/N7475 only.