

DESCRIPTION

The 54/7483 is a 4-Bit Binary Full Adder for adding two four bit binary numbers. A Carry Look Ahead circuit is included to provide minimum carry propagation delays.

Propagation delays of carry-in to carry-out is typically 12 nsec.

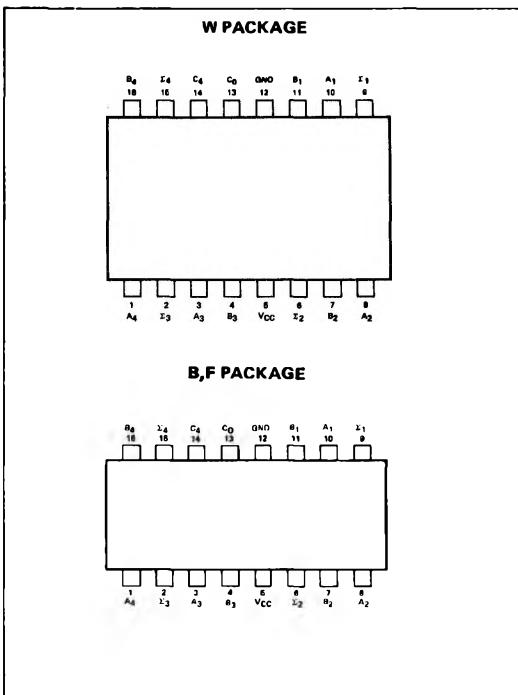
TRUTH TABLE

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
				Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
A_1	B_1	A_2	B_2	Σ_3	Σ_4	C_4	Σ_3	Σ_4	C_4
A_3	B_3	A_4	B_4	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	0	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTES:

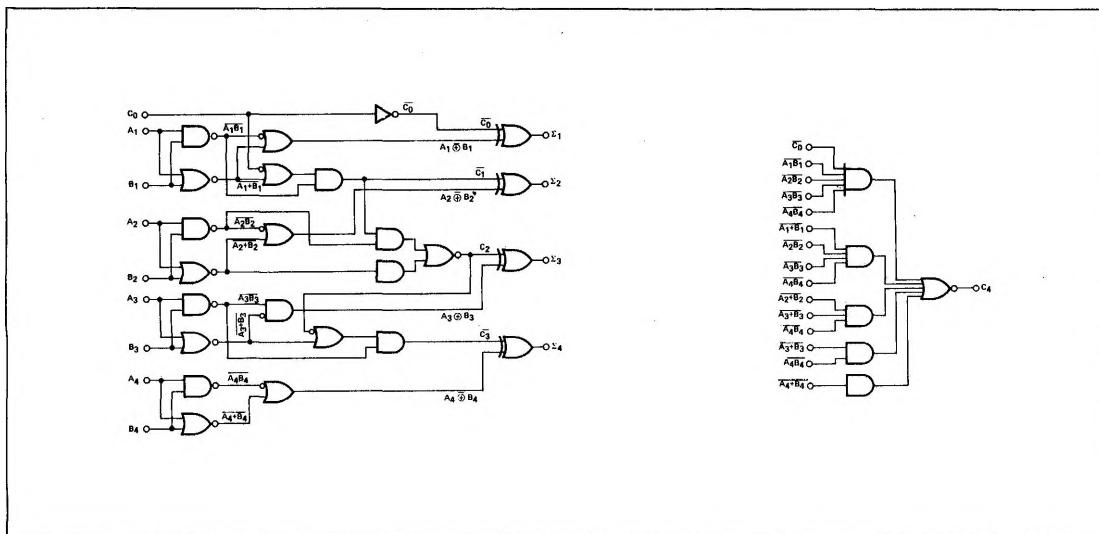
Input conditions at A_1 , A_2 , B_1 , B_2 , and C_0 are used to determine outputs Σ_1 and Σ_2 , and the value of the internal carry C_2 . The

PIN CONFIGURATIONS



values at C_2 , A_3 , B_3 , A_4 , and B_4 , are then used to determine outputs Σ_3 , Σ_4 , and C_4 .

LOGIC DIAGRAM



DIGITAL 54/74 TTL SERIES ■ S5483, N7483

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : (See Note 1)	S5483 Circuits N7483 Circuits	4.5 4.75	5	5.5 5.25 5 10	V V
Normalized Fan-Out From Outputs:	C_4 $\Sigma_1, \Sigma_2, \Sigma_3$ or Σ_4				

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal $V_{CC} = MIN$	2			V
$V_{in(0)}$	Input voltage required to ensure logical 1 at any input terminal $V_{CC} = MIN$		0.8		V
$V_{out(1)}$	Logical 1 output voltage $V_{CC} = MIN$	2.4			V
$V_{out(0)}$	Logical 0 output voltage $V_{CC} = MIN$		0.4		V
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3 , or C_0 $V_{CC} = MAX, V_{in} = 0.4V$		-3.2		mA
$I_{in(0)}$	Logical 0 level input current at A_2, A_4, B_2 , or B_4 $V_{CC} = MAX, V_{in} = 0.4V$		-1.6		mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_3, B_1, B_3 , or C_0 $V_{CC} = MAX, V_{in} = 2.4V$	80			μA
$I_{in(1)}$	Logical 1 level input current at A_2, A_4, B_2 , or B_4 $V_{CC} = MAX, V_{in} = 5.5V$	1			mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_3, B_1, B_3 , or C_0 $V_{CC} = MAX, V_{in} = 2.4V$	40			μA
$I_{in(1)}$	Logical 1 level input current at A_2, A_4, B_2 , or B_4 $V_{CC} @ MAX, V_{in} = 5.5V$	1			mA
I_{OS}	Short-circuit output current at $\Sigma_1, \Sigma_2, \Sigma_3$, or Σ_4 † $V_{CC} = MAX$	-20	-55		mA
I_{OS}	Short-circuit output current at $\Sigma_1, \Sigma_2, \Sigma_3$, or Σ_4 † $V_{CC} = MAX$	-18	-55		mA
I_{CC}	Supply current $V_{CC} = MAX$	58	79		mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, unless otherwise noted N = 10

PARAMETER ‡	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1} From C_0 to 1	$C_L = 50pF, R_L = 400\Omega$	23	34		ns
t_{pd0} From C_0 to 1	$C_L = 50pF, R_L = 400\Omega$	20	34		ns
t_{pd1} From C_0 to 2	$C_L = 50pF, R_L = 400\Omega$	24	35		ns
t_{pd0} From C_0 to 2	$C_L = 50pF, R_L = 400\Omega$	22	35		ns
t_{pd1} From C_0 to 3	$C_L = 50pF, R_L = 400\Omega$	30	50		ns
t_{pd0} From C_0 to 3	$C_L = 50pF, R_L = 400\Omega$	24	40		ns
t_{pd1} From C_0 to 4	$C_L = 50pF, R_L = 400\Omega$	30	50		ns
t_{pd0} From C_0 to 4	$C_L = 50pF, R_L = 400\Omega$	28	50		ns
t_{pd1} From C_0 to C_4	$C_L = 50pF, R_L = 780\Omega$	12	20		ns
t_{pd0} From C_0 to C_4	$C_L = 50pF, R_L = 780\Omega$	12	20		ns
t_{pd1} From A_2 or B_2 to 2	$C_L = 50pF, R_L = 400\Omega$	40			ns
t_{pd0} From A_2 or B_2 to 2	$C_L = 50pF, R_L = 400\Omega$	35			ns
t_{pd1} From A_4 of B_4 to 4	$C_L = 50pF, R_L = 400\Omega$	40			ns
t_{pd0} From A_4 of B_4 to 4	$C_L = 50pF, R_L = 400\Omega$	35			ns

† t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

† Not more than one output should be shorted at a time.

NOTE 1: These voltage values are with respect to network ground terminal.