Signetics

5-BIT SHIFT REGISTER

S5496 N7496

\$5496-B.F.W • N7496-B.F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

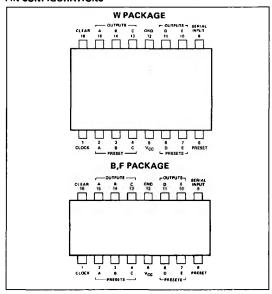
This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

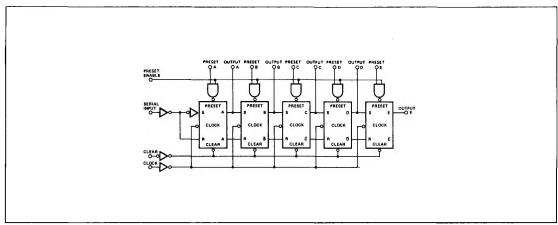
The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

PIN CONFIGURATIONS



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|--|----------------|------|-----|------|------|
| Supply Voltage V _{CC} | S5496 Circuits | 4.5 | 5 | 5.5 | V |
| | N7496 Circuits | 4.75 | 5 | 5.25 | ٧ |
| Normalized Fan-Out from Ou | itput | | | 10 | |
| Width of Clock Pulse, tp(cloc | k) | 35 | | | ns |
| Width of Clear Pulse, tolclear |) | 30 | | | ns |
| Width of Preset Pulse, tp(pres | et) | 30 | | | ns |
| Serial Input Setup Time, t _{sett} | ıp | 30 | | | ns |
| Serial Input Hold Time, t _{hold} | | 0 | | | ns |
| | | | | 1 | |

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------------|--|--|------------------------|------------|----------|--------------------|------------------|
| V _{in(1)} | Input voltege required to ensure logical 1 at any input terminal | V _{CC} - MIN | | 2 | | | v |
| V _{in(0)} | Input voltage required to ensure logical 0 at any input terminal | V _{CC} = MIN | | | | 0.8 | v |
| V _{out(1)} | Logical 1 output voltage | V _{CC} = MIN, I _{load} = -400mA | | 2.4 | 3.5 | | v |
| $V_{out(0)}$ | Logical 0 output voltage | V _{CC} = MIN, I _{sink} = 16mA | | { | 0.22 | 0.4 | v |
| l _{in(1)} | Logical 1 level input current at any input except preset (pin 8) | V _{CC} = MAX, V _{in} = 2.4V V _{CC} = MAX, V _{in} = 5.6V | | | | 40 1 | μ Α mA |
| ¹ in(1) | Logical 1 level input current at preset (pin 8) Logical 0 level input current | V _{CC} = MAX, V _{in} = 2.4V V _{CC} = MAX, V _{in} = 5.5V | | | | 200 1 | μA mA |
| lin(0) | at any input except preset (pin (8)) | V _{CC} = MAX, V _{in} = 0.4V | | | | -1.6 | mA |
| ¹ in(0) | Logical 0 level input current at preset (pin 8) | V _{CC} = MAX, V _{in} = 0.4V | | | | -8 | mA |
| los | Short-circuit output current | V _{CC} = MAX, V _{out} = 0 | S54 96 N7496 | -20 -18 | | -57 - 57 | mA mA |
| lcc | Supply current | V _{CC} = MAX | S5496 N7496 | | 48 48 | 68 79 | mA mA |

SWITCHING CHARACTERISTICS, V_{CC} = 6V, T_A = 25°C, N = 10

| PARAMETER | | TES | TEST CONDITIONS | | TYP | MAX | UNIT |
|------------------|-------------------------------|------------------------|-----------------------|----------|-----|-----|------|
| f _{max} | Maximum clock frequency | C _L = 15pF, | R _L = 400Ω | 10 | | - \ | MHz |
| | Propagation delay time to | | | 1 | | | l |
| ^t pd1 | logical 1 level from clock to | C _L = 15pF, | $R_L = 400\Omega$ | | 25 | 40 | ns |
| • | output | | | } | | | |
| | Propagation delay time to | | | \ | | | 1 |
| t _{pd0} | logical 0 level from clock to | C _L = 15pF, | R _L = 400Ω | | 25 | 40 | ns |
| pue | output | _ | | 1 | | | l |
| | Propagation delay time to | | | | | | 1 |
| ^t pd1 | logical 1 level from preset | C _L = 15pF, | $R_L = 400\Omega$ | | | 35 | ns |
| | to output | _ | | | | | |
| | Propagation delay time to | | | 1 | | | |
| ^t pd0 | logical O level from preset | C ₁ = 15pF, | $R_1 = 400\Omega$ | 1 | 28 | 40 | ns |
| | to output | | - | | | | Ì |
| | Propagation delay time to | | | | | | ļ |
| ^t pd0 | logical 0 level from clear | C ₁ = 15pF, | R ₁ = 400 | | | 55 | ns |
| | to output | | - | | | | |

^{*} For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable

^{*•} All typical values are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.
† Not more than one output should be shorted at a time.